Reference DESIGN

Variable x Variable Multiplier RPMs for Virtex

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Features

- Library of fixed size, parallel multiplier point solutions
- Drop-in modules for the Virtex family
- Multiplies N-bit wide variable A times M-bit wide variable B
- 2's complement Signed or Unsigned inputs
- Full precision outputs
- Supports pipelined or fully combinatorial construction
- Pipelined multipliers have registered inputs and outputs
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology

Functional Description

This multipliers in this library are high speed parallel implementations that multiply an N-bit wide variable by an M-bit variable and produce an N+M bit wide result.

An area-efficient, high-speed algorithm is used to give an efficient, tightly packed design. Each stage is pipelined for maximum performance.

The ability to halt each internal pipelined stage is provided through a clock enable control input. Partially completed results are stored internally when CE is pulled Low, and the multiplier resumes normal operation when CE returns to a High state.

Pinout and Instantiation Template

Port names are described in Table 1. Instantiation template examples for the Combinatorial and Pipelined multipliers are shown in Tables 2 and 3, respectively.

Table 1: Core Signal Pinout (n=N-1, m=M-1)

Signal	Signal Direction	Description
A[n:0]	Input	Parallel data in – A operand
B[m:0]	Input	Parallel data in – B operand
C (Pipelined only)	Input	Clock – Data inputs are captured, and new output data formed on rising clock transitions.
CE (Pipelined only)	Input	CLOCK ENABLE – When active high, allows data to move through internal pipeline stages. When inactive, all activity within the module ceases.
AR[n:0] (Pipelined with latency > 1 clock cycle only)	Output	Registered A operand
BR[m:0] (Pipelined with latency > 1 clock cycle only)	Output	Registered B operand
Y[m+n+1:0]	Output	Parallel data out – Product from multiply operation.

Table 2: Combinatorial multplier Instantiation template

VHDL Instantiation Template (.vhi)

```
component M1212SC is
   port map (
  A: in  std_logic_vector(11 downto 0);
  B: in  std_logic_vector(11 downto 0);
  PROD: out std_logic_vector(23 downto 0));
end component;
```

Verilog Instantiation Template (.vei)

```
module M1212SC (A,B,PROD);

input [11:0] A;
input [11:0] B;
output [23:0] PROD;

endmodule
```

Table 3: Registered multiplier Instantiation template

VHDL Instantiation Template (.vhi)

```
component M1212SR5 is
   port map (
  A: in  std_logic_vector(11 downto 0);
  B: in  std_logic_vector(11 downto 0);
  C: in std_logic;
  CE: in std_logic;
  AR: out  std_logic_vector(11 downto 0);
  BR: out  std_logic_vector(11 downto 0);
  PROD: out std_logic_vector(23 downto 0));
end component;
```

Verilog Instantiation Template (.vei)

```
module M1212SR5 (A,B,C,CE,AR,BR,PROD);

input [11:0] A;
input [11:0] B;
input C;
input CE;
output [11:0] AR;
output [11:0] BR;
output [23:0] PROD;
endmodule
```

Foundation users can generate a Foundation schematic symbol for a given multiplier by clicking on "Create macro symbol from netlist" under the "Hierarchy" menu of the Foundation schematic editor, The EDIF netlist for the appropriate multiplier should be specified as the input.

The archive also includes EDIF netlists with different bus delimiter formats to support Synopsys, Exemplar or Synplicity requirements. For Synopsys FPGA Express and FPGA Compiler, use the EDIF netlists found under the EDN_angle_brackets directory, and for Synplicity and Exemplar, use the EDIF netlists in the EDN_parenthesis directory.

Module naming convention

The naming convention for multipliers is as follows:

- Total name length is 7 to 8 characters:
  c1 c2 c3 c4 c5 c6 c7 c8
- All multipliers start with the letter M (c1 = M)
- The next two characters (c2 and c3) represent the number of bits for the "A" variable. Example: 08 = 8 bits wide
- The next two characters (c4 and c5) represent the number of bits for the "B" variable
- The next character is either S, U, M, for Signed by Signed, Unsigned by Unsigned, Mixed (either signed or unsigned dynamically) by Signed.
- The next character, c7, is either an "R" or a "C", for Registered or Combinatorial.
- The last character, c8 is blank for combinatorial multipliers. For non-combinatorial multipliers it represents the latency of the multiplier in clock cycles.

Example:

M1212SC: 12x12 signed by signed, combinatorial

M1212SR5: 12x12 signed by signed, 5 clock latency

M0808UR4: 8x8 unsigned by unsigned, 4 clock latency

Resource Utilization and Performance

Table 4 shows the resource utilization for each point solution.

Table 4: Characterization Data

Core Name	AxB	# of Slices	Latency	RPM Area (Rows x Columns)	Virtex-6 MHz/ns	Virtex-5 MHz/ns	Virtex-4 MHz/ns
M0808SR1	8x8	39	1	6 x 4	88 MHz	77 MHz	65 MHz
M0808SR4	8x8	48	4	6 x 4	184MHz	160 MHz	131 MHz
M0808UR4	8x8	48	4	6 x 4	184 MHz	160 MHz	131 MHz
M0812SR5	8x12	81	5	7 x 6	157 MHz	141 MHz	118 MHz
M0912SR1	9x12	46	1	8 x 6	63 MHz	55 MHz	46 MHz
M0920SR1	9x20	136	1	11 x 10	47 MHz	40 MHz	33 MHz
M1008SR1	10x8	46	1	7 x 4	84 MHz	73 MHz	61 MHz
M1010SR5	10x0	79	5	8 x 5	165 MHz	142 MHz	118 MHz
M1010UR5	10x10	79	5	8 x 5	165 MHz	142 MHz	118 MHz
M1212SC	12x12	82	0	9 x 6	58 MHz	51 MHz	42 MHz
M1212SR1	12x12	86	1	9 x 6	65 MHz	57 MHz	48 MHz
M1212SR5	12x12	107	5	9 x 6	167 MHz	143 MHz	117 MHz
M1410SC	14x10	76	0	10 x 5	58 MHz	51 MHz	42 MHz
M1412SR5	14x12	120	5	10 x 6	156 MHz	134 MHz	111 MHz
M1518SR6	15x18	203	6	13 x 9	133 MHz	115 MHz	95 MHz
M1616SC	16x16	143	0	12 x 8	53 MHz	46 MHz	38 MHz
M1616SR5	16x16	168	5	12 x 8	162 MHz	139 MHz	115 MHz
M1818SR6	18x18	222	6	14 x 9	126 MHz	107 MHz	87 MHz
M32UR12	32x32	974	13	30 x 26	156 MHz	134 MHz	111 MHz

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