May 19, 1998 (Version 2.1) Product Specification

XQ4000E/EX High-Reliability Features

- Certified to MIL-PRF-38535, appendix A QML (Qualified Manufacturers Listing)
- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 60 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per XQ4000E/EX output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Backward Compatible with XC4000 Devices
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Available Speed Grades:
  - XQ4000E -3 for plastic packages only
  - -4 for ceramic packages only
  - XQ4028EX -4 for all packages

More Information

For more information refer to Xilinx XC4000E and XC4000X series Field Programmable Gate Arrays product specification. This datasheet contains pinout tables for XQ4010E only. Refer to Xilinx 1998 Databook for pinout tables for other devices. (Pinouts for XQ4000E/EX are identical to XC4000E/EX.)

Table 1: XQ4000E/EX Field Programmable Gate Arrays

Device	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. Decode Inputs per side	Max. User I/O	Packages
XQ4005E	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112	PG156, CB164
XQ4010E	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160	PG191, CB196, HQ208
XQ4013E	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	72	192	PG223, CB228, HQ240
XQ4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	96	256	PG299, CB228
XQ4028EX	28,000	32,768	18,000 - 50,000	32 x 32	1024	2560	96	256	PG299, CB228, HQ240, BG352

Note: Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

XQ4000E/EX Switching Characteristics

XQ4000E/EX Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC overshoot or undershoot above Vcc or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XQ4000E/EX Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_C = -55°C to +125°C	Ceramic packages	4.5	5.5	V
V_{CC}	Supply voltage relative to GND, T_J = -55°C to +125°C	Plastic packages	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
T_{IN}	Input signal transition time			250	ns

Note 1: At case temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.

Note 2: Input and output Measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

Note 3: All specifications are subject to change without notice.

XQ4000E/EX DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min	TTL outputs	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)			50	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)			16	pF
I_{RIN*}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		-0.02	-0.25	mA
I_{RLL*}	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with the development system Tie option.
* Characterized Only.

XQ4000E Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)

		Speed Grade	-3*	-4**	
Description	**Symbol**	**Device**	**Max**	**Max**	**Units**
From pad through Primary buffer, to any clock K	T_{PG}	XQ4005E		7.0	ns
		XQ4010E	6.3	11.0	ns
		XQ4013E	6.8	11.5	ns
		XQ4025E		12.5	ns
From pad through Secondary buffer, to any clock K	T_{SG}	XQ4005E		7.5	ns
		XQ4010E	6.8	11.5	ns
		XQ4013E	7.3	12.0	ns
		XQ4025E		13.0	ns

* For plastic package options only.
** For ceramic package options only.

XQ4000E Horizontal Longline Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-3	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (LL):					
I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T_{IO1}	XQ4005E XQ4010E XQ4013E XQ4025E	 6.4 7.2 	5.0 8.0 9.0 11.0	ns ns ns ns
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T_{IO2}	XQ4005E XQ4010E XQ4013E XQ4025E	 6.9 7.7 	6.0 10.5 11.0 12.0	ns ns ns ns
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T_{ON}	XQ4005E XQ4010E XQ4013E XQ4025E	 7.3 7.5 	7.0 8.5 8.7 11.0	ns ns ns ns
T going High to TBUF going inactive, not driving LL	T_{OFF}	XQ4005E XQ4010E XQ4013E XQ4025E		1.8 3.0 3.5 4.0	ns ns ns ns
T going High to LL going from Low to High, pulled up by a single resistor. (Note 1)	T_{PUS}	XQ4005E XQ4010E XQ4013E XQ4025E	 22 26 	23.0 29.0 32.0 42.0	ns ns ns ns
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T_{PUF}	XQ4005E XQ4010E XQ4013E XQ4025E	 11 13 	10.0 13.5 15.0 18.0	ns ns ns ns

Note 1: These values include a minimum load. Use the static timing analyzer to determine the delay for each destination.

XQ4000E Wide Decoder Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-3	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XQ4005E		9.5	ns
		XQ4010E	9.0	15.0	ns
		XQ4013E	11.0	16.0	ns
		XQ4025E		18.0	ns
Full length, both pull-ups, inputs from internal logic	T_{WAFL}	XQ4005E		12.5	ns
		XQ4010E	11.0	18.0	ns
		XQ4013E	13.0	19.0	ns
		XQ4025E		21.0	ns
Half length, one pull-up, inputs from IOB I-pins	T_{WAO}	XQ4005E		10.5	ns
		XQ4010E	10.0	16.0	ns
		XQ4013E	12.0	17.0	ns
		XQ4025E		19.0	ns
Half length, one pull-up, inputs from internal logic	T_{WAOL}	XQ4005E		12.5	ns
		XQ4010E	12.0	18.0	ns
		XQ4013E	14.0	19.0	ns
		XQ4025E		21.0	ns

Note 1: These delays are specified from the decoder input to the decoder output.

Note 2: Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

XQ4000E CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

	Speed Grade	-3		-4		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	
Combinatorial Delays						
F/G inputs to X/Y outputs	T_{ILO}		3.1		3.9	ns
F/G inputs via H to X/Y outputs	T_{IHO}		5.5		5.9	ns
C inputs via H to X/Y outputs	T_{HH1O}		4.7		4.9	ns
CLB Fast Carry Logic						
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		2.6		4.4	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		4.4		6.8	ns
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.7		2.9	ns
CIN through function generators to X/Y outputs	T_{SUM}		4.4		5.0	ns
CIN to COUT, bypass function generators	T_{BYP}		0.7		1.0	ns
Sequential Delays						
Clock K to outputs Q	T_{CKO}				5.0	ns
Setup Time before Clock K						
F/G inputs	T_{ICK}	3.0		4.0		ns
F/G inputs via H	T_{IHCK}	4.6		6.1		ns
C inputs via H1 through H	T_{HH1CK}	4.1		5.0		ns
C inputs via H2 through H	T_{HH2CK}	3.8		4.8		ns
C inputs via DIN	T_{DICK}	2.4		3.0		ns
C inputs via EC	T_{ECCK}	3.0		4.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	4.0		4.2		ns

XQ4000E CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the static timing analyzer and used in the simulator.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XQ4000E/EX devices unless otherwise noted.

		Speed Grade	-3		-4		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	
Hold Time after Clock K							
F/G inputs	T_{CKI}		0		0		ns
F/G inputs via H	T_{CKIH}		0		0		ns
C inputs via H1 through H	T_{CKHH1}		0		0		ns
C inputs via DIN	T_{CKDI}		0		0		ns
C inputs via EC	T_{CKEC}		0		0		ns
C inputs via SR, going Low (inactive)	T_{CKR}		0		0		ns
Clock							
Clock High time	T_{CH}		4.0		4.5		ns
Clock Low time	T_{CL}		4.0		4.5		ns
Set/Reset Direct							
Width (High)	T_{RPW}		4.0		5.5		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		4.0			6.5	ns
Master Set/Reset							
Width (High or Low)	T_{MRW}	4005E			13.0		ns
		4010E	11.5		55.0		ns
		4013E	11.5		70.0		ns
		4025E			112.0		ns
Delay from Global Set/Reset net to Q	T_{MRQ}	4005E				23.0	ns
		4010E		18.7		60.0	ns
		4013E		18.7		77.0	ns
		4025E				134.0	ns

XQ4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

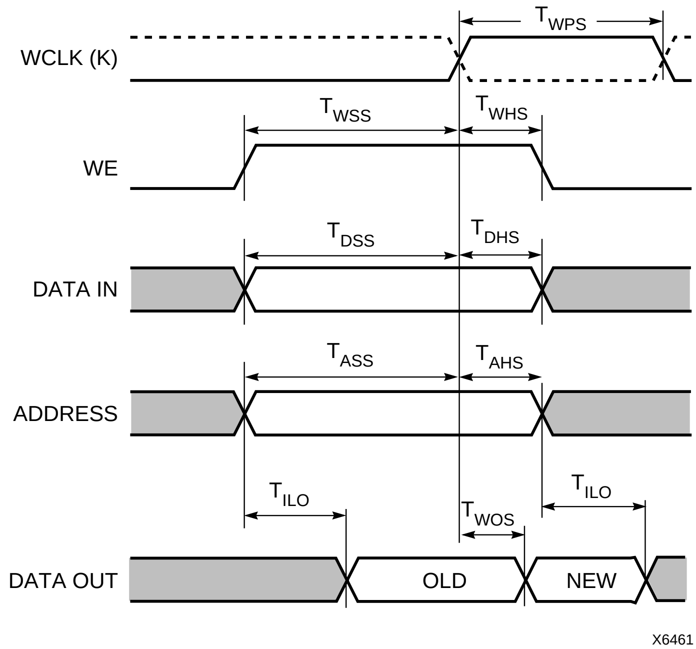
Single Port RAM	Speed Grade		-3		-4		Units
	Size	Symbol	Min	Max	Min	Max	
Write Operation							
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	14.4 14.4		15.0 15.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	7.2 7.2		7.5 7.5	1 ms 1 ms	ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	2.4 2.4		2.8 2.8		ns ns
Address hold time after clock K	16x2 32x1	T_{AHS} T_{AHTS}	0 0		0 0		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	3.2 1.9		3.5 2.5		ns ns
DIN hold time after clock K	16x2 32x1	T_{DHS} T_{DHTS}	0 0		0 0		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	2.0 2.0		2.2 2.2		ns ns
WE hold time after clock K	16x2 32x1	T_{WHS} T_{WHTS}	0 0		0 0		ns ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}	8.8 10.3			10.3 11.6	ns ns

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

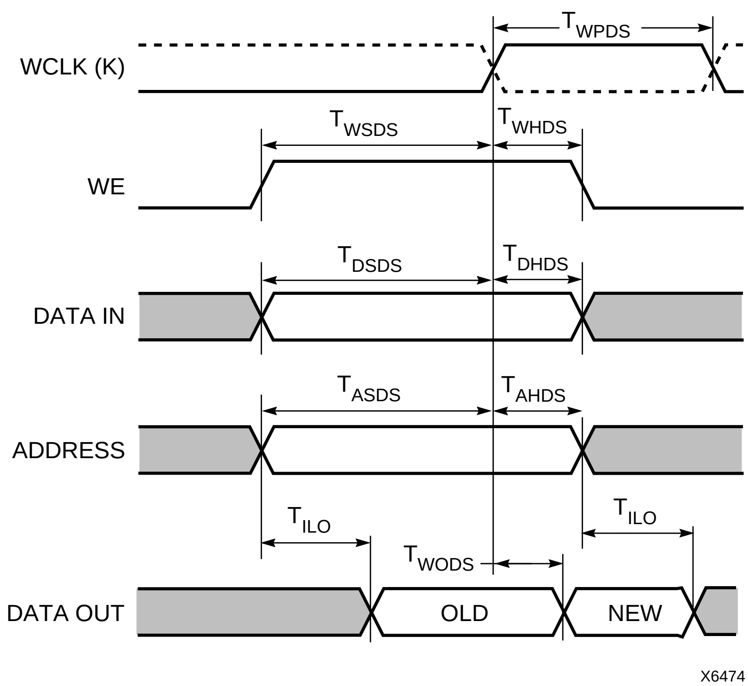
Dual-Port RAM	Speed Grade		-3		-4		Units
	Size	Symbol	Min	Max	Min	Max	
Write Operation							
Address write cycle time (clock K period)	16x1	T_{WCDS}	14.4		15.0		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	7.2		7.5	1 ms	ns
Address setup time before clock K	16x1	T_{ASDS}	2.5		2.8		ns
Address hold time after clock K	16x1	T_{AHDS}	0		0		ns
DIN setup time before clock K	16x1	T_{DSDS}	1.9		2.2		ns
DIN hold time after clock K	16x1	T_{DHDS}	0		0		ns
WE setup time before clock K	16x1	T_{WSDS}	2.0		2.2		ns
WE hold time after clock K	16x1	T_{WHDS}	0		0.3		ns
Data valid after clock K	16x1	T_{WODS}		7.8		10.0	ns

Note 1: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

XQ4000E CLB RAM Synchronous (Edge-Triggered) Write Timing



XQ4000E CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



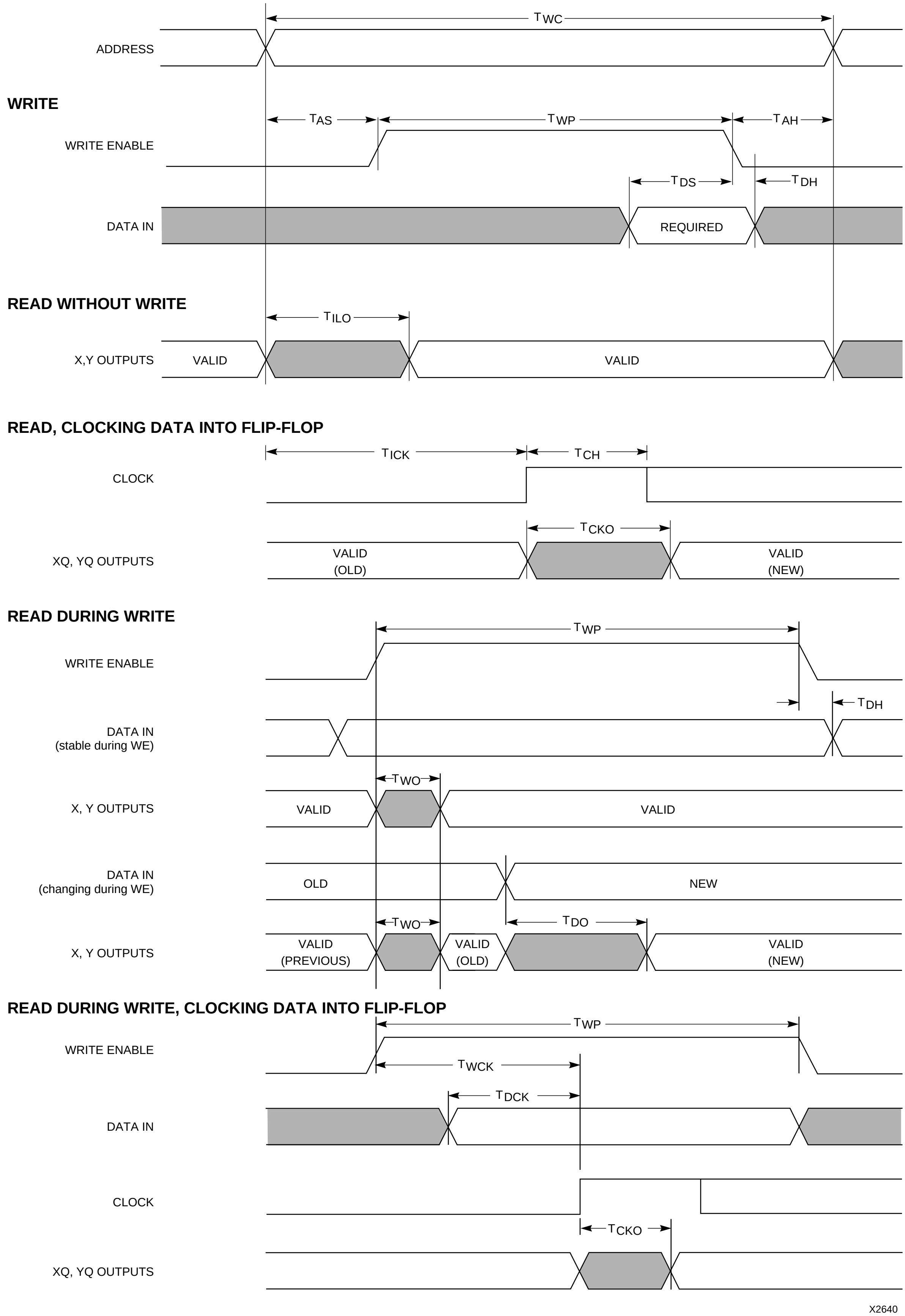
XQ4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

		Speed Grade	-3		-4		Units
Description	**Size**	**Symbol**	**Min**	**Max**		**Max**	
Write Operation							
Address write cycle time	16x2 32x1	T_{WC} T_{WCT}	8.0 8.0		8.0 8.0		ns ns
Write Enable pulse width (High)	16x2 32x1	T_{WP} T_{WPT}	4.0 4.0		4.0 4.0		ns ns
Address setup time before WE	16x2 32x1	T_{AS} T_{AST}	2.0 2.0		2.0 2.0		ns ns
Address hold time after end of WE	16x2 32x1	T_{AH} T_{AHT}	2.0 2.0		2.5 2.0		ns ns
DIN setup time before end of WE	16x2 32x1	T_{DS} T_{DST}	2.2 2.2		4.0 5.0		ns ns
DIN hold time after end of WE	16x2 32x1	T_{DH} T_{DHT}	2.0 2.0		2.0 2.0		ns ns
Read Operation							
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	3.1 5.5		4.5 6.5		ns ns
Data valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		3.1 5.5		3.9 5.9	ns ns
Read Operation, Clocking Data into Flip-Flop							
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	3.0 4.6		4.0 6.1		ns ns
Read During Write							
Data valid after WE goes active (DIN stable before WE)	16x2 32x1	T_{WO} T_{WOT}		6.0 7.3		10.0 12.0	ns ns
Data valid after DIN (DIN changes during WE)	16x2 32x1	T_{DO} T_{DOT}		6.6 7.6		9.0 11.0	ns ns
Read During Write, Clocking Data into Flip-Flop							
WE setup time before clock K	16x2 32x1	T_{WCK} T_{WCKT}	6.0 6.8		8.0 9.6		ns ns
Data setup time before clock K	16x2 32x1	T_{DCK} T_{DCKT}	5.2 6.2		7.0 8.0		ns ns

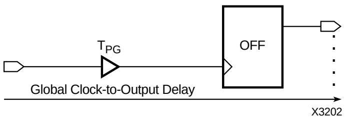
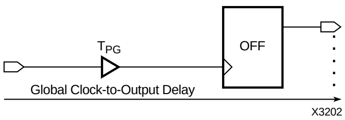
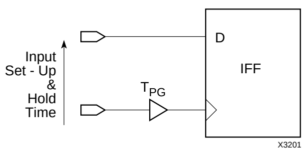
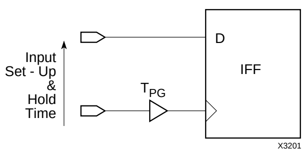
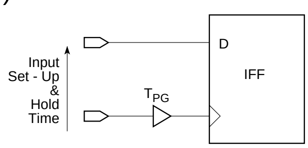
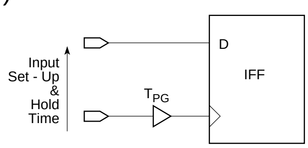
Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XQ4000E CLB Level-Sensitive RAM Timing Characteristics



XQ4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000E/EX devices unless otherwise noted.

		Speed Grade	-3	-4	Units
Description	**Symbol**	**Device**			
Global Clock to Output (fast) using OFF 	T_{ICKOF}	XQ4005E		14.0	ns
		XQ4010E	10.9	16.0	ns
		XQ4013E	11.0	16.5	ns
	(Max)	XQ4025E		17.0	ns
Global Clock to Output (slew-limited) using OFF 	T_{ICKO}	XQ4005E		18.0	ns
		XQ4010E	14.9	20.0	ns
		XQ4013E	15.0	20.5	ns
	(Max)	XQ4025E		21.0	ns
Input Setup Time, using IFF (no delay) 	T_{PSUF}	XQ4005E		2.0	ns
		XQ4010E	0.2	1.9	ns
		XQ4013E	0	1.6	ns
	(Min)	XQ4025E		1.5	ns
Input Hold Time, using IFF (no delay) 	T_{PHF}	XQ4005E		4.6	ns
		XQ4010E	5.5	6.0	ns
		XQ4013E	6.5	7.0	ns
	(Min)	XQ4025E		8.0	ns
Input Setup Time, using IFF (with delay) 	T_{PSU}	XQ4005E		8.5	ns
		XQ4010E	7.0	8.5	ns
		XQ4013E	7.0	8.5	ns
	(Min)	XQ4025E		9.5	ns
					ns
					ns
					ns
					ns
Input Hold Time, using IFF (with delay) 	T_{PH}	XQ4005E		0	ns
		XQ4010E	0	0	ns
		XQ4013E	0	0	ns
	(Min)	XQ4025E		0	ns

OFF = Output Flip-Flop IFF = Input Flip-Flop or Latch

XQ4000E IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000E/EX devices unless otherwise noted.

		Speed Grade	-3		-4		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays (TTL Inputs)							
Pad to I1, I2	T_{PID}	All devices		2.5		3.0	ns
Pad to I1, I2 via transparent latch, no delay	T_{PLI}	All devices				6.0	ns
with delay	T_{PDLI}	XQ4005E				12.0	ns
		XQ4010E		10.8		12.2	ns
		XQ4013E		11.2		12.6	ns
		XQ4025E				15.0	ns
Propagation Delays							
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		2.8		6.8	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices		4.0		7.3	ns
Hold Times (Note 1)							
Pad to Clock (IK), no delay	T_{IKPI}	All devices	0		0		ns
with delay	T_{IKPID}	All devices	0		0		ns

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XQ4000E IOB Input Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

		Speed Grade	**-3**		**-4**		**Units**
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	
Setup Times (TTL Inputs)							
Pad to Clock (IK), no delay	T_{PICK}	All devices	2.6		4.0		ns
with delay	T_{PICKD}	XQ4005E			10.9		ns
		XQ4010E	9.8		11.3		ns
		XQ4013E	10.2		11.8		ns
		XQ4025E			14.0		ns
							ns
							ns
							ns
							ns
(TTL or CMOS)							
Clock Enable (EC) to Clock (IK), no delay							
with delay	T_{ECIK}	All devices	2.5		3.5		ns
	T_{ECIKD}	XQ4005E			10.4		ns
		XQ4010E	9.7		10.7		ns
		XQ4013E	10.1		11.1		ns
		XQ4025E			14.0		ns
Global Set/Reset (Note 3)							
Delay from GSR net through Q to I1, I2	T_{RRI}	XQ4005E				12.0	ns
GSR width		XQ4010E		7.8		21.0	ns
GSR inactive to first active Clock (IK) edge		XQ4013E		7.8		23.0	ns
		XQ4025E				29.0	ns
	T_{MRW}	XQ4005E			13.0		ns
		XQ4010E		11.5	55.0		ns
		XQ4013E		11.5	70.0		ns
		XQ4025E			112.0		ns
	T_{RPO}	XQ4005E				15.0	ns
		XQ4010E		11.8		20.3	ns
		XQ4013E		11.8		22.0	ns
		XQ4025E				28.0	ns

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.
Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.
Note 3: Timing is based on the XQ4005E. For other devices see the static timing analyzer.

XQ4000E IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

	Speed Grade	**-3**		**-4**		**Units**
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays (TTL Output Levels)						
Clock (OK) to Pad, fast	T_{OKPOF}		6.5		7.5	ns
slew-rate limited	T_{OKPOS}		9.5		11.5	ns
Output (O) to Pad, fast	T_{OPF}		5.5		8.0	ns
slew-rate limited	T_{OPS}		8.6		12.0	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		4.2		10.0	ns
3-state to Pad active						
and valid, fast	T_{TSONF}		8.1		10.0	ns
slew-rate limited	T_{TSONS}		11.1		13.7	ns

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XQ4000 Data” section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XQ4000E IOB Output Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XQ4000E/EX devices unless otherwise noted.

		Speed Grade	-3		-4		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	
Setup and Hold							
Output (O) to clock (OK) setup time	T_{OOK}		4.6		5.0		ns
Output (O) to clock (OK) hold time	T_{OKO}		0		0		ns
Clock							
Clock High	T_{CH}		4.0		4.5		ns
Clock Low	T_{CL}		4.0		4.5		ns

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XQ4000 Data” section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XQ4005E. For other devices see the static timing analyzer.

XQ4028EX Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

All specifications subject to change without notice.

XQ4028EX Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
V_{CCt}	Longest Supply Voltage Rise Time from 1 V to 4 V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC overshoot or undershoot above V_{cc} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XQ4028EX Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_C = -55 °C to +125°C	Ceramic Packages	4.5	5.5	V
	Supply voltage relative to GND, T_J = -55°C to +125°C	Plastic Packages	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

Note 2: Input and output measurement thresholds for TTL are 1.5 V. Input and output measurement thresholds for CMOS are 2.5 V.

Note 3: All timing parameters are specified for Commercial temperature range only.

XQ4028EX DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0 mA	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
V_{DR}	Data Retention Supply Voltage (below which configuration data may be lost)		3.0		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			25	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	Plastic packages		10	pF
		Ceramic packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 5.5 V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND.

XQ4028EX Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

	Speed Grade	-4	Units
Description	Symbol	Max	
From pad through Global Low Skew buffer, to any clock K	T_{GLS}	9.2	ns
From pad through Global Early buffer, to any clock K in same quadrant	T_{GE}	5.7	ns

XQ4028EX Longline and Wide Decoder Timing Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted. Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

XQ4028EX Horizontal Longline Switching Characteristic Guidelines

Speed Grade		-4	Units
Description	**Symbol**	**Max**	
TBUF driving a Horizontal Longline			
I going High or Low to Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T_{IO1}	13.7	ns
T going Low to Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T_{ON}	14.7	ns
T going High to Horizontal Longline going from Low to High, pulled up by two resistors. (Note 1)	T_{PU2}		ns ns
TBUF driving Half a Horizontal Longline			
I going High or Low to half of a Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T_{HIO1}	6.3	ns
T going Low to half of a Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T_{HON}	7.2	ns
T going High to half of a Horizontal Longline going from Low to High, pulled up by four resistors. (Note 1)	T_{HPU4}		ns

Note 1: These values include a minimum load of one output, spaced as far as possible from the activated pullup(s). Use the static timing analyzer to determine the delay for each destination.

XQ4028EX Wide Decoder Switching Characteristic Guidelines

Speed Grade		-4	Units
Description	**Symbol**	**Max**	
Full length, two pull-ups, inputs from IOB I-pins	T_{WAF2}		ns ns
Full length, two pull-ups, inputs from internal logic	T_{WAF2L}		ns ns
Half length, two pull-ups, inputs from IOB I-pins	T_{WAO2}		ns ns
Half length, two pull-ups, inputs from internal logic	T_{WAO2L}		ns ns

Note 1: These delays are specified from the decoder input to the decoder output.

XQ4028EX CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

	Speed Grade	-4		Units
Description	**Symbol**	**Min**	**Max**	
Combinatorial Delays				
F/G inputs to X/Y outputs	T_{ILO}		2.2	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		3.8	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		3.2	ns
C inputs via SR/H0 via H' to X/Y outputs	T_{HH0O}		3.6	ns
C inputs via H1 via H' to X/Y outputs	T_{HH1O}		3.0	ns
C inputs via DIN/H2 via H' to X/Y outputs	T_{HH2O}		3.6	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T_{CBYP}		2.0	ns
CLB Fast Carry Logic				
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		2.5	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		4.1	ns
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.9	ns
CIN through function generators to X/Y outputs	T_{SUM}		3.0	ns
C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		0.60	ns
Carry Net Delay, C_{OUT} to C_{IN}	T_{NET}		0.18	ns
Sequential Delays				
Clock K to Flip-Flop outputs Q	T_{CKO}		2.2	ns
Clock K to Latch outputs Q	T_{CKLO}		2.2	ns
Setup Time before Clock K				
F/G inputs	T_{ICK}	1.3		ns
F/G inputs via H'	T_{IHCK}	3.0		ns
C inputs via H0 through H'	T_{HH0CK}	2.8		ns
C inputs via H1 through H'	T_{HH1CK}	2.2		ns
C inputs via H2 through H'	T_{HH2CK}	2.8		ns
C inputs via DIN	T_{DICK}	1.2		ns
C inputs via EC	T_{ECCK}	1.2		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.8		ns
CIN input via F'/G'	T_{CCK}	2.2		ns
CIN input via F'/G' and H'	T_{CHCK}	3.9		ns
Hold Time after Clock K				
F/G inputs	T_{CKI}	0		ns
F/G inputs via H'	T_{CKIH}	0		ns
C inputs via SR/H0 through H'	T_{CKHH0}	0		ns
C inputs via H1 through H'	T_{CKHH1}	0		ns
C inputs via DIN/H2 through H'	T_{CKHH2}	0		ns
C inputs via DIN/H2	T_{CKDI}	0		ns
C inputs via EC	T_{CKEC}	0		ns
C inputs via SR, going Low (inactive)	T_{CKR}	0		ns
Clock				
Clock High time	T_{CH}	3.5		ns
Clock Low time	T_{CL}	3.5		ns
Set/Reset Direct				
Width (High)	T_{RPW}	3.5		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		4.5	ns

Description	Symbol	-4 Min	-4 Max	Units
	Speed Grade	-4		Units
Global Set/Reset				
Minimum GSR Pulse Width	T_{MRW}		13.0	ns
Delay from GSR input to any Q (XQ4028EX)	T_{MRQ}		22.8	ns
Delay from GSR input to any Q (XQ4036EX)	T_{MRQ}		24.0	ns
Toggle Frequency) (for export control purposes)	F_{TOG}		143	MHz

XQ4028EX CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

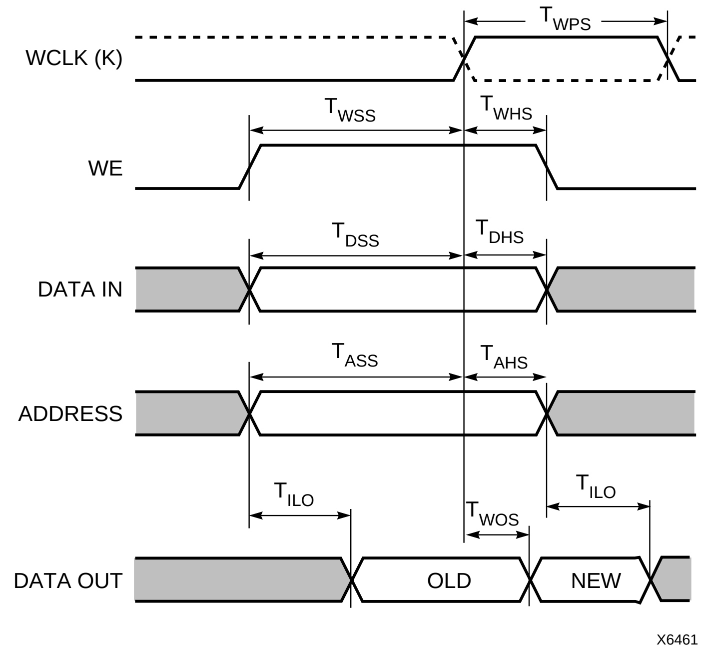
Single Port RAM	Speed Grade		-4		Units
	Size	Symbol	Min	Max	
Write Operation					
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	11.0 11.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	5.5 5.5		ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	2.7 2.6		ns ns
Address hold time after clock K	16x2 32x1	T_{AHS} T_{AHTS}	0 0		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	2.4 2.9		ns ns
DIN hold time after clock K	16x2 32x1	T_{DHS} T_{DHTS}	0 0		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	2.3 2.1		ns ns
WE hold time after clock K	16x2 32x1	T_{WHS} T_{WHTS}	0 0		ns ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}		8.2 10.1	ns ns

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

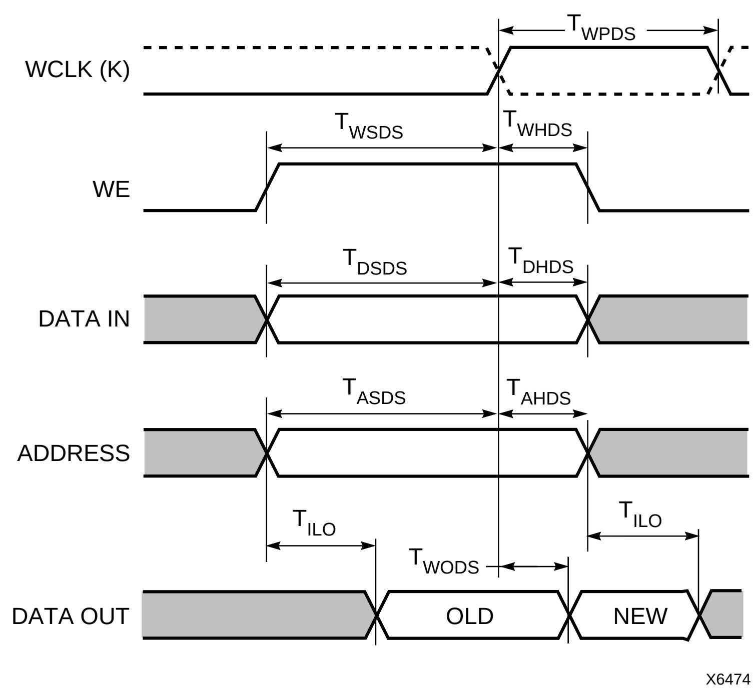
Dual-Port RAM	Speed Grade		-4		Units
	Size	Symbol	Min	Max	
Write Operation					
Address write cycle time (clock K period)	16x1	T_{WCDS}	11.0		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	5.5		ns
Address setup time before clock K	16x1	T_{ASDS}	3.1		ns
Address hold time after clock K	16x1	T_{AHDS}	0		ns
DIN setup time before clock K	16x1	T_{DSDS}	2.9		ns
DIN hold time after clock K	16x1	T_{DHDS}	0		ns
WE setup time before clock K	16x1	T_{WSDS}	2.1		ns
WE hold time after clock K	16x1	T_{WHDS}	0		ns
Data valid after clock K	16x1	T_{WODS}		9.4	ns

Note 1: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

XQ4000EX CLB RAM Synchronous (Edge-Triggered) Write Timing



XQ4000EX CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



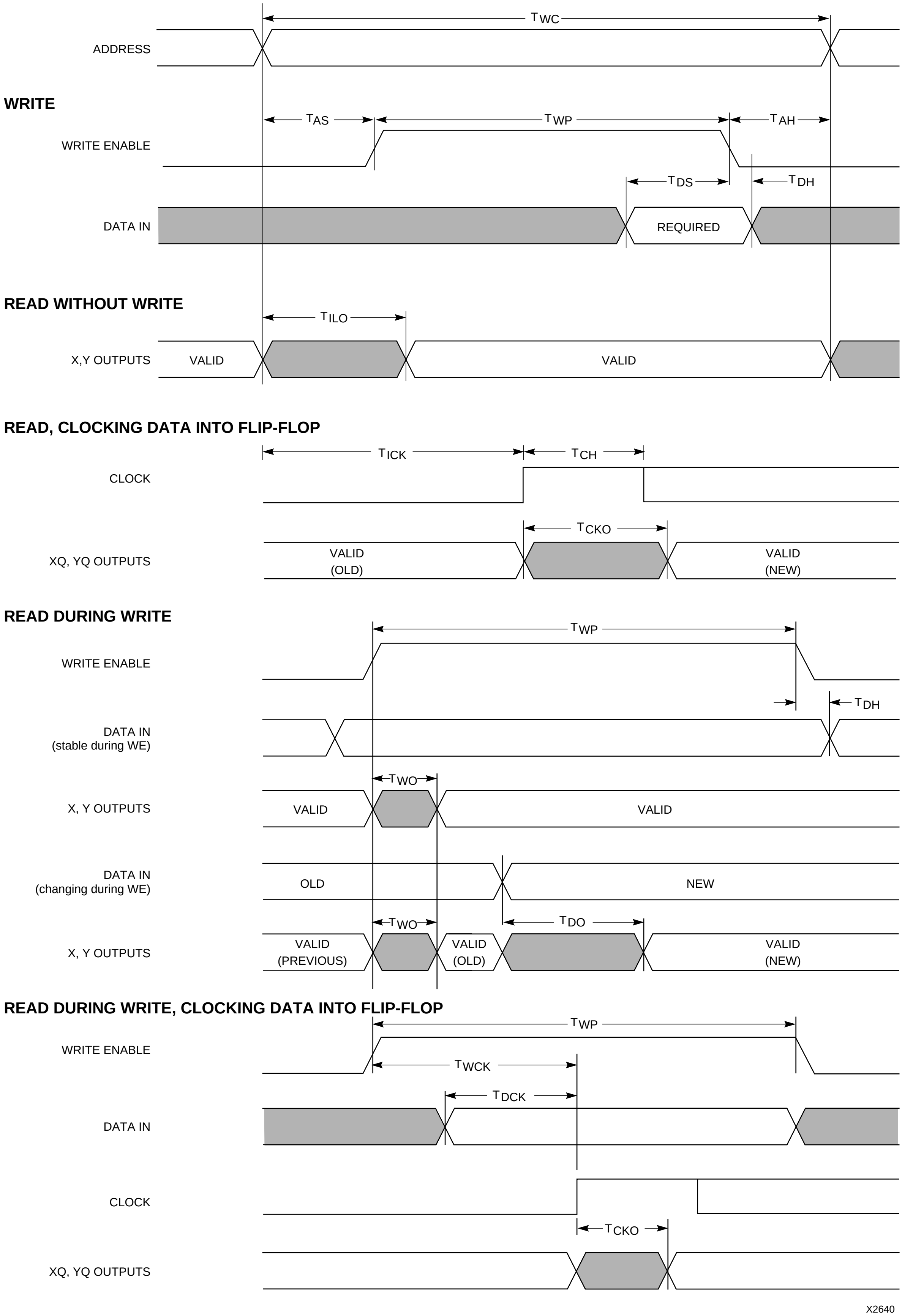
XQ4028EX CLB RAM Asynchronous (Level-Sensitive) Write and Read Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

		Speed Grade	-4		Units
Description	**Size**	**Symbol**	**Min**	**Max**	
Write Operation					
Address write cycle time	16x2 32x1	T_{WC} T_{WCT}	10.6 10.6		ns ns
Write Enable pulse width (High)	16x2 32x1	T_{WP} T_{WPT}	5.3 5.3		ns ns
Address setup time before WE	16x2 32x1	T_{AS} T_{AST}	2.8 2.9		ns ns
Address hold time after end of WE	16x2 32x1	T_{AH} T_{AHT}	1.7 1.7		ns ns
DIN setup time before end of WE	16x2 32x1	T_{DS} T_{DST}	1.1 1.1		ns ns
DIN hold time after end of WE	16x2 32x1	T_{DH} T_{DHT}	6.6 6.6		ns ns
Read Operation					
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	4.5 6.5		ns ns
Data valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		2.2 3.8	ns ns
Read Operation, Clocking Data into Flip-Flop					
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	1.5 3.2		ns ns
Read During Write					
Data valid after WE goes active (DIN stable before WE)	16x2 32x1	T_{WO} T_{WOT}		6.5 7.4	ns ns
Data valid after DIN (DIN changes during WE)	16x2 32x1	T_{DO} T_{DOT}		7.7 8.2	ns ns
Read During Write, Clocking Data into Flip-Flop					
WE setup time before clock K	16x2 32x1	T_{WCK} T_{WCKT}	7.1 9.2		ns ns
Data setup time before clock K	16x2 32x1	T_{DCK} T_{DCKT}	5.9 8.4		ns ns

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XQ4028EXX CLB RAM Asynchronous (Level-Sensitive) Timing Characteristics



XQ4028EX Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000EX devices unless otherwise noted.

XQ4028EX Output Flip-Flop, Clock to Out

	Speed Grade	-4	Units
Description	**Symbol**	**Max**	
Global Low Skew Clock to TTL Output (fast) using OFF	T_{ICKOF}	16.6	ns
Global Early Clock to TTL Output (fast) using OFF	T_{ICKEOF}	13.1	ns

OFF = Output Flip Flop

XQ4028EX Output MUX, Clock to Out

	Speed Grade	-4	Units
Description	**Symbol**	**Max**	
Global Low Skew Clock to TTL Output (fast) using OMUX	T_{PFPF}	15.9	ns
Global Early Clock to TTL Output (fast) using OMUX	T_{PEFPF}	12.4	ns

OMUX = Output MUX

Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Note 2: Output timing is measured at TTL threshold with 50 pF external capacitive load.
Note 3: Set-up time is measured with the fastest route and the lightest load. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

XQ4028EX Output Level and Slew Rate Adjustments

The following table must be used to adjust output parameters and output switching characteristics.

	Speed Grade	-4	Units
Description	**Symbol**	**Max**	
For TTL output FAST add	T_{TTLOF}	0	ns
For TTL output SLOW add	T_{TTLO}	2.9	ns
For CMOS FAST output add	T_{CMOSOF}	1.0	ns
For CMOS SLOW output add	T_{CMOSO}	3.6	ns

XQ4028EX Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000EX devices unless otherwise noted

XQ4028EX Global Low Skew Clock, Set-Up and Hold

	Speed Grade	-4	Units
Description	**Symbol**	**Min**	
Input Setup Time, using Global Low Skew clock and IFF (full delay)	T_{PSD}	8.0	ns
Input Hold Time, using Global Low Skew clock and IFF (full delay)	T_{PHD}	0	ns

IFF = Flip-Flop or Latch

XQ4028EX Global Early Clock, Set-Up and Hold for IFF

	Speed Grade	-4	Units
Description	**Symbol**	**Min**	
Input Setup Time, using Global Early clock and IFF (partial delay)	T_{PSEP}	6.5	ns
Input Hold Time, using Global Early clock and IFF (partial delay)	T_{PHEP}	0	ns

IFF = Flip-Flop or Latch

Note 1: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.6 ns for BUFGE #s 1, 2, 5 and 6.

XQ4028EX Global Early Clock, Set-Up and Hold for FCL

	Speed Grade	-4	Units
Description	**Symbol**	**Min**	
Input Setup Time, using Global Early clock and FCL (partial delay)	T_{PFSEP}	3.4	ns
Input Hold Time, using Global Early clock and FCL (partial delay)	T_{PFHEP}	0	ns

FCL = Fast Capture Latch

Note 1: For CMOS input levels, see the “XQ4028EX Input Threshold Adjustments” on page 27.
Set-up time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time
Note 2: Under given design conditions. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.
Note 3: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.2 ns for BUFGE #s 1, 2, 5 and 6.

XQ4028EX Input Threshold Adjustments

The following table must be used to adjust input parameters and input switching characteristics.

	Speed Grade	-4	Units
Description	**Symbol**	**Max**	
For TTL input add	T_{TTLI}	0	ns
For CMOS input add	T_{CMOSI}	0.3	ns

XQ4028EX IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

	Speed Grade	-4	Units
Description	**Symbol**	**Min**	
Clocks			
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	3.2	ns
Propagation Delays		**Max**	
Pad to I1, I2	T_{PID}	2.2	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	3.8	ns
Pad to I1, I2 via transparent input latch, partial delay	T_{PPLI}	13.3	ns
Pad to I1, I2 via transparent input latch, full delay	T_{PDLI}	18.2	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}	5.3	ns
Pad to I1, I2 via transparent FCL and input latch, partial delay	T_{PPFLI}	13.6	ns
Propagation Delays			
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	3.0	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	3.2	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{OKLI}	6.2	ns
Global Set/Reset			
Minimum GSR Pulse Width	T_{MRW}	13.0	ns
Delay from GSR input to any Q	T_{RRI}	22.8	ns

FCL = Fast Capture Latch, IFF = Input Flip-Flop or Latch

Note 1: For CMOS input levels, see the “XQ4028EX Input Threshold Adjustments” on page 27.

Note 2: For set-up and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page 27.

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XQ4028EX IOB Input Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

	Speed Grade	-4	Units
Description	**Symbol**	**Min**	
Setup Times			
Pad to Clock (IK), no delay	T_{PICK}	2.5	ns
Pad to Clock (IK), partial delay	T_{PICKP}	10.8	ns
Pad to Clock (IK), full delay	T_{PICKD}	15.7	ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	3.9	ns
Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	T_{PICKFP}	12.3	ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	0.8	ns
Pad to Fast Capture Latch Enable (OK), partial delay	T_{POCKP}	9.1	ns
Setup Times (TTL or CMOS Inputs)			
Clock Enable (EC) to Clock (IK)	T_{ECIK}	0.3	ns
Hold Times			
Pad to Clock (IK),			
no delay	T_{IKPI}	0	ns
partial delay	T_{IKPIP}	0	ns
full delay	T_{IKPID}	0	ns
Pad to Clock (IK) via transparent Fast Capture Latch,			
no delay	T_{IKFPI}	0	ns
partial delay	T_{IKFPIP}	0	ns
full delay	T_{IKFPID}	0	ns
Clock Enable (EC) to Clock (IK),			
no delay	T_{IKEC}	0	ns
partial delay	T_{IKECP}	0	ns
full delay	T_{IKECD}	0	ns
Pad to Fast Capture Latch Enable (OK),			
no delay	T_{OKPI}	0	ns
partial delay	T_{OKPIP}	0	ns

Note 1: For CMOS input levels, see the “XQ4028EX Input Threshold Adjustments” on page 27.
Note 2: For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page 27.

XQ4028EX IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XQ4000EX devices unless otherwise noted.

	Speed Grade	-4			Units
Description	**Symbol**	**Min**	**Max**	**Max**	
Propagation Delays					
Clock (OK) to Pad	T_{OKPOF}		7.4	6.0	ns
Output (O) to Pad	T_{OPF}		6.2	5.0	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		4.9	4.1	ns
3-state to Pad active and valid	T_{TSONF}		6.2	5.0	ns
Output MUX Select (OK) to Pad	T_{OKFPF}		6.7	5.4	ns
Fast Path Output MUX Input (EC) to Pad	T_{CEFPF}		6.2	5.0	ns
Slowest Path Output MUX Input (O) to Pad	T_{OFPF}		7.3	5.9	ns
Setup and Hold Times					
Output (O) to clock (OK) setup time	T_{OOK}	0.6			ns
Output (O) to clock (OK) hold time	T_{OKO}	0			ns
Clock Enable (EC) to clock (OK) setup	T_{ECOK}	0			ns
Clock Enable (EC) to clock (OK) hold	T_{OKEC}	0			ns
Clock					
Clock High	T_{CH}	3.5			ns
Clock Low	T_{CL}	3.5			ns
Global Set/Reset					
Minimum GSR pulse width	T_{MRW}	13.0			ns
Delay from GSR input to any Pad (XQ4028EX)	T_{RPO}	30.2			ns
Delay from GSR input to any Pad (XQ4036EX)	T_{RPO}	31.4			ns

Note 1: Output timing is measured at TTL threshold, with 35pF external capacitive loads.
Note 2: For CMOS output levels, see the “XQ4028EX Output Level and Slew Rate Adjustments” on page 26.

CB191/196 Package for XQ4010E

Pin Description	PG191	CB196	Bound Scan
GND	D4	P1	-
PGCK1_(A16*I/0)	C3	P2	122
I/O_(A17)	C4	P3	125
I/0	B3	P4	128
-	-	P5*	-
I/O	C5	P6	131
I/O_(TDI)	A2	P7	134
I/O_(TCK)	B4	P8	137
I/O	C6	P9	140
I/O	A3	P10	143
I/O	B5	P11	146
I/O	B6	P12	149
GND	C7	P13	-
I/O	A4	P14	152
I/O	A5	P15	155
I/O_(TMS)	B7	P16	158
I/O	A6	P17	161
I/O	C8	P18	164
I/O	A7	P19	167
I/O	B8	P20	170
I/O	A8	P21	173
I/O	B9	P22	176
I/O	C9	P23	179
GND	D9	P24	-
VCC	D10	P25	-
I/O	C10	P26	182
I/O	B10	P27	185
I/O	A9	P28	-
I/O	A10	P29	191
I/O	A11	P30	194
I/O	C11	P31	197
I/O	B11	P32	200
I/O	A12	P33	203
I/O	B12	P34	206
I/O	A13	P35	209
GND	C12	P36	-
I/O	B13	P37	212
I/O	A14	P38	215
I/O	A15	P39	218
I/O	C13	P40	221

* Indicates unconnected package pins.
** Contributes only one bit (.I) to the boundary scan register.
Boundary Scan BIt 0 = TD0.T
Boundary Scan Bit 1 = TD0.0
Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O	B14	P41	224
I/O	A16	P42	227
I/O	B15	P43	230
I/O	C14	P44	233
I/O	A17	P45	236
SCGK2_(I/O)	B16	P46	239
M1	C15	P47	242
GND	D15	P48	
M0	A18	P49	245**
VCC	D16	P50	-
M2	C16	P51	246**
PGCK2_(I/O)	B17	P52	247
I/O_(HDC)	E16	P53	250
-	-	P54*	-
I/O	C17	P55	253
I/0	D17	P56	256
I/O	B18	P57	259
I/O_(LDC)	E17	P58	262
I/O	F16	P59	265
I/O	C18	P60	268
I/O	D18	P61	271
I/O	F17	P62	274
GND	G16	P63	-
I/O	E18	P64	277
I/O	F18	P65	280
I/O	G17	P66	283
I/O	G18	P67	286
I/O	H16	P68	286
I/O	H17	P69	291
I/O	H18	P70	295
I/O	J18	P71	298
I/O	J17	P72	301
I/O_(/ERR_/INIT)	J16	P73	304
VCC	J15	P74	-
GND	K15	P75	-
I/O	K16	P76	307
I/O	K17	P77	310
I/O	K18	P78	313
I/O	L18	P79	316
I/O	L17	P80	319
I/O	L16	P81	322

* Indicates unconnected package pins.
** Contributes only one bit (.I) to the boundary scan register.
Boundary Scan BIt 0 = TD0.T
Boundary Scan Bit 1 = TD0.0
Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O	M18	P82	325
I/O	M17	P83	328
I/O	N18	P84	331
I/O	P18	P85	334
GND	M16	P86	-
I/O	N17	P87	337
I/O	R18	P88	340
I/O	T18	P89	343
I/O	P17	P90	349
I/O	N16	P91	349
I/O	T17	P92	352
I/O	R17	P93	355
I/O	P16	P94	358
I/O	U18	P95	361
SGCK3_(I/O)	T16	P96	364
GND	R16	P97	-
DONE	U17	P98	-
VCC	R15	P99	-
/PROG	V18	P100	-
I/O_(D7)	T15	P101	367
PGCK3_(I/O)	U16	P102	370
-	-	P103*	-
I/O	T14	P104	376
I/O	U15	P105	376
I/O_(D6)	V17	P106	379
I/O	V16	P107	382
I/O	T13	P108	385
I/O	U14	P109	388
I/O	V15	P110	391
I/O	V14	P111	394
GND	T12	P112	-
I/O	U13	P113	397
I/O	V13	P114	400
I/O_(D5)	U12	P115	403
I/O_(/CSO)	V12	P116	406
I/O	T11	P117	409
I/O	U11	P118	412
I/O	V11	P119	415
I/O	V1	P120	418
I/O_(D4)	U10	P121	421
I/O	T10	P122	424

* Indicates unconnected package pins.
** Contributes only one bit (.I) to the boundary scan register.
Boundary Scan BIt 0 = TD0.T
Boundary Scan Bit 1 = TD0.0
Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
VCC	R10	P123	-
GND	R9	P124	-
I/O_(D3)	T9	P125	427
I/O_(/RS)	U9	P126	430
I/O	V9	P127	433
I/O	V8	P128	436
I/O	U8	P129	439
I/O	T8	P130	442
I/O_(D2)	V7	P131	445
I/O	U7	P132	448
I/O	V6	P133	451
I/O	U6	P134	454
GND	T7	P135	-
I/O	V5	P136	457
I/O	V4	P137	460
I/O	U5	P138	463
I/O	T6	T139	446
I/O_(D1)	V3	P140	469
I/O_(RCLK-/BUSY/RDY)	V2	P141	472
I/O	U4	P142	475
I/O	T5	P143	478
I/O_(D0*_DIN)	U3	P144	481
SGCK4_(DOUT*_I/O)	T4	P145	484
CCLK	V1	P146	-
VCC	R4	P147	-
TDO	U2	P148	-
GND	R3	P149	-
I/O_(A0*_WS)	T3	P150	2
PGCK4_(I/O*_A1)	U1	P151	5
-	-	P152*	-
I/O	P3	P153	8
I/O	R2	P154	11
I/O_(CS1*_A2)	T2	P155	14
I/O_(A3)	N3	P156	17
I/O	P2	P157	20
I/O	T1	P158	23
I/O	R1	P159	26
I/O	N2	P160	29
GND	M3	P161	-
I/O	P1	P162	32
I/O	N1	P163	35

* Indicates unconnected package pins.
** Contributes only one bit (.I) to the boundary scan register.
Boundary Scan BIt 0 = TD0.T
Boundary Scan Bit 1 = TD0.0
Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O_(A4)	M2	P164	38
I/O_(A5)	M1	P165	41
I/O	L3	P166	44
I/O	L2	P167	47
I/O	L1	P168	50
I/O	K1	P169	53
I/O_(A6)	K2	P170	56
I/O_(A7)	K3	P171	59
GND	K4	P172	-
VCC	J4	P173	-
I/O_(A8)	J3	P174	62
I/O_(A9)	J2	P175	65
I/O	J1	P176	68
I/O	H1	P177	71
I/O	H2	P178	74
I/O	H3	P179	77
I/O_(A10)	G1	P180	80
I/O_(A11)	G2	P181	83
I/O	F1	P182	86
I/O	E1	P183	89

* Indicates unconnected package pins.
** Contributes only one bit (.I) to the boundary scan register.
Boundary Scan BIt 0 = TD0.T
Boundary Scan Bit 1 = TD0.0
Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
GND	G3	P184	-
I/O	F2	P185	92
I/O	D1	P186	96
I/O	C1	P187	98
I/O	E2	P188	101
I/O_(A12)	F3	P189	104
I/O_(A13	D2	P190	107
-	-	P192*	-
I/O	E3	P193	113
I/O_(A14)	C2	P194	116
SGCK1(A15*I/O)	B2	P195	119
VCC	D3	P196	-

* Indicates unconnected package pins.
** Contributes only one bit (.I) to the boundary scan register.
Boundary Scan BIt 0 = TD0.T
Boundary Scan Bit 1 = TD0.0
Boundary Scan Bit 487 = BSCAN.UPD

Additional XQ4010E Package Pins

CB196

N.C. Pins			
P5	P54	P103	P152
P192	-	-	-

Note: Information current as of 8/14/97.

Example Ordering Information