XV Specification Information

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions.

All specifications subject to change without notice.

XC4000XV D.C. Characteristics

Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CCINT}	Supply voltage relative to GND		-0.5 to 3.0	V
V_{CCIO}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to 5.5	V
V_{CC}	Longest Supply Voltage Rise Time from 1 V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC excursion above V_{cc} or below Ground must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot toV_{CC} + 2.0 V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	2.3	2.7	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	2.3	2.7	V
V_{CCIO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Notes: At junction temperatures above those listed above, all delay parameters increase by 0.35% per °C.
Input and output measurement threshold is ~50% of V_{CC}.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min (LVTTL)		2.4		V
	High-level output voltage @ I_{OH} = -500 µA, (LVCMOS)		90% V_{CC}		V
V_{OL}	Low-level output voltage @ I_{OL} = 24.0 mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)			10% V_{CC}	V
V_{DRINT}	V_{CCINT} Data Retention Supply Voltage (below which configuration data may be lost)		2.1		V
V_{DRIO}	V_{CCIO} Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			10	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, & MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 24 mA.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating.

XC4000XV Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Global Buffer Switching Characteristics Guidelines

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
Delay from pad through Global Low Skew (GLS) clock buffer to any clock input, K.	T_{GLS}	XC40110XV		7.2	6.3	5.4	ns
		XC40150XV		**7.3**	6.4	5.5	ns
		XC40200XV		8.8	7.7	6.6	ns
		XC40250XV		8.9	7.8	6.7	ns
Delay from pad through Global Early (GE) clock buffer to any IOB clock input for BUFGE #s 1, 2, 5, and 6.	T_{GE_1256}	XC40110XV		2.5	2.2	1.8	ns
		XC40150XV		**2.6**	2.3	1.9	ns
		XC40200XV		2.9	2.6	2.2	ns
		XC40250XV		3.0	2.7	2.3	ns
Delay from pad through Global Early (GE) clock buffer to any IOB clock input for BUFGE #s 3, 4, 7, and 8.	T_{GE_3478}	XC40110XV		5.1	4.5	3.8	ns
		XC40150XV		**5.2**	4.6	3.9	ns
		XC40200XV		5.6	4.9	4.2	ns
		XC40250XV		5.7	5.0	4.3	ns
Delay from pad through FastCLK buffer to any IOB clock input	T_{FCLK}	XC40110XV		5.1	4.5	3.8	ns
		XC40150XV		**5.2**	4.6	3.9	ns
		XC40200XV		5.6	4.9	4.2	ns
		XC40250XV		5.7	5.0	4.3	ns

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance.

Advance

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XC4000XV CLB Characteristics Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

CLB Switching Characteristic Guidelines

Description	Speed Grade Symbol	-09 Min	-09 Max	-08 Min	-08 Max	-07 Min	-07 Max	Units
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		1.3		1.1		1.0	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		2.0		1.7		1.5	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		2.1		1.8		1.6	ns
C inputs via SR/H0 via H to X/Y outputs	T_{HH0O}		1.9		1.6		1.4	ns
C inputs via H1 via H to X/Y outputs	T_{HH1O}		1.7		1.5		1.3	ns
C inputs via DIN/H2 via H to X/Y outputs	T_{HH2O}		1.9		1.6		1.4	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass0	T_{CBYP}		1.2		1.0		0.9	ns
CLB Fast Carry Logic								
Operand inputs (F1, F2, G1, G4) to C_{OUT}	T_{OPCY}		2.2		1.9		1.7	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		1.3		1.1		1.0	ns
Initialization inputs (F1, F3) to C_{OUT}	T_{INCY}		1.4		1.2		1.0	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		1.8		1.6		1.4	ns
C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		0.3		0.2		0.2	ns
Carry Net Delay, C_{OUT} to C_{IN}	T_{NET}		0.4		0.3		0.3	ns
Sequential Delays								
Clock K to Flip-Flop outputs Q	T_{CKO}		1.6		1.4		1.2	ns
Clock K to Latch outputs Q	T_{CKLO}		1.6		1.4		1.2	ns
Setup Time before Clock K								
F/G inputs	T_{ICK}	0.8		0.7		0.6		ns
F/G inputs via H	T_{IHCK}	1.5		1.3		1.1		ns
C inputs via H0 through H	T_{HH0CK}	1.4		1.2		1.0		ns
C inputs via H1 through H	T_{HH1CK}	1.2		1.1		0.9		ns
C inputs via H2 through H	T_{HH2CK}	1.4		1.2		1.0		ns
C inputs via DIN	T_{DICK}	0.6		0.6		0.5		ns
C inputs via EC	T_{ECCK}	0.7		0.6		0.5		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.6		0.5		0.4		ns
CIN input via F/G	T_{CCK}	1.3		1.1		1.0		ns
CIN input via F/G and H	T_{CHC}	2.0		1.7		1.5		ns
Hold Time after Clock K								
All Hold Times		0.0		0.0		0.0		ns
Clocks								
Clock High time	T_{CH}	2.3		2.0		1.7		ns
Clock Low time	T_{CL}	2.3		2.0		1.7		ns
Set/Reset Direct								
Width (High)	T_{RPW}	3.0		2.8		2.5		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		2.6		2.3		2.0	ns
Global Set/Reset								
Minimum GSR Pulse Width	T_{MRW}		13.4		11.7		10.2	ns
Delay from GSR input to any Q	T_{MRQ}	See page 197 for TRRI values per device						
Toggle Frequency (MHz) (for export control purposes)	F_{TOG}		224		258		296	MHz
		Advance						

CLB RAM Single Port Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XV devices and are expressed in nanoseconds unless otherwise noted.

Single Port RAM	Speed Grade		-09		-08		-07		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Write Operation									
Address write cycle time (clock K period)	16x2	T_{WCS}	7.0		6.1		5.3		ns
	32x1	T_{WCTS}	7.0		6.1		5.3		ns
Clock K pulse width (active edge)	16x2	T_{WPS}	3.5		3.1		2.7		ns
	32x1	T_{WPTS}	3.5		3.1		2.7		ns
Address setup time before clock K	16x2	T_{ASS}	1.5		1.3		1.2		ns
	32x1	T_{ASTS}	1.6		1.4		1.2		ns
Address hold time after clock K	16x2	T_{AHS}	0.0		0.0		0.0		ns
	32x1	T_{AHTS}	0.0		0.0		0.0		ns
DIN setup time before clock K	16x2	T_{DSS}	1.6		1.4		1.2		ns
	32x1	T_{DSTS}	2.0		1.7		1.5		ns
DIN hold time after clock K	16x2	T_{DHS}	0.0		0.0		0.0		ns
	32x1	T_{DHTS}	0.0		0.0		0.0		ns
WE setup time before clock K	16x2	T_{WSS}	1.5		1.3		1.2		ns
	32x1	T_{WSTS}	1.4		1.3		1.1		ns
WE hold time after clock K	16x2	T_{WHS}	0.0		0.0		0.0		ns
	32x1	T_{WHTS}	0.0		0.0		0.0		ns
Data valid after clock K	16x2	T_{WOS}		5.2		4.6		4.0	ns
	32x1	T_{WOTS}		6.2		5.4		4.7	ns
Read Operation									
Address read cycle time	16x2	T_{RC}	4.5		3.1		3.1		ns
	32x1	T_{RCT}	6.5		5.5		5.5		ns
Data Valid after address change (no Write Enable)	16x2	T_{ILO}		1.3		1.1		1.0	ns
	32x1	T_{IHO}		2.0		1.7		1.5	ns
Address setup time before clock K	16x2	T_{ICK}	0.8		0.7		0.6		ns
	32x1	T_{IHCK}	1.5		1.3		1.1		ns
			Advance						

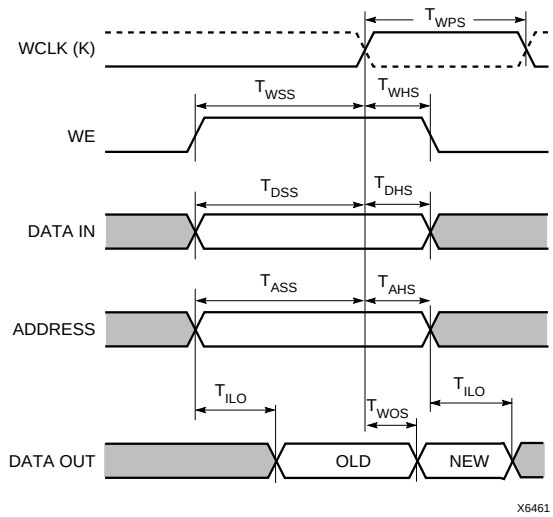
CLB RAM Dual Port Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

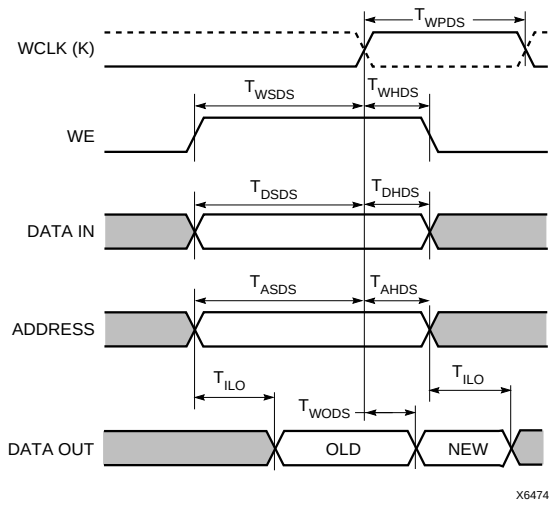
Dual Port RAM	Speed Grade		-09		-08		-07		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Address write cycle time (clock K period)	16x1	T_{WCDS}	7.0		6.1		5.3		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	3.5		3.1		2.7		ns
Address setup time before clock K	16x1	T_{ASDS}	1.5		1.3		1.2		ns
Address hold time after clock K	16x1	T_{AHDS}	0.0		0.0		0.0		ns
DIN setup time before clock K	16x1	T_{DSDS}	1.9		1.7		1.4		ns
DIN hold time after clock K	16x1	T_{DHDS}	0.0		0.0		0.0		ns
WE setup time before clock K	16x1	T_{WSDS}	1.5		1.3		1.2		ns
WE hold time after clock K	16x1	T_{WHDS}	0.0		0.0		0.0		ns
Data valid after clock K	16x1	T_{WODS}		6.0		5.3		4.6	ns
			Advance						

Note: Timing for 16x1 option is identical to 16x2 RAM.

CLB RAM Synchronous (Edge-Triggered) Write Timing Waveforms



Single Port RAM



Dual Port RAM

XC4000XV Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Global Clock Input to Output Delay Guidelines

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
Global Low Skew (GLS) Clock Input to Output Delay using Output Flip-Flop.	T_{ICKOF}	XC40110XV		10.6	9.2	8.0	ns
		XC40150XV		**10.7**	9.3	8.1	ns
		XC40200XV		12.2	10.6	9.2	ns
		XC40250XV		12.3	10.7	9.3	ns
For output SLOW option add	T_{SLOW}	All Devices		1.7	1.6	1.4	ns

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance.

Advance

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST mode specification.

Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 1.

Low Skew FastCLK Input to Output Delay Guidelines for BUFNW, SW, NE, and SE

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
FastCLK Input to Output Delay using Output Flip-Flop for FastCLK buffers BUFNW, BUFSW, BUFNE, and BUFSE.	T_{ICKFOF}	XC40110XV		5.9	5.1	4.4	ns
		XC40150XV		**6.0**	5.2	4.5	ns
		XC40200XV		6.3	5.5	4.8	ns
		XC40250XV		6.4	5.6	4.9	ns

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance.

Advance

Notes: Listed above are representative values where one FastCLK input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the FastCLK net.

Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST slew mode specification.

Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 1.

Global Early Clock Input to Output Delay Guidelines for BUFGE #s 1, 2, 5, and 6

Description	Symbol	Speed Grade / Device	All Min	-09 Max	-08 Max	-07 Max	Units
Global Clock Signal Input to Output Delay using Global Early (GE) clock buffer to clock Output Flip-Flop for BUFGE #s 1, 2, 5, and 6.	T_{ICKEOF_1256}	XC40110XV		8.5	7.4	6.4	ns
		XC40150XV		**8.6**	7.5	6.5	ns
		XC40200XV		9.0	7.8	6.8	ns
		XC40250XV		9.1	7.9	6.9	ns
				Advance			

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance.

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST mode specification.

Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 1.

Global Early Clock Input to Output Delay Guidelines for BUFGE #s 3, 4, 7, and 8

Description	Symbol	Speed Grade / Device	All Min	-09 Max	-08 Max	-07 Max	Units
Global Clock Signal Input to Output Delay using Global Early (GE) clock buffer to clock Output Flip-Flop for BUFGE #s 3, 4, 7, and 8.	T_{ICKEOF_3478}	XC40110XV		8.5	7.4	6.4	ns
		XC40150XV		**8.**6	7.5	6.5	ns
		XC40200XV		9.0	7.8	6.8	ns
		XC40250XV		9.1	7.9	6.9	ns
				Advance			

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance.

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST mode specification.

Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 1.

Capacitive Load Factor

Figure 1 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 1 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

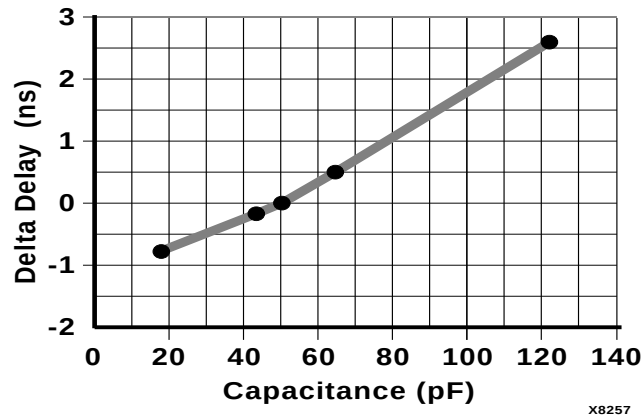


Figure 1: Delay Factor at Various Capacitive Loads

XC4000XV Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Global Low Skew Clock, Set-Up and Hold Guidelines

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC40110XV	0.0 / 6.8	0.0 / 5.9	0.0 / 5.1	ns
Global Low Skew Clock and IFF	T_{PSN}/T_{PHN}	XC40150XV	**0.0 / 7.5**	0.0 / 6.6	0.0 / 5.7	ns
Global Low Skew Clock and FCL		XC40200XV	0.0 / 8.8	0.0 / 6.7	0.0 / 6.7	ns
		XC40250XV	0.0 / 9.8	0.0 / 8.5	0.0 / 7.4	ns
Partial Delay		XC40110XV	5.5 / 0.5	4.8 / 0.5	4.1 / 0.4	ns
Global Low Skew Clock and IFF	T_{PSP}/T_{PHP}	XC40150XV	**6.1 / 0.5**	5.3 / 0.5	4.6 / 0.4	ns
Global Low Skew Clock and FCL		XC40200XV	7.9 / 0.3	6.8 / 0.2	5.9 / 0.2	ns
		XC40250XV	8.7 / 0.0	7.6 / 0.0	6.6 / 0.0	ns
Full Delay		XC40110XV	8.0 / 0.0	6.9 / 0.0	6.0 / 0.0	ns
Global Low Skew Clock and IFF	T_{PSD}/T_{PHD}	XC40150XV	**8.9 / 0.0**	7.7 / 0.0	6.7 / 0.0	ns
		XC40200XV	9.4 / 0.0	8.2 / 0.0	7.1 / 0.0	ns
		XC40250XV	9.7 / 0.0	8.4 / 0.0	7.3 / 0.0	ns
IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch				**Advance**		

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance.

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

FastCLK Input Set-Up and Hold Guidelines for BUFNW, SW, NE, and SE

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
No Delay		XC40110XV	0.8 / 4.2	0.7 / 3.7	0.6 / 3.2	ns
FastCLK and IFF	T_{PSFN}/T_{PHFN}	XC40150XV	**0.8 / 4.6**	0.7 / 4.0	0.6 / 3.5	ns
		XC40200XV	0.8 / 4.9	0.7 / 4.3	0.6 / 3.7	ns
		XC40250XV	0.8 / 5.3	0.7 / 4.6	0.6 / 4.0	ns
Partial Delay		XC40110XV	11.0 / 0.0	9.5 / 0.0	8.3 / 0.0	ns
FastCLK and IFF	T_{PSFP}/T_{PHFP}	XC40150XV	**11.1 / 0.0**	9.7 / 0.0	8.4 / 0.0	ns
		XC40200XV	11.4 / 0.0	9.9 / 0.0	8.6 / 0.0	ns
		XC40250XV	11.6 / 0.0	10.1 / 0.0	8.8 / 0.0	ns
Full Delay		XC40110XV	11.7 / 0.0	10.5 / 0.0	9.1 / 0.0	ns
FastCLK and IFF	T_{PSFD}/T_{PHFD}	XC40150XV	**11.8 / 0.0**	10.6 / 0.0	9.2 / 0.0	ns
		XC40200XV	12.4 / 0.0	10.8 / 0.0	9.4 / 0.0	ns
		XC40250XV	12.7 / 0.0	11.0 / 0.0	9.6 / 0.0	ns
IFF = Input Flip-Flop or Latch				**Advance**		

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance

Notes: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

BUFGE #s 1, 2, 5, & 6 Global Early Clock, Set-Up and Hold for IFF and FCL Guidelines

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC40110XV	0.5 / 6.1	0.4 / 5.3	0.4 / 4.6	ns
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XC40150XV	**0.6 / 6.2**	0.5 / 5.4	0.4 / 4.7	ns
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XC40200XV	1.3 / 7.3	1.2 / 6.3	1.0 / 5.5	ns
		XC40250XV	1.5 / 7.5	1.3 / 6.6	1.1 / 5.7	ns
Partial Delay		XC40110XV	7.3 / 0.0	6.3 / 0.0	5.5 / 0.0	ns
Global Early Clock and IFF	T_{PSEP}/T_{PHEP}	XC40150XV	**8.1 / 0.0**	7.0 / 0.0	6.1 / 0.0	ns
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XC40200XV	10.8 / 0.0	9.4 / 0.0	8.2 / 0.0	ns
		XC40250XV	12.0 / 0.0	10.5 / 0.0	9.1 / 0.0	ns
FullDelay		XC40110XV	10.6 / 0.0	9.2 / 0.0	8.0 / 0.0	ns
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC40150XV	**10.7 / 0.0**	9.3 / 0.0	8.1 / 0.0	ns
		XC40200XV	11.9 / 0.0	10.4 / 0.0	9.0 / 0.0	ns
		XC40250XV	13.1 / 0.0	11.4 / 0.0	9.9 / 0.0	ns
				Advance		

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance.

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

BUFGE #s 3, 4, 7, & 8 Global Early Clock, Set-Up and Hold for IFF and FCL Guidelines

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC40110XV	0.4 / 5.2	0.3 / 4.5	0.3 / 3.9	ns
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XC40150XV	**0.4 / 5.3**	0.4 / 4.6	0.3 / 4.0	ns
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XC40200XV	0.9 / 6.2	0.8 / 5.4	0.7 / 4.7	ns
		XC40250XV	1.1 / 6.5	0.9 / 5.6	0.8 / 4.9	ns
Partial Delay		XC40110XV	7.4 / 0.0	6.5 / 0.0	5.6 / 0.0	ns
Global Early Clock and IFF	T_{PSEP}/T_{PHEP}	XC40150XV	**7.5 / 0.0**	6.6 / 0.0	5.7 / 0.0	ns
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XC40200XV	9.7 / 0.0	8.4 / 0.0	7.3 / 0.0	ns
		XC40250XV	11.6 / 0.0	10.1 / 0.0	8.8 / 0.0	ns
FullDelay		XC40110XV	10.0 / 0.0	8.6 / 0.0	7.5 / 0.0	ns
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC40150XV	**10.1 / 0.0**	8.7 / 0.0	7.6 / 0.0	ns
		XC40200XV	10.7 / 0.0	9.3 / 0.0	8.1 / 0.0	ns
		XC40250XV	12.8 / 0.0	11.2 / 0.0	9.7 / 0.0	ns
				Advance		

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance.

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-09		-08		-07		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Clocks									
Clock Enable (EC) to Clock (IK)	T_{ECIK}	All Devices	0.0		0.0		0.0		ns
Delay from Fast Capture Latch enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	All Devices	1.3		1.2		1.0		ns
Setup Times									
Pad to Clock (IK), no delay	T_{PICK}	All Devices	1.3		1.1		1.0		ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	Al Devices	1.8		1.6		1.4		ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	All Devices	1.1		1.0		0.8		ns
Hold Times									
All Hold Times		All Devices	0.0		0.0		0.0		ns
Global Set/Reset									
Minimum GSR Pulse Width	T_{MRW}	All Devices	13.4		11.7		10.2		ns
Delay from GSR input to any Q	T_{RRI*}	XC40110XV	27.2		23.6		20.5		ns
		XC40150XV	**29.1**		25.3		22.0		ns
		XC40200XV	33.8		29.4		25.5		ns
		XC40250XV	35.8		31.1		27.0		ns
Propagation Delays									
Pad to I1, I2	T_{PID}	All devices		1.6		1.4		1.2	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices		2.7		2.3		2.0	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}	All Devices		3.6		3.1		2.7	ns
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All Devices		1.4		1.2		1.1	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All Devices		1.6		1.4		1.2	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{OKLI}	All Devices		2.7		2.4		2.1	ns
			Advance						

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch.

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance.

* Indicates Minimum Amount of Time to Assure Valid Data.

IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-09		-08		-07		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Clocks									
Clock High	T_{CH}	All Devices	2.3		2.0		1.7		ns
Clock Low	T_{CL}	All Devices	2.3		2.0		1.7		ns
Propagation Delays (See Note 1)									
Clock (OK) to Pad	T_{OKPOF}	All Devices		3.5		3.0		2.7	ns
Output (O) to Pad	T_{OPF}	All Devices		3.0		2.6		2.3	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}	All Devices		3.0		2.6		2.2	ns
3-state to Pad active and valid	T_{TSONF}	All Devices		3.1		2.7		2.3	ns
Clock to Pad hi-Z	T_{OKSHZ}	All Devices		4.7		4.1		3.5	ns
Clock to Pad active and valid	T_{OKSONF}	All Devices		4.8		4.2		3.6	ns
Output (O) to Pad via Fast Output MUX	T_{OFPF}	All Devices		4.4		3.8		3.3	ns
Select (OK) to Pad via Fast MUX	T_{OKFPF}	All Devices		4.0		3.5		3.0	ns
Setup and Hold Times									
Output (O) to clock (OK) setup time	T_{OOK}	All Devices	0.4		0.4		0.3		ns
Output (O) to clock (OK) hold time	T_{OKO}	All Devices	0.0		0.0		0.0		ns
Clock Enable (EC) to clock (OK) setup time	T_{ECOK}	All Devices	0.0		0.0		0.0		ns
Clock Enable (EC) to clock (OK) hold time	T_{OKEC}	All Devices	0.3		0.2		0.1		ns
Global Set/Reset									
Minimum GSR pulse width	T_{MRW}	All Devices	13.4		11.7		10.2		ns
Delay from GSR input to any Pad	T_{RPO*}	XC40110XV		30.5		26.6		23.1	ns
		XC40150XV		**32.5**		28.3		24.6	ns
		XC40200XV		37.1		32.3		28.1	ns
		XC40250XV		39.1		34.0		29.6	ns
Slew Rate Adjustment									
For output SLOW option add	T_{SLOW}	All Devices		2.3		2.0		1.7	ns

* Indicates Minimum Amount of Time to Assure Valid Data.

Advance

Bold Face: Preliminary Values for the XC40150-09. All other values are Advance.
Note: Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads.

Revision Control

Version	Description
2/1/99 (1.0)	Release included in 1999 data book, section 6
2/19/99 (1.1)	Updated Switching Characteristics Tables
5/14/99 (1.2)	Replaced Electrical Specification pages for XLA and XV families with separate updates and added URL link on placeholder page for electrical specifications/pinouts for WebLINX users.