XCR3256XL 256 Macrocell CPLD

DS013 (v1.5) January 17, 2001 **Preliminary Product Specification**

Features

- 7.5 ns pin-to-pin logic delays
- System frequencies up to 140 MHz
- 256 macrocells with 6,400 usable gates
- Available in small footprint packages
  - 144-pin TQFP (120 user I/O pins)
  - 208-pin PQFP (164 user I/O)
  - 280-ball CS BGA (164 user I/O)
- Optimized for 3.3V systems
  - Ultra low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five metal layer re-programmable process
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 clocks available per function block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per function block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V supply voltage at industrial grade voltage range
- Programmable slew rate control per output
- Security bit prevents unauthorized access
- Refer to XPLA3 family data sheet (DS012) for architecture description

Description

The XCR3256XL is a 3.3V, 256 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of 16 function blocks provide 6,400 usable gates. Pin-to-pin propagation delays are 7.5 ns with a maximum system frequency of 140 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 1 and Table 1 showing the I_{CC} vs. Frequency of our XCR3256XL TotalCMOS CPLD (data taken with 16 up/down, loadable 16-bit counters at 3.3V, 25°C).

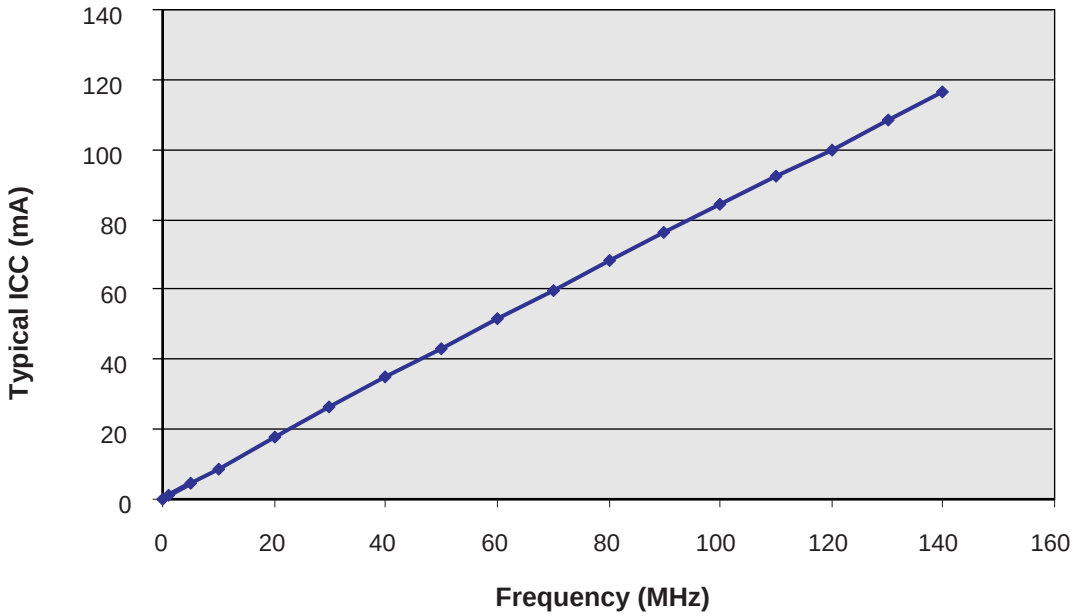


Figure 1: **XCR3256XL Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Table 1: **Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Frequency (MHz)	0	1	10	20	40	60	80	100	120	140
Typical I_{CC} (mA)	0.02	0.91	8.87	17.7	34.8	51.5	68	84.2	100.1	116.6

DC Electrical Characteristics Over Recommended Operating Conditions(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output High voltage for 3.3V outputs	I_{OH} = –8 mA	2.4	-	V
V_{OL}	Output Low voltage for 3.3V outputs	I_{OL} = 8 mA	-	0.4	V
I_{IL}	Input leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{IH}	I/O High-Z leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{CCSB}	Standby current	V_{CC} = 3.6V	-	100	µA
I_{CC}	Dynamic current(2,3)	f = 1 MHz	-	2	mA
		f = 50 MHz	-	60	mA
C_{IN}	Input pin capacitance(4)	f = 1 MHz	-	8	pF
C_{CLK}	Clock input capacitance(4)	f = 1 MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance(4)	f = 1 MHz	-	10	pF

Notes:
1. See XPLA3 family data sheet (DS012) for recommended operating conditions.
2. See Table 1, Figure1 for typical values.
3. This parameter measured with a 16-bit, loadable up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
4. Typical values, not tested.

AC Electrical Characteristics Over Recommended Operating Conditions(1,2)

Symbol	Parameter	-7		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay time (single p-term)	-	7.0	-	9.0	-	10.8	ns
T_{PD2}	Propagation delay time (OR array)(3)	-	7.5	-	10.0	-	12.0	ns
T_{CO}	Clock to output (global synchronous pin clock)	-	4.5	-	5.8	-	6.9	ns
T_{SUF}(4)	Setup time fast	2.0	-	2.5	-	3.0	-	ns
T_{SU}(4)	Setup time	4.8	-	6.5	-	7.9	-	ns
T_{H}(4)	Hold time	0	-	0	-	0	-	ns
T_{WLH}(4)	Global Clock pulse width (High or Low)	3.0	-	4.0	-	5.0	-	ns
Tt_{PLH}(4)	P-term clock pulse width	4.5	-	6.0	-	7.5	-	ns
T_{R}(4)	Input rise time	-	20	-	20	-	20	ns
T_{L}(4)	Input fall time	-	20	-	20	-	20	ns
f_{SYSTEM}(4)	Maximum system frequency	-	140	-	105	-	88	MHz
T_{CONFIG}(4)	Configuration time(5)	-	40	-	40	-	40	µs
T_{POE}(4)	P-term OE to output enabled	-	9.0	-	11.0	-	13.0	ns
T_{POD}(4)	P-term OE to output disabled(6)	-	9.0	-	11.0	-	13.0	ns
T_{PCO}(4)	P-term clock to output	-	8.0	-	10.3	-	12.4	ns
T_{PAO}(4)	P-term set/reset to output valid	-	9.0	-	11.0	-	13.0	ns

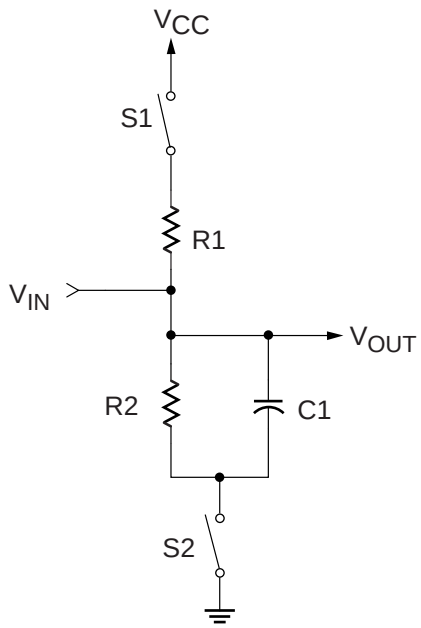
Notes:
1. Specifications measured with one output switching.
2. See XPLA3 family data sheet (DS012) for recommended operating conditions.
3. See Figure 3 for derating.
4. These parameters guaranteed by design and/or characterization, not testing.
5. Typical current draw during configuration is 10 mA at 3.6V.
6. Output C_L = 5 pF.

Internal Timing Parameters(1,2)

Symbol	Parameter	-7		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	2.5	-	3.3	-	4.0	ns
T_{FIN}	Fast input buffer delay	-	2.2	-	2.8	-	3.3	ns
T_{GCK}	Global clock buffer delay	-	1.0	-	1.3	-	1.5	ns
T_{OUT}	Output buffer delay	-	2.5	-	2.8	-	3.3	ns
T_{EN}	Output buffer enable/disable delay	-	4.5	-	5.2	-	6.0	ns
Internal Register and Combinatorial Delays								
T_{LDI}	Latch transparent delay	-	1.3	-	1.6	-	2.0	ns
T_{SUI}	Register setup time	0.8	-	1.0	-	1.2	-	ns
T_{HI}	Register hold time	4.0	-	5.5	-	6.7	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.5	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	3.0	-	4.5	-	5.5	-	ns
T_{COI}	Register clock to output delay	-	1.0	-	1.3	-	1.6	ns
T_{AOI}	Register async. S/R to output delay	-	2.0	-	2.0	-	2.2	ns
T_{RAI}	Register async. recovery	-	5.0	-	7.0	-	8.0	ns
T_{LOGI1}	Internal logic delay (single p-term)	-	2.0	-	2.5	-	3.0	ns
T_{LOGI2}	Internal logic delay (PLA OR term)	-	2.5	-	3.5	-	4.2	ns
Feedback Delays								
T_{F}	ZIA delay	-	2.8	-	3.7	-	4.4	ns
Time Adders								
T_{LOGI3}	Fold-back NAND delay	-	6.0	-	8.0	-	9.5	ns
T_{UDA}	Universal delay	-	2.0	-	2.5	-	3.0	ns
T_{SLEW}	Slew rate limited delay	-	4.0	-	5.0	-	6.0	ns

Notes:
1. These parameters guaranteed by design and/or characterization, not testing.
2. See XPLA3 family data sheet (DS012) for the timing model.

Switching Characteristics



Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T_{POE} (High)	Open	Closed
T_{POE} (Low)	Closed	Open
T_P	Closed	Closed

Note: For T_{POD}, C1 = 5 pF

DS013_03_050200

Figure 2: **AC Load Circuit**

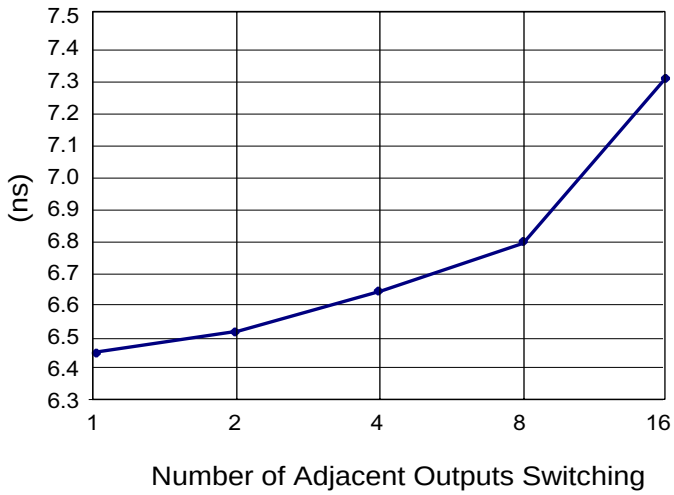


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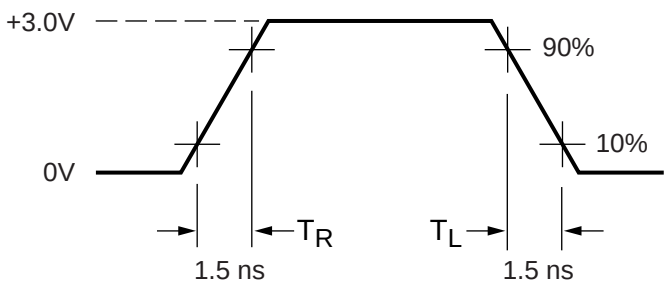
Figure 3: **Derating Curve for T_{PD2}**



Measurements:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

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Figure 4: **Voltage Waveform**

Pin Descriptions

Table 2: **XCR3256XL I/O Pins**

Function Block	Macrocell	TQ144	PQ208	CS280
1	1	106	6	E18
1	2	-	7	E19
1	3	104(1)	8	F15
1	4	103	9	F17
1	5	102	10	F18
1	6	-	-	-
1	7	-	-	-
1	8	-	-	-
1	9	-	-	-
1	10	-	-	-
1	11	-	-	-
1	12	101	11	F19
1	13	100	12	G16
1	14	99	13	G17
1	15	-	15	G19
1	16	-	16	H16
2	1	107	4	B19
2	2	108	3	B18
2	3	-	206	B17
2	4	-	205	A18
2	5	109	204	A17
2	6	-	-	-
2	7	-	-	-
2	8	-	-	-
2	9	-	-	-
2	10	-	-	-
2	11	-	-	-
2	12	110	203	C16
2	13	111	202	A16
2	14	-	201	E15
2	15	112	199	D15
2	16	113	198	A15
3	1	98	17	H17
3	2	97	18	H18
3	3	96	19	H19
3	4	94	20	J16
3	5	93	21	J17
3	6	-	-	-
3	7	-	-	-
3	8	-	-	-
3	9	-	-	-
3	10	-	-	-
3	11	-	-	-
3	12	92	22	J18
3	13	-	24	K16
3	14	91	25	K17
3	15	90	26	K18
3	16	-	27	L16
4	1	114	197	E14
4	2	116	196	D14
4	3	117	195	A14
4	4	-	194	C13
4	5	118	193	B13
4	6	-	-	-
4	7	-	-	-
4	8	-	-	-
4	9	-	-	-
4	10	-	-	-
4	11	-	-	-
4	12	119	192	A13
4	13	120	190	A12
4	14	121	189(1)	C12(1)
4	15	-	188	B12
4	16	122	187	D12
5	1	89(1)	28	L17
5	2	-	29	L18
5	3	88	30(1)	L19(1)
5	4	87	31	M16
5	5	86	33	M18
5	6	-	-	-
5	7	-	-	-
5	8	-	-	-
5	9	-	-	-

Table 2: **XCR3256XL I/O Pins *(Continued)***

Function Block	Macrocell	TQ144	PQ208	CS280
5	10	-	-	-
5	11	-	-	-
5	12	84	34	M17
5	13	-	35	N16
5	14	83	36	N19
5	15	82	37	N18
5	16	-	38	N17
6	1	-	78	U10
6	2	55	77	T10
6	3	56	76	W11
6	4	-	73	U11
6	5	60	71	T11
6	6	-	-	-
6	7	-	-	-
6	8	-	-	-
6	9	-	-	-
6	10	-	-	-
6	11	-	-	-
6	12	61	70	W12
6	13	62	69	U12
6	14	63	68	T12
6	15	-	67	V13
6	16	65	66	U13
7	1	81	39	P16
7	2	-	40	P18
7	3	80	42	R19
7	4	79	43	R16
7	5	78	44	R18
7	6	-	-	-
7	7	-	-	-
7	8	-	-	-
7	9	-	-	-
7	10	-	-	-
7	11	-	-	-
7	12	77	45	R17
7	13	-	46	R15
7	14	75	47	T17
7	15	74	48	T16
7	16	-	49	U19
8	1	66	65	T13
8	2	67	64	W14
8	3	68	62	T14
8	4	69	61	R14
8	5	-	60	W15
8	6	-	-	-
8	7	-	-	-
8	8	-	-	-
8	9	-	-	-
8	10	-	-	-
8	11	-	-	-
8	12	70	59	U15
8	13	-	58	V15
8	14	71	57	T15
8	15	-	56	V16
8	16	72	55	W17
9	1	2	153	B1
9	2	1	154	C3
9	3	-	159	A4
9	4	-	160	B5
9	5	143	161	C5
9	6	-	-	-
9	7	-	-	-
9	8	-	-	-
9	9	-	-	-
9	10	-	-	-
9	11	-	-	-
9	12	-	162	A5
9	13	142	163	E6
9	14	141	164	D6
9	15	140	166	B6
9	16	139	167	A6
10	1	4(1)	151	D2
10	2	-	150	D1
10	3	5	149	E3

Table 2: **XCR3256XL I/O Pins *(Continued)***

Function Block	Macrocell	TQ144	PQ208	CS280
10	4	6	148	E2
10	5	7	147	E4
10	6	-	-	-
10	7	-	-	-
10	8	-	-	-
10	9	-	-	-
10	10	-	-	-
10	11	-	-	-
10	12	8	146	E1
10	13	-	145	F5
10	14	9	144	F3
10	15	10	142	F4
10	16	11	141	G3
11	1	-	168	D7
11	2	-	169	C7
11	3	138	170	B7
11	4	-	171	A7
11	5	137	172	C8
11	6	-	-	-
11	7	-	-	-
11	8	-	-	-
11	9	-	-	-
11	10	-	-	-
11	11	-	-	-
11	12	136	173	B8
11	13	134	175	C9
11	14	133	176(1)	B9(1)
11	15	132	177	D10
11	16	131	178	C10
12	1	-	140	G2
12	2	-	139	G1
12	3	12	138	G4
12	4	14	137	H1
12	5	15	136	H3
12	6	-	-	-
12	7	-	-	-
12	8	-	-	-

Table 2: **XCR3256XL I/O Pins *(Continued)***

Function Block	Macrocell	TQ144	PQ208	CS280
12	9	-	-	-
12	10	-	-	-
12	11	-	-	-
12	12	16	135	H2
12	13	-	133	J2
12	14	18	132	J3
12	15	19	131	K2
12	16	-	130	K3
13	1	-	79	W10
13	2	54	80	T9
13	3	53	81	U9
13	4	-	84	T8
13	5	49	86	T7
13	6	-	-	-
13	7	-	-	-
13	8	-	-	-
13	9	-	-	-
13	10	-	-	-
13	11	-	-	-
13	12	48	87	W7
13	13	47	88	V7
13	14	46	89	U7
13	15	-	90	W6
13	16	45	91	T6
14	1	20(1)	129	K4
14	2	-	128	L1
14	3	21	127(1)	L2(1)
14	4	22	126	L3
14	5	23	124	M1
14	6	-	-	-
14	7	-	-	-
14	8	-	-	-
14	9	-	-	-
14	10	-	-	-
14	11	-	-	-
14	12	25	123	M3
14	13	-	122	M4

Table 2: **XCR3256XL I/O Pins *(Continued)***

Function Block	Macrocell	TQ144	PQ208	CS280
14	14	26	121	N1
14	15	27	120	N2
14	16	28	119	N3
15	1	44	92	V6
15	2	43	93	U6
15	3	42	95	R6
15	4	41	96	W5
15	5	40	97	T5
15	6	-	-	-
15	7	-	-	-
15	8	-	-	-
15	9	-	-	-
15	10	-	-	-
15	11	-	-	-
15	12	-	98	V5
15	13	39	99	U5
15	14	38	100	W4
15	15	-	101	U4
15	16	37	102	W3
16	1	-	118	P1
16	2	-	117	P2
16	3	29	115	P4
16	4	30	114	R3
16	5	31	113	R2
16	6	-	-	-
16	7	-	-	-
16	8	-	-	-
16	9	-	-	-
16	10	-	-	-
16	11	-	-	-
16	12	32	112	R4
16	13	-	111	T3
16	14	34	110	U1
16	15	35	109	V1
16	16	36	108	U2

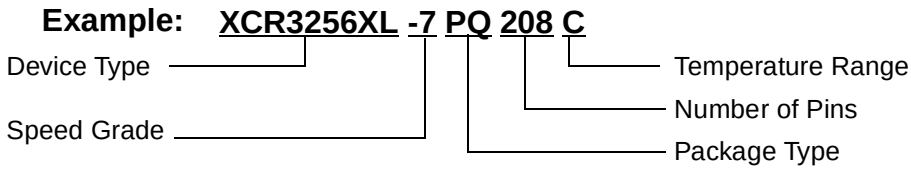
Notes:
1. JTAG pins.

Table 3: **XCR3256XL Global, JTAG, Port Enable, Power, and No Connect Pins**

Pin Type	TQ144	PQ208	CS280
IN0 / CLK0	128	181	A10
IN1 / CLK1	127	182	D11
IN2 / CLK2	126	183	C11
IN3 / CLK3	125	184	B11
TCK	89	30	L19
TDI	4	176	B9
TDO	104	189	C12
TMS	20	127	L2
PORT_EN	13(1)	116(1)	P3(1)
Vcc	24, 50, 51, 58, 73, 76, 95, 115, 123, 130, 144	5, 23, 41, 63, 74, 83, 85, 107, 125, 143, 165, 179, 186, 191	A11, B10, C6, C14, D13, D17, F2, J19, L4, P15, T18, U8, U14, V2, V9, V11
GND	3, 17, 33, 52, 57, 59, 64, 85, 105, 124, 129, 135	14, 32, 50, 72, 75, 82, 94, 134, 152, 174, 180, 185, 200	E5, E7, E8, E9, E10, E11, E12, E13, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, R7, R8, R9, R10, R11, R12, R13
No Connects	-	1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208	A1, A2, A3, A8, A9, A19, B2, B3, B4, B14, B15, B16, C1, C2, C4, C15, C17, C18, C19, D3, D4, D5, D8, D9, D16, D18, D19, E16, E17, F1, F16, G18, H4, J1, J4, K1, K19, M2, M19, N4, P5, P17, P19, R1, R5, T1, T2, T4, T19, U3, U16, U17, U18, V3, V4, V8, V10, V12, V14, V17, V18, V19, W1, W2, W8, W9, W13, W16, W18, W19

Notes:
1. Port Enable is brought High to enable JTAG pins when JTAG pins are used as I/O. See family data sheet for full explanation.

Ordering Information



Device Ordering Options

Speed	
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay
-7	7.5 ns pin-to-pin delay

Package	
TQ144	144-pin Thin Quad Flat Pack
PQ208	208-pin Plastic Quad Flat Package
CS280	280-ball Chip Scale Package

Temperature	
C = Commercial	T_A = 0°C to + 70°C V_{CC} = 3.0V to 3.6V
I = Industrial	T_A = –40°C to + 85°C V_{CC} = 2.7V to 3.6V

Component Compatibility

Pins		144	208	280
Type		Plastic TQFP	Plastic PQFP	Plastic BGA
Code		TQ144	PQ208	CS280
XCR3256XL	-7	C	C	C
	-10	C, I	C, I	C, I
	-12	C, I	C, I	C, I

Revision History

The following table shows the revision history for this document

Date	Version	Revision
01/21/00	1.0	Initial Xilinx release.
02/10/00	1.1	Updated Pinout table.
05/03/00	1.2	Minor updates and added Boundary Scan to pinout table.
11/20/00	1.3	Updated pinout tables.
12/11/00	1.4	Updated specifications and pinout tables.
01/17/01	1.5	Removed Timing Model.