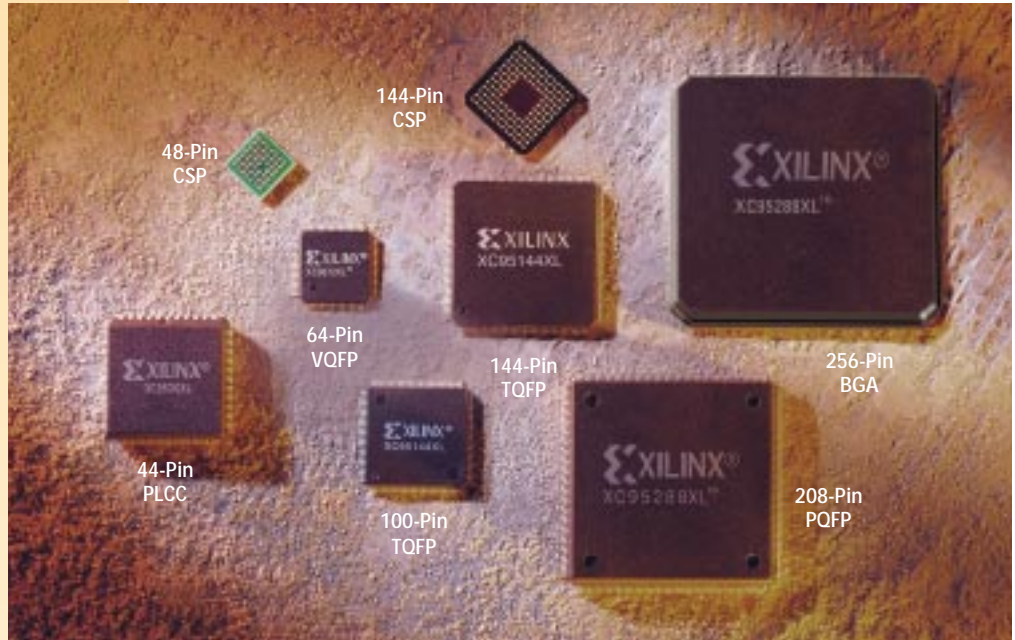


XC9500XL™

XC9500XL™ CPLD Family

3.3V, Faster, Lower Power, Lower Cost, New Features



The all-new XC9500XL™ series expands the capability of our popular XC9500™ family, bringing you more speed, more new features, and lower costs, in a new power-saving 3.3V technology. Targeted for leading-edge systems that require rapid design development, longer system life, and robust field upgrade capability, this series provides unparalleled performance along with the highest programming reliability and ease-of use. In addition, XC9500XL CPLDs easily complement our higher density FPGAs, giving you a total, seamless, logic solution; a robust, unified development environment that makes it very quick and easy for you to translate your creative ideas into working designs.

The XC9500XL family is WebPOWERED™ via its free WebFITTER™ and WebPACK™ software.

Family Overview:

- 36 to 288 macrocells
- 5ns pin-to-pin speeds with 222MHz system frequency
- Fast in-system programming and erase times
- Superior pin-locking for reliable field upgrade capability
- Full IEEE 1149.1 (JTAG) ISP and Boundary Scan test

Ideal Applications:

- DRAM controller
- Microprocessor interface
- Video clock generator
- Display driver
- Gate array patch
- Bus transceiver
- PAL/GAL consolidation
- LSI replacement

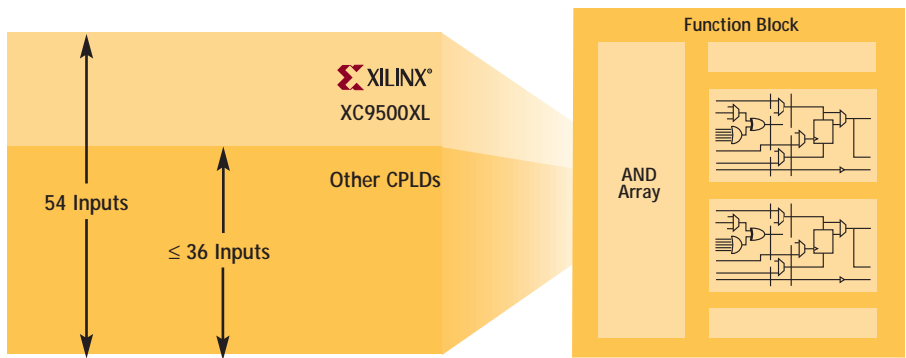
FastFLASH™ XC9500XL Family

	XC9536XL	XC9572XL	XC95144XL	XC95288XL
Macrocells	36	72	144	288
Usable	800	1,600	3,200	6,400
Registers	36	72	144	288
t _{PD} (ns)	5	5	5	6
f _{SYSTEM} (MHz)	222	222	222	208
User I/O Pins				
44-pin PLCC	34	34		
44-pin VQFP	34	34		
64-pin VQFP	36	52		
100-pin TQFP		72	81	
144-pin TQFP			117	117
208-pin PQFP				168
48-pin CSP	36	38		
144-pin CSP			117	
280-pin CSP				192
256-pin BGA				192
256-pin FBGA				192

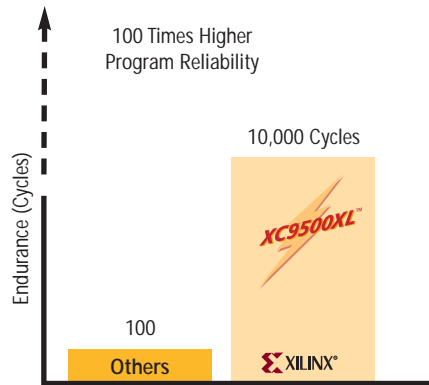
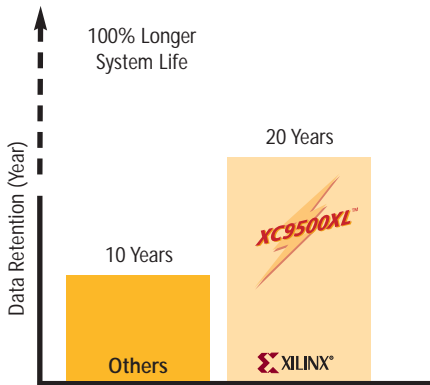
Advanced Architecture

- Ultra-wide 54 input function blocks for fast wide logic
- Oversized 18 macrocell blocks for lookahead logic
- 90 possible product-terms per macrocell
- Three global clocks and product-term clock, with inversion at macrocell
- Global and individual OE per output, with inversion at the output
- Bus-hold circuitry on all user I/O pins
- Input hysteresis on all user and JTAG inputs

50% Wider Block Fan-In



Highest Device Reliability



Solid Reliability

- Endurance rating of 10,000 cycles
- Virtually eliminates programming failures
- Data retention rating of 20 years
- Supports longer system life
- Immune from "ISP Lock-Out" failure mode
- Allows arbitrary mixed power sequencing ("hot-socketing")

Instant Design Evaluation Via WWW

Fast and easy evaluation for your CPLD designs is available instantly on the Internet. Simply go to the Xilinx homepage (www.xilinx.com) to access the WebFitter software and submit your sample designs. Or contact your local Xilinx sales representative for more information.

Features

- Highest performance 5 ns / 178 MHz
- Most flexible pin-locking architecture
- Highest device reliability
- Smallest packages (CSP)
- In-system programming via JTAG
- Robust 5V, 3.3V, 2.5V interfacing
- WebFITTER & WebPACK

Benefits

- Leading-edge computing applications
- Design iterations without board rework
- Higher quality, reduced support cost
- Reduced board area, increased flexibility
- Compatible with industry-standard ISP
- Worry free mixed voltage operation
- Easily accessible and free software tools saves development time and cost

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