IMA-8 Inverse Multiplexer for ATM

January 17, 2000 Product Specification

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Features

- Fully compliant with the ATM Forum Inverse Multiplexer for ATM (IMA) specification
- Supports the 8/16-bit UTOPIA Level 2 specification
- IMA Programmable Features
  - Number of Groups, 1-4
  - Number of Links, 1-8
  - Assignment of facilities to groups or pass-through
  - Differential Delay Compensation
  - IMA Frame Size (32, 64, 128, 256)
  - Transmit Clock Mode
  - Symmetrical/Asymmetrical Configuration and Operation
- IMA Date Cell Rate (IDCR) implementation
- IMA Device Driver software available
  - Simplifies Configuration and Status Reporting
  - Supports IMA MIB
  - Provides group start-up procedures
  - Controls link addition/deletion procedures
  - IMA Layer Failure Monitoring
  - IMA Layer Performance Monitoring
- Includes Diagnostics for external memory devices
- Chip solution provided for the specific IMA implementation

Applications

- Network access equipment such as adapters, multiplexers, routers, and switches
- Public/private UNI, NNI, and B-ICI applications

AllianceCORE™ Facts

Core Specifics	
Supported Family	Spartan-II
Device Tested	XC2S150-5FG256C
CLB Slices	1728
Clock IOBs	4
IOBs	147
Performance (MHz)	50
Xilinx Tools	M2.1i or later
Special Features	SelectRAM, Block RAM
Provided with Core	
Documentation	Product Brief Specification/Design Document Product Summary Software Specification
Design File Formats	Viewlogic schematic, VHDL source or PROM files
Constraints File	UCF file
Verification	Through ModelSIM and hardware evaluation board
Instantiation Templates	None
Reference designs & application notes	EP-IMA Hardware Evaluation Platform Schematic Reference Design
Additional Items	DRV-IMA Software Device Driver
Simulation Tool Used	
Modelsim PE V5.2e	
Support	
Support provided by Applied Telecom, Inc.	

General Description

The IMA products implement the ATM Forum Inverse Multiplexing for ATM (IMA) specification. The IMA specification uses a cell based multiplexing technique for converting a single ATM stream into multiple lower speed ATM streams for transmission over independent links. Applied Telecom's IMA-8 solution supports 8 physical links and 4 IMA groups with a maximum of 8 physical links per group. Mechanisms are specified for accommodating differential delay variations present in the transmission links and for handling link failures and changes to the available transmission bandwidth. Figure 1 illustrates the basic IMA mechanism for sending a single ATM cell stream over a number of lower speed transmission links.

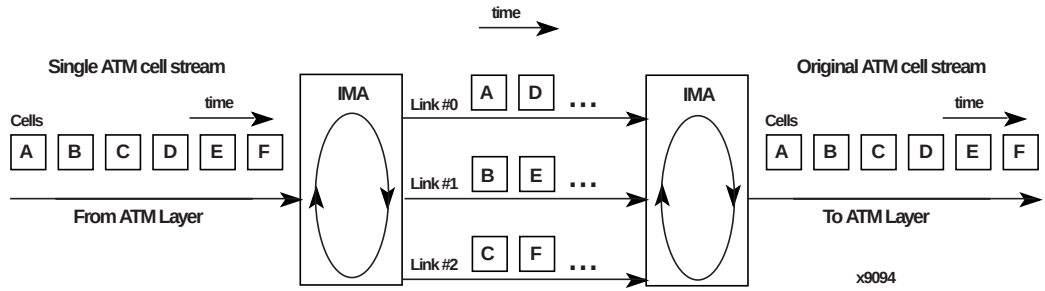

Figure 1: Simplified IMA Diagram

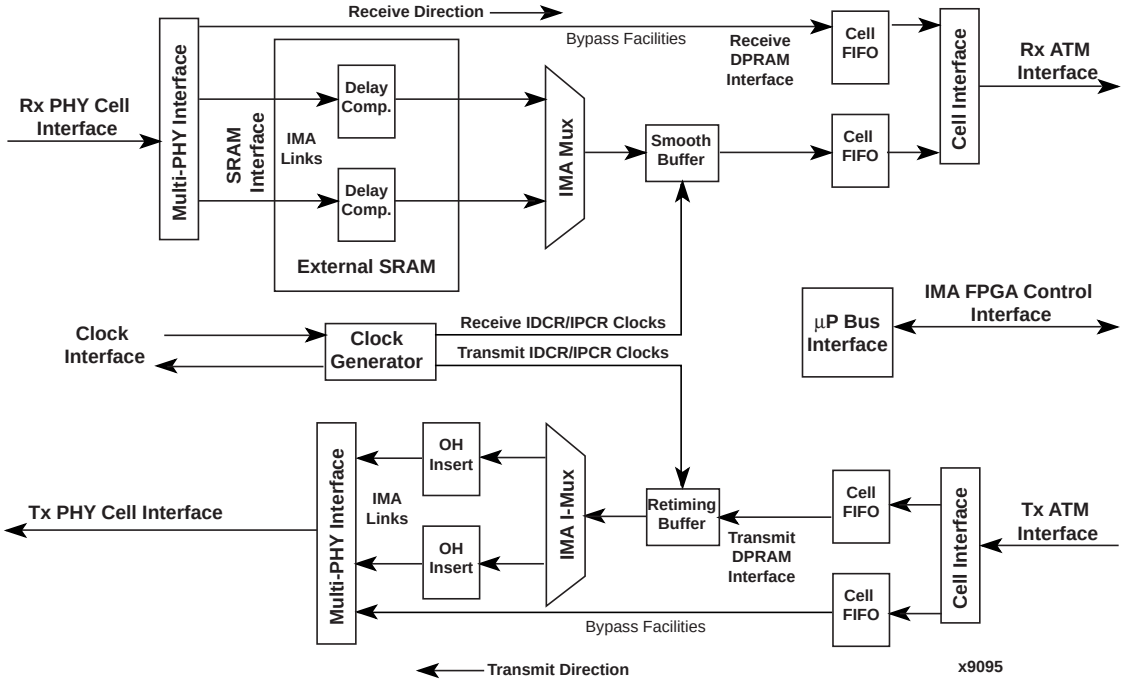

Figure 2: Functional Block Diagram - Detailed

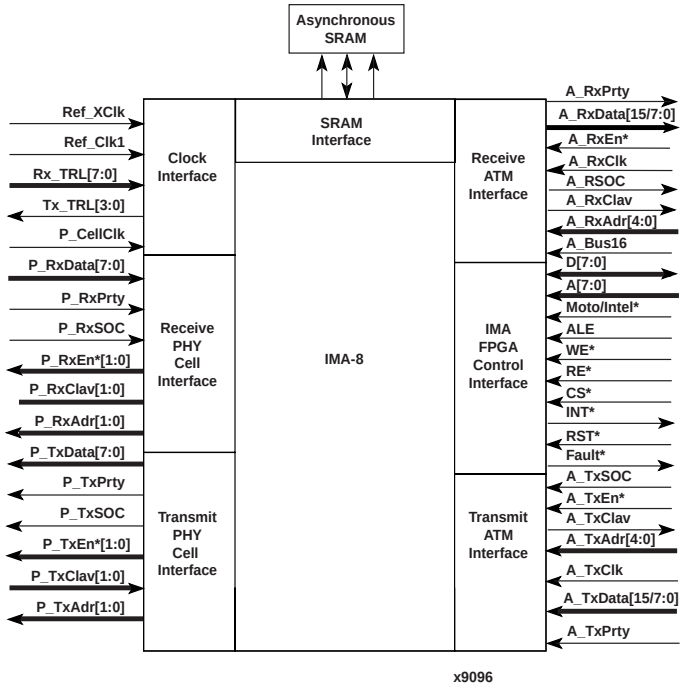

Figure 3: Functional Block Diagram - Overview

Functional Description

The Functional Block diagrams shown in Figure 2 and 3 provide an overview of the IMA implementation, which is composed of four main functional areas: the IMA clock generator, the Transmit IMA processing, the Receive IMA processing, and the Microprocessor Bus Interface.

IMA Clock Generator

The IMA clock generator is responsible for producing the IMA Data Cell Rate (IDCR) and IMA PHY Cell Rate (IPCR) clocks that are used by both the Receive and Transmit IMA Processors. This block allows for significant flexibility in clocking for both the Transmit and Receive IMA Processors.

Transmit IMA Processing

The Transmit IMA Processing section receives ATM cells from the ATM layer via the Utopia Transmit ATM Interface (Tx ATM I/F), which connects directly to internal DPRAMs implemented using the BlockRAM. The Retiming Buffer extracts the received transmit ATM cells to synchronize the data according to the Transit IMA Data Cell Rate (Transmit IDCR) clock. The IMA I-Mux inverse multiplexes the Transit ATM Interface data into the individual IMA links. The OH Insert block generates the IMA frame and inserts the ICP, SICP, and Filler cells for each IMS link. The IMA encoded cell stream is then passed to the Transmit PHY Cell Interface (Tx PHY Cell I/F), which serves as a Utopia Level 2 master to one or multiple PHY devices. These PHY devices encapsulate the ATM cell data for transmission over the T1/E1 facility link. The Transmit IMA Processor also provides Bypass Facilities to allow individual T1/E1 links to operate in a pass-through mode allowing ATM cell data to be passed from the Transmit ATM Interface to the Transmit PHY Cell Interface without IMA processing.

Receive IMA Processing

The Receive IMA Processing section provides inverse operation of the Transmit IMA Processor. The Receive IMA Processor accepts cell streams from multiple T1/E1 links via the Utopia Level 2 Receive PHY Cell Interface (Rx PHY Cell I/F). The Receive PHY Cell Interface data is monitored for IMA framing, and then written to the external SRAM memory via the SRAM I/F. The SRAM memory provides storage for Delay Compensation, which is necessary because of the variable delay paths which occur when receiving ATM cell data over multiple T1/E1 links. The IMA Mux extracts the realigned cell data from the SRAM I/F and removes the IMA control overhead. The cell data is then multiplexed into higher speed ATM cell streams according to the assigned IMA groups. The Smooth Buffer is used to retime the cell data according to the Receive IMA Data Cell Rate (Receive IDCR) clock and then passed to the DPRAM which provides a cell FIFO for the Receive ATM Interface (Rx ATM I/F). The Receive ATM Interface distributes the cells to the ATM layer. The Receive IMA Processor also provides Bypass Facilities to allow individual T1/E1 links to operate in a pass-through mode allowing ATM cell data to be passed from the Receive PHY Cell Interface to the Receive ATM Interface without IMA processing.

Microprocessor Bus Interface

The IMA FPGA Control Interface provides a standard Motorola or Intel compatible microprocessor bus interface for configuration, control, and status. The DRV-IMA software available from Applied Telecom, uses this interface to communicate with the IMA core.

Core Modifications

Since the IMA cores are targeted towards specific Xilinx devices and typically utilize the entire targeted device, it is not recommended that the customer include any significant additional functions in the same device with an IMA core. Please contact Applied Telecom for further information or to discuss additions to the IMA core designs.

Pinout

Applied Telecom's IMA solutions utilize the entire FPGA device and are offered as complete chip solutions for specific device packages. Signal names are shown in the block diagram in Figure 3 and described in Table 1.The IMA-8 pinout diagram in Figure 3 shows that an external asynchronous SRAM device is required for the Spartan-II implementation.

Verification Methods

The IMA core designs have been verified through extensive lab and inter-vendor interoperability testing. The IMA core designs have been incorporated by more than ten companies and have been tested successfully with IMA network equipment products offered by more than ten additional companies.

Core Assumptions

The IMA-8 core fully complies with the ATM forum Inverse Multiplexing for ATM specification versions 1.0 and 1.1.

Recommended Design Experience

Knowledge of ATM technology and ATM Forum specifications is needed.

Available Support Products

Applied Telecom offers the DRV-IMA software program that configures and controls the IMA FPGA core devices to complete the standards compliant IMA implementation. Additionally, an IMA evaluation/test system is available that combines the IMA FPGA based solution with the DRV-IMA software and multiple T1 or E1 facility interfaces.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Clock Interface		
Ref_XClk	Input	IMA Subsystem clock. Most of the IMA logic circuits use this clock (or a derivative of it). It can also be used as a T1/E1 clock. • For E1 facilities, use 49.152 MHz (24 * 2.048 MHz) ± 50 ppm • For T1 facilities, use 37.056 MHz (24 * 1.544 MHz) ± 32 ppm
P_CellClk	Output	Clock signal used for the transfer of Receive and Transmit PHY cells between the PHY device and the IMA FPGA.
Ref_Clk1	Input	Alternate IMA Group Reference Clock. Set to the line rate of the facility type being used.
Rx_TRL[7:0]	Input	Receive Reference Clocks for facility n (where n = 0 to 7). Used for IMA Data Cell Clock generation.
Tx_TRL[3:0]	Output	Transmit Reference Clocks used for the generation of the facility transmit line clock.
Receive and Transmit PHY Cell Interface		
P_RxData[7:0]	Input	Receives 8 bit PHY Cell Data. All received cells are passed to the IMA FPGA.
P_RxPrty	Input	Parity status signal. A parity calculation is performed over P_RxData[7:0] for each clock cycle of P_RxClk. Odd parity is used.
P_RxSOC	Input	Start of Cell synchronization signal for Receive PHY cells. Indicates first byte of the cell placed on the P_RxData[7:0] bus.
P_RxAdr[1:0]	Output	Receive PHY Cell Bus address. Used to identify 1 T1/E1 link in the PHY device. Both address bits may not be used, depending on software configuration.
P_RxEn*[1:0]	Output	Data transfer and output enable for Receive PHY cells. To support different PHY devices, separate enable signals are provided.
P_RxClav[1:0]	Input	Cell Available signals for Receive PHY cells. P_RxClav[n] is Active when one or more complete cells can be transferred from the PHY to the IMA FPGA. To support different PHY devices, separate cell available signals are provided
P_TxData[7:0]	Output	8 bit PHY Cell Data to be sent out the PHY facility. The PHY will append the facility overhead prior to generating the output T1/E1 signal.
P_TxPrty	Output	Parity status signal. A parity calculation is performed over P_TxData[7:0] for each clock cycle of P_TxClk. Odd parity is used.
P_TxSOC	Output	Start of Cell synchronization signal for Transmit PHY cells (Active High). Indicates that the first byte of a cell is being placed on the P_TxData[7:0] bus.
P_TxAdr[1:0]	Output	Transmit PHY Cell Bus address. Used to identify 1 T1/E1 link in the PHY device. Both address bits may not be used, depending on software configuration.
P_TxEn*[1:0]	Output	Data transfer enable for Transmit PHY cells. To support different PHY devices, separate enable signals are provided
P_TxClav[1:0]	Input	Cell Available signals for Transmit ATM cells. When P_TxClav[n] is Active High, the PHY has space available for one or more complete cells. To support different PHY devices, separate cell available signals are provided.
Receive and Transmit ATM Interface		
A_Bus16	Input	Signal which selects the width of the ATM bus for IMA32. When the signal is High, 16 bit UTOPIA operation is enabled. Set this signal Low for 8 bit UTOPIA operation.
A_RxClk	Input	Clock signal used for transfer of Receive ATM cells to the ATM Layer. The maximum clock rate is 33 MHz for IMA32 and its derivatives.
A_RxEn*	Input	Data transfer and output enable for Receive ATM cells. This signal enables transfer of A_RxData[15/7:0] and turns on A_RxSOC and A_RxPrty[0] outputs.

Table 1: Core Signal Pinout (Cont.)

Signal	Signal Direction	Description
A_RxSOC	Tristated output	Start of Cell synchronization signal for Receive ATM cells; indicating the first byte/word of the 53 byte/27 word cell is being placed on the A_RxData[15/7:0] bus.
A_RxAdr[4:0]	Input	Receive ATM Cell Bus address determines the source channel of the Receive ATM cells output from the IMA subsystem and also selects the channel sourcing A_RxClav signal.
A_RxClav	Tristated output	Cell Available signal for Receive ATM cells. When A_RxClav is Active, one or more complete cells can be transferred to the ATM Layer.
A_RxData[15/7:0]	Tristated output	Receive direction ATM side cell data. Bus width depends on A_Bus16.
A_RxPrty	Tristated output	Parity status signal. In 8-bit Utopia mode, a parity calculation is performed over A_RxData[15/7:0] for each clock cycle over A_RxClk. Odd parity is used.
A_TxClk	Input	Clock signal used for transfer of Transmit ATM cells from the ATM Layer. Maximum clock rate is 33 MHz.
A_TxEn*	Input	Data transfer enable for Transmit ATM cells (Active Low); Indicates that the first byte/word of the 53 byte/27 word cell is being placed on the A_TxData[15/7:0] bus.
A_TxSOC	Input	Start of Cell synchronization signal for Transmit ATM cells (Active High); indicating the first byte/word of 53 byte/27 word cell is being placed on the A_TxData[15/7:0] bus.
A_TxAdr[4:0]	Input	Transmit ATM Cell Bus address: determines the destination channel of Transmit ATM cells input to the IMA subsystem and also selects the channel sourcing A_TxClav signal.
A_TxClav	Tristated output	Cell Available signals for Transmit ATM cells. When A_TxClav is Active, one or more complete cells can be transferred from the ATM layer.
A_TxData[15/7:0]	Input	Transmit direction ATM side cell data. Bus width depends on A_Bus16.
A_TxPrty	Input	Parity status signal. In 8-bit Utopia mode, a parity calculation is performed over A_TxData[7:0] for each clock cycle of A_TxClk. Odd parity is used.
Control Interface		
D[7:0]	Input/Output	Data Bus; 8-bit microprocessor interface.
A[7:0]	Input	Microprocessor interface Address Bus. Both multiplexed and non-multiplexed address /data bus applications supported.
Moto/Intel*	Input	Control signal determining the operation of IMA Control Interface. If set High, the IMA FPGA is compatible with typical Motorola microprocessors; if set Low, the IMA FPGA is compatible with typical Intel microprocessors. This signal affects the behavior of RE*, WE*, and CS* signals.
ALE	Input	Address Latch Enable; typically used for multiplexed address/data bus applications.
RE*	Input	Microprocessor bus read enable: only driven in Intel mode.This signal is combined with CS* to define the time that a read operation is valid.
WE*	Input	Microprocessor bus write enable: valid in both Intel and Motorola mode and is combined with CS* to define the time that a write operation is valid
CS*	Input	Microprocessor bus chip select
INT*	Output	Microprocessor bus interrupt request signal
RST*	Input	IMA reset (level sensitive)
Fault*	Input	Status signal indicating a fault has occurred either due to the FPGA failing to configure or due to some fault internal to the IMA implementation in the FPGA

Table 1: Core Signal Pinout (Cont.)

Signal	Signal Direction	Description
Receive Asynchronous SRAM Interface		
R_Sr_Data[7:0]	Input/Output	Receive SRAM Data Bus. ATM cells extracted from the Receive facilities are written into and out of the SRAM for the purpose of differential delay compensation.
R_Sr_Adr[16:0]	Output	Receive SRAM Address Bus. The SRAM address space is defined to accommodate up to 4 times the ATM Forum requirement for differential delay compensation (25 ms) of T1/E1 facilities.
R_Sr_We*	Output	Receive SRAM write enable signal.
R_Sr_Ce*[1:0]	Output	Receive SRAM Device Select control signals. R_Sr_Ce*[0] is the main SRAM select signal and is always used. R_Sr_Ce*[1] may be optional.

1. Signal names with * indicate Active Low signals; all other signals are Active High

Ordering Information

For information on this or other products mentioned in this document, contact Applied Telecom directly using the information provided on the first page.

Related Information

The ATM Forum

The ATM Forum publishes specifications regarding ATM. For more information, contact them as follows:

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