C8250 Universal Asynchronous Receiver/Transmitter

December 5, 2000 Product Specification

CAST, Inc.

5 N. Broadway
Nyack, New York 10960 USA
Phone: +1 845-353-6160
Fax: +1 845-727-7607
E-Mail: info@cast-inc.com
URL: www.cast-inc.com

Features

- Supports Virtex™, Virtex-E and Spartan™-II devices
- Full double buffering
- Asynchronous operation
- Independently controlled Transmit, Line Status, Receive, and Data Set Interrupts
- Programmable data word length (5-8 bit), parity and stop bits
- Parity, overrun, and framing error checking
- Supports up to 1.5 Mbps transmission rates
- Programmable baud rate generator allows division of any reference clock by 1 to (2^{16}-1) and generates an internal 16X clock
- False start bit detection
- Internal diagnostic capabilities
- Peripheral modem control functions
- Intel 80x CPU interface

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core documentation
Design File Formats	.ngo, EDIF netlist, VHDL Source RTL available at extra cost
Constraints File	C8250.ucf
Verification	VHDL test bench
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	VHDL/ Verilog behavioral model
Simulation Tool Used	
1076-compliant VHDL simulator	
Support	
Support provided by CAST, Inc.	

Applications

The C8250 core is used in serial data communications and modem applications.

Table 1: Core Implementation Data

Supported Family	Device Tested	CLB Slices[1]	Clock IOBs[2]	IOBs[2]	Performance (MHz)	Xilinx Tools	Special Features
Virtex-E	V50E-8	163	1	39	98	3.2i	None
Virtex	V50-6	163	1	39	71	3.2i	None
Spartan-II	2S150-6	172	1	39	70	3.2i	None

Notes:
1. Optimized for speed
2. Assuming all core I/Os are routed off-chip

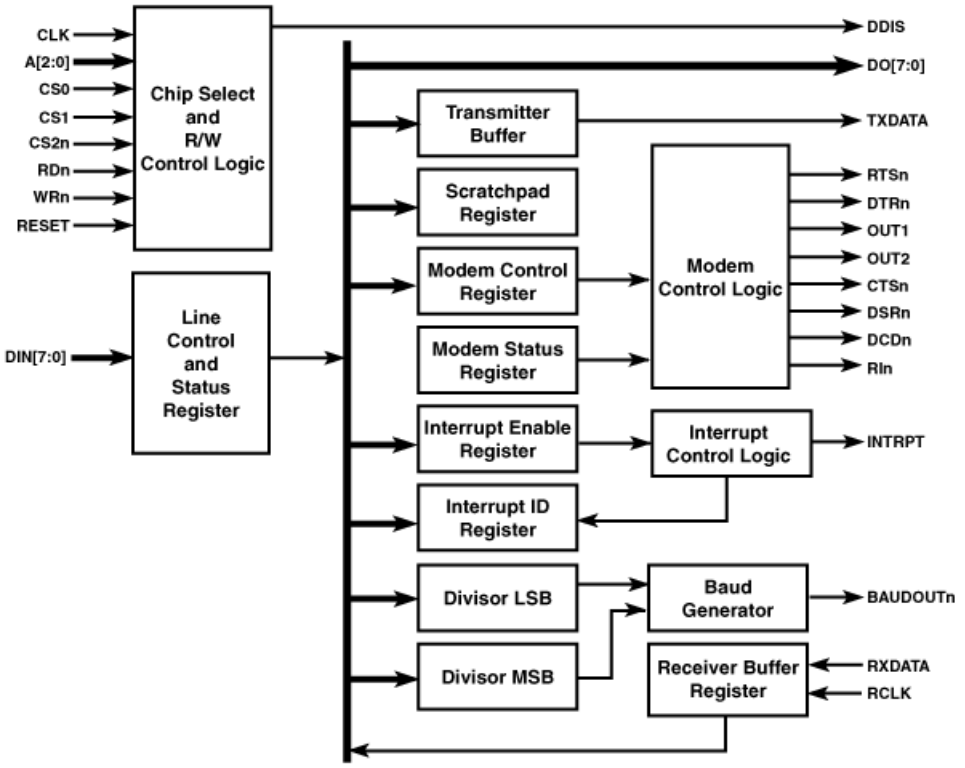

Figure 1: C8250 Universal Asynchronous Receiver/Transmitter Block Diagram

General Description

The C8250 programmable communications interface (UART) core provides data formatting and control to a serial communication channel.

The core has select, read/write, interrupt and bus interface logic features that allow data transfers over an 8-bit I-directional parallel data bus system. With proper formatting and error checking, the core can transmit and receive serial data, supporting both synchronous and asynchronous operation.

Functional Description

The C8250 core is partitioned into modules as shown in Figure 1. The internal structure of the core is shown in Figure 1 and described below.

Chip Select and R/W Control Logic

The chip select and R/W control logic controls the internal chip addressing.

Line Control and Status Register

The Line Control Register is used to specify the data communication format. The break feature, parity, stop bits and word length can be changed by writing to the appropriate bits in LSR.

The Line Status Register provides information on the status of data transfers between the C8250 and the CPU.

Transmitter Buffer

The transmitter buffer section is comprised of a Transmit Holding Register (THR) and a Transmit Shift Register (TSR). Writing to THR will transfer the contents of the data bus DIN[7:0] to the Transmit Holding Register every time that the THR or TSR is empty. This write operation should be done when Transmit Holding Register Empty is set.

Scratchpad (SR)

This register stores the temporary byte for variable use.

Modem Control Register and Modem Control Logic

The register controls the interface lines with the Modem control logic and changes the status of the C8250 from normal operating mode and local loop-back mode (diagnostics mode).

Modem Status Register

This register provides the current state of the modem control lines.

Interrupt Enable Register

The Interrupt Enable Register masks interrupts from the modem status registers, line status, transmitter empty, and receiver ready to the INTRPT output pin.

Interrupt Control Logic

The C8250 contains an interrupt generation and prioritization logic.

When an interrupt is generated, the IIR indicates that an interrupt is pending and also the type of interrupt between various available.

The C8250 provides four prioritized levels of interrupt:

Priority 1 - Receiver line status (highest priority)

Priority 2 -Receiver data ready or receiver character time-out

Priority 3 -Transmitter holding register empty

Priority 4 -Modem Status (lowest priority)

Interrupt Identification Register

The Interrupt Identification Register provides the source of interrupt among four levels of prioritized interrupt conditions in order to minimize the CPU overhead during data transfers.

Baud Generator and LSB and MSB Divisor Registers

The C8250 contains a programmable baud rate generator that takes any clock input from DC-20 MHz and dividing it by any divisor from 1 to (2^{16} - 1). The frequency of output on the BAUDOUTn signal is equal to 16X of the transmission baud rate. The two registers, divisor MSB and divisor LSB, are used to store the divisor in a 16-bit binary format.

Receiver Buffer Register

This register contains the assembled received data. On the falling edge of the start bit, the receiver section starts its operations. The start bit is valid if the RXDATA is still low at the middle sample of Start bit, thus preventing the receiver from assembling a false data character.

Core Modifications

The C8250 core can be customized easily to include:

- Removal of internal baud rate generator
- Different CPU interface (Intel 80x CPU is default)

Please contact CAST directly for any required modifications.

Pinout

The pinout of the C8250 core has not been fixed to specific FPGA I/O, thereby allowing flexibility with a user's application. Signal names are shown in Figure 1 and described in Table 2.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
RESET	Input	External reset
CLK	Input	Master Clock
RCLK	Input	Receive clock
RDn	Input	Read control
WRn	Input	Write Control
CS0	Input	Chip Select 0
CS1	Input	Chip Select 1
CS2n	Input	Chip Select 2
DIN[7:0]	Input	Data Input Bus
CTSn	Input	Clear-to-Send
DSRn	Input	Data Set Ready
DCDn	Input	Data Carrier Detect
RXDATA	Input	Receive Data
RIn	Input	Ring Indicator
A[2:0]	Input	Register Select
D0[7:0]	Output	Data Register Bus
TXDATA	Output	Transmit Data
DDIS	Output	Driver Disable
RTSn	Output	Request-to-Send
DTRn	Output	Data Terminal Ready
OUT1n	Output	Output 1
OUT2n	Output	Output 2
INTRPT	Output	Interrupt
BAUDOUTn	Output	Baud Out

Core Assumptions

- The bi-directional data bus has been split into separate buses: DIN[7:0] and DO[7:0]
- The 11/2 stop bit mode (for 5 bit word length) is not supported
- Signals rd2, wr2, xin, xout, and csout have been eliminated from the interface
- Signal ADSn and address latch removed

Verification Methods

The functionality of the C8250 core has been extensively tested with a VHDL testbench and a large number of test patterns.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

The C8250 is available from Xilinx AllianceCORE partner, CAST Inc. Please contact CAST, Inc. directly for pricing and more information.

The C8250 core is licensed from Moxsyn S.r.l.

Related Information

Data Transmission Circuits 1993 Data Book

Contact:

Texas Instruments
Literature Response Center
P.O. Box 8966
Dallas, TX 7538-9066
URL: http://www.ti.com

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: 408-231-3386 (inside the USA)
408-879-5017 (outside the USA)
Email: literature@xilinx.com