R80515 Microcontroller

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Features

- Reduced instruction cycle enables about 8 times faster performance on average
- 8-bit Control Unit
- 8-bit Arithmetic Logic Unit
- 32-bit Fast Multiplication/Division Unit
- 32-bit Input/Output ports
- Four 16-bit Compare/Capture Unit
- Three 16-bit Timer/Counters
- Two Serial Peripheral Interfaces in full duplex mode
- 15-bit Programmable Watchdog Timer
- Four priority Interrupt Controller
- Internal Data Memory interface can address up to 256 bytes of Read/Write Data Memory Space
- External Memory interface can address up to 64K bytes of External Program Memory Space and up to 64K bytes of External Data Memory Space
- Variable length MOVX instruction to access fast/slow RAM or peripherals
- Special Function Registers (SFR) interface

AllianceCORE™ Facts

| Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core Specification, Instruction Set Details, Test Set Details
Design File Formats	.ngo, EDIF Netlist, VHDL Source RTL available at extra cost
Constraints File	R80515.ucf
Verification	VHDL testbench
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	Example design, assembler programs
Additional Items	Synthesis and simulation scripts
Simulation Tool Used	
1076-Compliant VHDL Simulator, Verilog Simulator	
Support	
Support provided by CAST, Inc.	

Applications

- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

Table 1: Core Implementation Data

Supported Family	Device Tested	CLBs[1]	Clock IOBs[2]	IOBs	Performance (MHz)	Xilinx Tools	Special Features
Virtex-E	V200E-8	2108	1	173	40	M2.1i	None
Virtex	V200-6	2108	1	173	32	M2.1i	None

Notes:
1. Optimized for speed
2. Assuming all core I/Os are routed off-chip
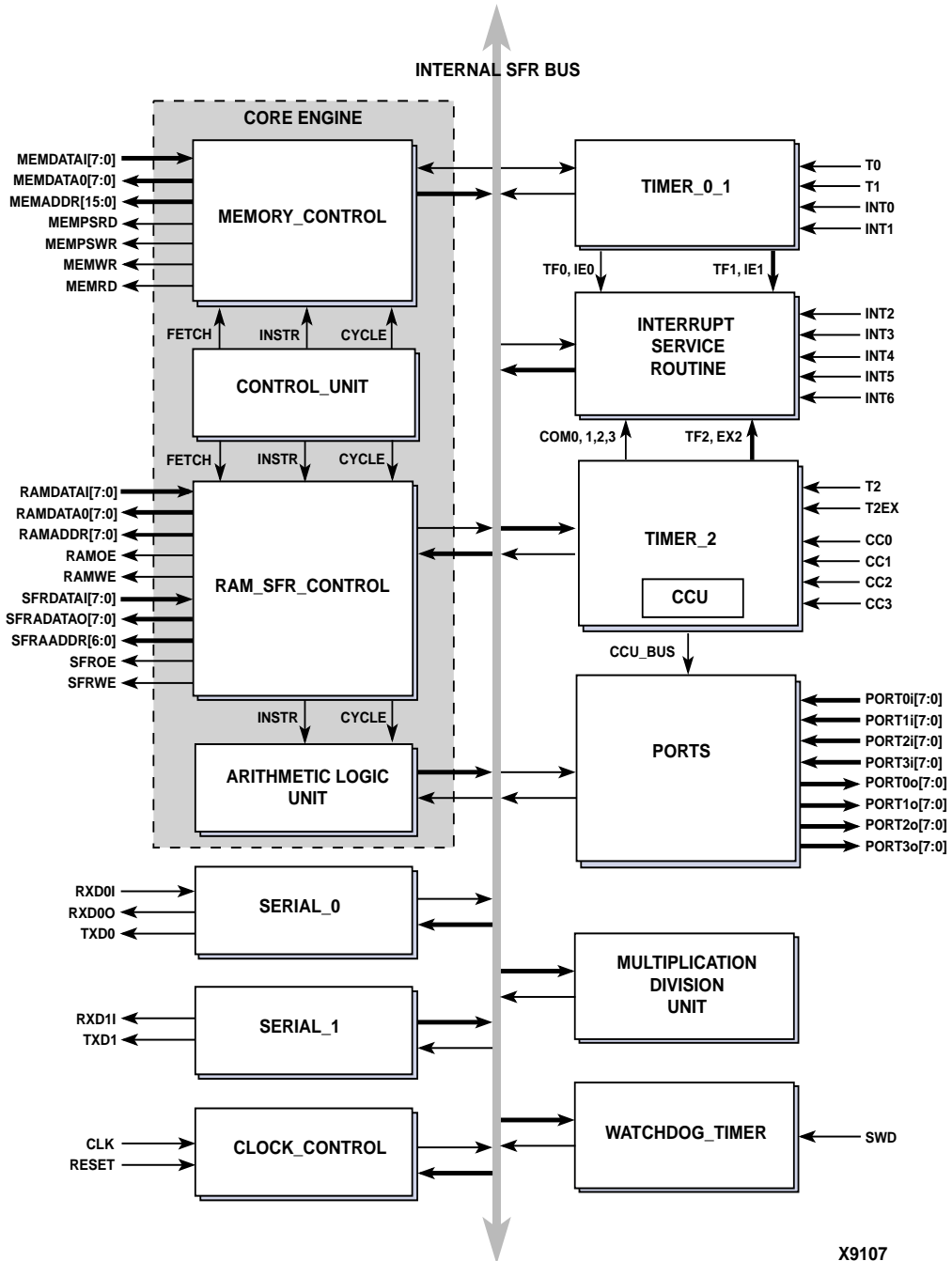
Figure 1: R80515 Microcontroller Block Diagram

General Description

The R80515 is a fast, single-chip, 8-bit microcontroller. It is a fully functional 8-bit embedded controller that executes all ASM51 instructions and has the same instruction set as the 80C51. The R80515 provides software and hardware interrupts; an interface for serial communications, and a timer system with auto-reload resources.

The R80515 is a microcode-free design and is strictly synchronous with positive-edge clocking, a synchronous reset, and no internal tri-states.

The core architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Since a cycle is aligned with memory fetch when possible, most instructions have the same number of cycles as bytes. The R80515 uses 1 clock per cycle. This leads to performance improvement of rate 7.9 (in terms of MIPS) with respect to the legacy 8051 device working at the same clock frequency. The original 8051 had a 12-clock architecture.

Table 2 shows the speed advantage of the R80515 over a standard 8051. A speed advantage of 12 means that the R80515 performs the same instruction three times faster than the standard 8051.

Table 2: Core Speed Average

Speed Advantage	Number Instructions	Number of Op Codes
24	1	1
12	27	83
8	16	38
6	46	91
4.8	1	2
4	18	31
3	2	9
Average: 7.9[1]	Sum: 111	Sum: 225

Note: The actual speed improvement seen in any system will depend on the instruction mix

Functional Description

The R80515 core is partitioned into modules as shown in Figure 1 and described below.

The R80515 core engine is composed of four components:

- Memory Control Unit
- RAM_SFR control unit
- Control Unit
- Arithmetic Logic Unit (ALU)

The R80515 engine allows to fetch instruction from program memory and executes them using RAM or SFR.

Memory Control Unit

- Can address up to 64K bytes of External Program Memory Space

- Can address up to 64K bytes of External Data Memory Space

Control Unit

The Control Unit performs instruction fetch and execution from the Memory Control Unit and the RAM_SFR Control Unit.

RAM_SFR Control Unit

- Can address up to 256 bytes of Read/Write Data Memory Space
- Serves as Interface for off-core Special Function Registers

Arithmetic Logic Unit (ALU)

The ALU performs:

- 8-bit arithmetic operations
- 8-bit logical operations
- Boolean manipulations
- 8 x 8 bit multiplication
- 8 / 8 bit division

Serial _0 and Serial_1

The R80515 core provides two fully independent serial ports for simultaneous communication over two channels. The serials can operate in identical or different modes and communication speeds. Each serial port is capable of both synchronous and asynchronous modes. In synchronous mode, the microcontroller generates the clock and operates in a half-duplex mode. In asynchronous mode, full duplex operation is available. Receive data is buffered in a holding register. This allows the serial ports to receive an incoming word before software has read the previous value.

Each port provides four operating modes. These offer different communication protocols and baud rates:

- Synchronous mode, fixed baud rate
- 8-bit UART mode, variable baud rate
- 9-bit UART mode, fixed baud rate
- 9-bit UART mode, variable baud rate

Clock Control

This unit generates the internal synchronous reset signal. It also contains registers for selecting the clock for the timers and for programming the length of the external data memory accesses.

Timer_0 _1

This block has two timers: Timer_0 and Timer_1, which are nearly identical. Both have four modes:

- 13-bit Timer/counter
- 16-bit Timer/counter
- 8-bit timer/counter with auto reload
- Two 8-bit timers (Timer_0 only)

Each timer can also serve as a counter of external pulses (1 to 0 transition) on the corresponding T0 or T1 pin. The T0 and T1 pins are input through signals of the P3i bus of the Ports block. The user can gate the timer/counter using an external control signal. This allows the timer to measure the pulse width of external signals.

Interrupt Service Routine

The R80515 core provides a three-priority interrupt system. There are 14 interrupt sources. Each source has an independent priority bit, flag, interrupt vector, and enable. In addition, interrupts can be globally enabled or disabled.

Timer 2

Timer 2 can operate as timer, event counter, or gated timer.

In the Timer mode, Timer 2 can by incremented every machine cycle, or every second machine cycle, depending on the 2:1 prescaler.

In the Event counter mode, Timer 2 is incremented when the external signal T2 changes value from 1 to 0. The T2 input is sampled every machine cycle. Timer 2 is incremented in the cycle following the one in which the transition was detected.

In gated timer mode, the internal clock which increments timer 2 is gated by the external signal T2.

Reload of Timer 2 can be executed in two modes:

- Mode 0: Reload signal is generated by Timer 2 overflow - auto reload
- Mode 1: Reload signal is generated by a negative transition at the corresponding input of pin T2ex

Compare/Capture Unit (CCU)

The CCU performs compare and capture functions.

In Compare function, the value stored in the four 16-bit compare/capture registers is compared with the contents of the Timer 2 register.

In Capture function, the actual timer/counter contents can be saved into one of four 16-bit registers upon an external event (mode 0) or a software write operation (mode 1).

Ports

The R80515 provides four I/O ports. Port0 to Port3 are 8-bit bi-directional I/O ports with separated inputs and outputs.

Port0 serves as the multiplexed low-order address and data bus during accesses to external program and data memories.

Port1 serves the special features, such as, external interrupt inputs, Serial 1 interface, and Timer 2 inputs.

Port2 provides the high-order address byte during fetches from external program memory that use 16-bit addresses.

Port3 serves the special features, such as, read and write strobes for external data memory, Timer_0 and Timer_1 inputs.

Multiplication Division Unit (MDU)

This on-chip arithmetic unit provides:

- 16x16 bit multiplication
- 32/16 bit division
- 16/16 bit division
- 32-bit normalization
- 32-bit left/right shifting

All operations are unsigned integer operations.

The multiplication/division unit allows operations concurrently to, and independent, of the core engine activity.

Operation of the MDU consist of three phases:

- Loading the operand registers
- Executing calculation
- Reading the result from the result registers

Watchdog Timer

The Watchdog Timer is a user programmable clock counter that can serve as a time-base generator, an event timer, or a system supervisor. The timer is driven by the main system clock that is supplied to a series of dividers. The watchdog counter has 15-bit width. The divider output is selectable, and determines the interval between time-outs. When a time-out is reached, an interrupt flag will be set, and if enabled, a reset will occur. The interrupt flag will cause an interrupt to occur, if its individual enable bit is set and the global interrupt enable is set.

Core Modifications

The R80515 core can be modified to include features such as realtime clock.

Please contact CAST, Inc. directly for any required modifications.

Verification Methods

The functionality of the R80515 core was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 chip and the results compared with the core's simulation outputs.

Pinout

The pinout of the R80515 core has not been fixed to specific FPGA I/O, thereby, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1 and described in Table 3.

Table 3: Core Signal Pinout

Signal	Signal Direction	Description
Internal Program Memory Interface		
MEMDATAI[7:0]	Input	Memory data input
MEMDATAO[7:0]	Output	Memory data output
MEMADDR[15:0]	Output	Data File Address
MEMPSRD	Output	Program Store Read
MEMPSWR	Output	Program Store Write Enable
MEMWR	Output	Data Memory Write Enable
MEMRD	Output	Data Memory Read Enable
Internal Data Memory Interface		
RAMDATAI[7:0]	Input	Data Bus Input
RAMDATAO[7:0]	Output	Data Bus Output
RAMADDR[7:0]	Output	Data File Address
RAMOE	Output	Data File Output Enable
RAMWE	Output	Data File Write Enable
SFRDATAI[7:0]	Input	SFR Data Bus Input
SFRDATAO[7:0]	Output	SFR Data Bus Output
SFADDR[6:0]	Output	SFR Address
SFROE	Output	SFR Output Enable
SFRWE	Output	SFR Write Enable
Serial Ports		
RXD0I	Input	Serial 0 Receive Data
RXD0O	Output	Serial 0 Receive Clock
TXD0	Output	Serial 0 Transmit Data
RXD1I	Input	Serial 1 Receive Data
TXD1	Output	Serial 1 Transmit Data
Clock_Control		
CLK	Input	Clock
RESET	Input	Hardware Reset Input
Timer_0_1		
T0	Input	Timer 0 External Input
T1	Input	Timer 1 External Input
INTO	Input	External Interrupt 0
INT1	Input	External Interrupt 1
Interrupt Service Routine		
INT2	Input	External Interrupt 2
INT3	Input	External Interrupt 3
INT4	Input	External Interrupt 4
INT5	Input	External Interrupt 5
INT6	Input	External Interrupt 6
Timer_2		
T2	Input	Timer 2 External Input
T2EX	Input	Timer 2 Capture Trigger
CC0	Input	Compare/Capture0
CC1	Input	Compare/Capture1

Table 3: Core Signal Pinout (Cont)

Signal	Signal Direction	Description
CC2	Input	Compare/Capture2
CC3	Input	Compare/Capture3
Ports		
PORT0I[7:0]	Input	Port 0
PORT1I[7:0]	Input	Port 1
PORT2I[7:0]	Input	Port 2
PORT3I[7:0]	Input	Port 3
PORT0O[7:0]	Output	Port 0
PORT1O[7:0]	Output	Port 1
PORT2O[7:0]	Output	Port 2
PORT3O[7:0]	Output	Port 3
Watchdog_Timer		
SWD	Input	Start Watchdog Timer

Recommended Design Experience

The user must be familiar with HDL design methodology, as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available from the AllianceCORE™ partner listed on the first page. Please contact the partner for pricing and more information.

The R80515 core is licensed from Evatronix S.A.

Related Information

- *High-Speed Microcontroller Data Book*, Dallas Semiconductor, 1995.
- *CMOS Single-chip 8-bit Microcontrollers*, Philips, 1996.
- *Addendum to the MCS®51 Microcontroller Family,* Intel, 1996.
- *8-bit Embedded Controllers*, Intel, 1990
- *SAB 80515/80C515, 8-Bit Single-Chip Microcontroller Family, User's Manual, Siemens, 1995*
- *SAB 80C517/80C537, 8-Bit CMOS Single-Chip Microcontroller, User's Manual, Siemens, 1994*

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