



CSELT S.p.A

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Features

- Supports Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Distributed sample descrambler for cell-based data transmission
- Customizable VHDL source code available, allowing generation of different netlist versions
- Can implement ITU-T I.432 descrambler for standard 53-bit ATM cells
- Can implement custom descrambler for proprietary format ATM cells
- Customized testbench for pre- and post-synthesis verification supplied with the module
- Core customization:
 - 8/16 bits interface data width
 - ATM cell length
 - ATM cell header length and position
 - Feedback and output polynomials of the descrambling sequence generator
 - Reset value of the descrambling sequence generator

Applications

- Physical layer ATM circuits

AllianceCORE™ Facts		
Core Specifics ¹		
Supported Family	Spartan	Virtex
Device Tested	S05-3	V50-6
CLB Slices ²	97	109
Clock IOBs	1	1
IOBs ³	28	28
Performance (MHz)	42	74
Xilinx Tools	M1.5i/M2.1i	M1.5i/M2.1i
Special Features	None	None
Provided with Core		
Documentation	User Manual	
Design File Formats	EDIF netlist, XNF netlist, VHDL source available extra	
Constraints File	TOP_DSD_nl.ncf	
Verification	VHDL testbench	
Instantiation Templates	VHDL, Verilog	
Reference Designs & Application Notes	None	
Additional Items	None	
Simulation Tool Used		
Synopsys VSS		
Support		
Design and customization support provided by CSELT		

Notes:

- Data refer to the following customization:
 - 8-bit interface
 - 53 byte ATM cell
 - ATM cell header from byte 1 to 5 inclusive
 - Descrambling sequence generator with: feedback polynomial = $x^{31}+x^{28}+1$, output polynomial = $x^{31}+x^{28}$, reset value = 1
- Utilization numbers for Virtex are in CLB slices
- Assuming all core I/Os are routed off-chip

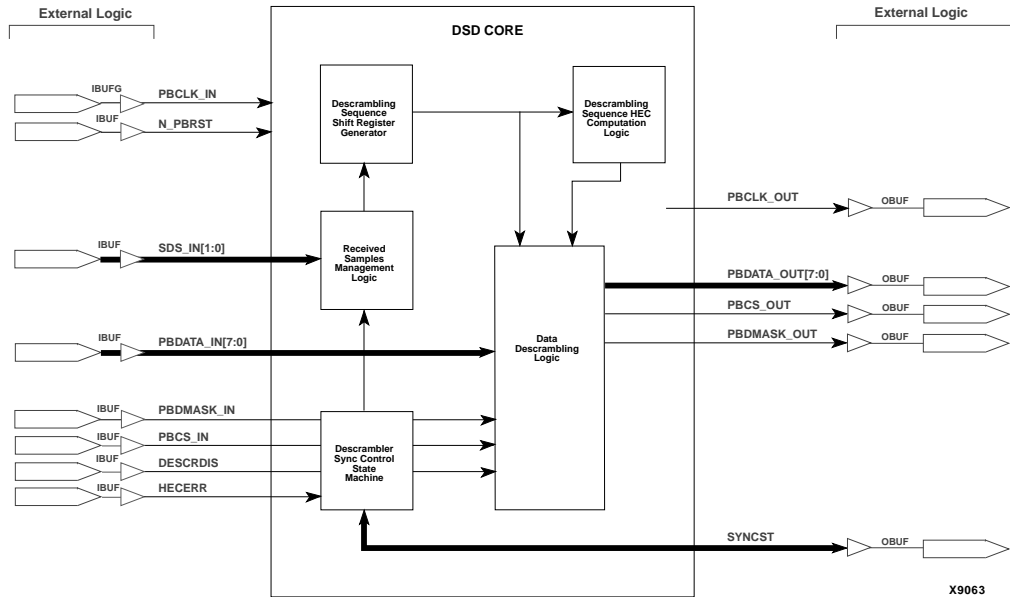


Figure 1: DSD Block Diagram

General Description

The Distributed Sample Descrambler (DSD) core decodes a scrambled ATM cell stream by modulo-2 addition of the cell bits with a pseudo-random sequence identical to, and synchronized with the sequence used by the scrambler for encoding the stream. This core is the companion of the Distributed Sample Scrambler (DSS) core, which encodes a cell-based stream by modulo-2 addition of the cell bits with a pseudo-random sequence.

To allow synchronization of the descrambler to the scrambler, samples of the scrambling sequence are sent from the DSS to the DSD. In this implementation, two sequence samples, taken at half-cell distance are carried by the two most significant bits of the Header Error Correction (HEC) field of each ATM cell. While acquiring synchronization, the descrambler compares each received sample to its locally generated counterpart, and performs a correction of the descrambling sequence generator state whenever the two samples differ. After synchronization has been acquired, sample comparison continues for verification purposes, but no further generator state correction is performed.

The Absolute Maximum ratings, Operating Conditions, DC Electrical Specifications and Capacitances depend on the Xilinx device selected for implementation and can be retrieved from the corresponding Xilinx datasheet.

Functional Description

The internal architecture of the DSD core is shown in Figure 1. A brief description of the operation of each module follows.

Descrambler Sync Control State Machine

The Descrambler Sync Control State Machine handles the phase synchronization process of the Descrambling Sequence Shift Register Generator (SRG). The FSM controls the SRG correction process and signals the current synchronization status on the SYNCST outputs.

Received Samples Management Logic

The Received Samples Management Logic handles the scrambling sequence samples received through the SDS_IN input. New samples are expected on each input data word that carries a cell HEC field.

This logic also handles the storage of samples of the bit sequence generated by the Descrambling Sequence SRG. Samples are taken at half-cell distance, from the same position in the sequence as those forwarded by the scrambler.

Descrambling Sequence Shift Register Generator

The Descrambling Sequence SRG generates the descrambling sequence for the received input data stream. The generator, a linear feedback shift register with customizable length, feedback logic and output generation logic, produces one descrambling sequence word per clock cycle. SRG correction performed by modulo-2 addition of a pre-computed correction vector to the SRG register content, takes place at times specified by the Sequence Samples Management Logic (when correction is enabled by the Descrambler Sync Control FSM), if the received scrambling sequence sample does not match the corresponding locally generated sample.

Descrambling Sequence HEC Computation Logic

The Descrambling Sequence HEC Computation Logic computes the Header Error Control codeword corresponding to the cell header descrambling sequence. The computed codeword is forwarded to the Data Descrambling Logic block.

Data Descrambling Logic

The Data Descrambling Logic selects the appropriate descrambling data and generates output data as the modulo-2 sum of descrambling data and input data. The selected descrambling data is the descrambling sequence data from the Descrambling Sequence SRG for every cell byte excluding the HEC. For the HEC byte, the selected descrambling data is the HEC CRC of the header descrambling data sequence (from the Descrambling Sequence HEC Computation logic block). Also, the appropriate two bit samples of the descrambling sequence are added modulo-2, to the two most significant bits of the result.

Pinout

Pinout of the core has not been fixed to specific FPGA I/O allowing flexibility with a user's application. Signal names for this core are shown in Figure 1 and described in Table 1.

Core Modifications

CSELT provides netlist customized to user's requirements. The DSD core is parametric. Parameters shown in Table 2 are implemented as a set of generics in the synthesizable VHDL source code of the core. Parameters allow the user to specify some architectural and functional features, so as to customize the netlist to a specific design or application.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Input Interface		
PBCLK_IN	Input	Data clock
PBDATA_IN [7:0]	Input	Data input; port size can be 8/16 bits based on DMODE generic
PBDMASK_IN	Input	Data mask
PBCS_IN	Input	Start of cell flag
Output Interface		
PBCLK_OUT	Output	Data clock
PBDATA_OUT [7:0]	Output	Data output; port size can be 8/16 bits based on DMODE generic
PBCS_OUT	Output	Start of cell flag
PBDMASK_OUT	Output	Data mask
Control and Status Ports		
N_PBRST	Input	Reset
SDS_IN [1:0]	Input	Scrambler data samples
DESCRDIS	Input	Descrambler disable
HECERR	Input	HEC error flag
SYNCST [1:0]	Output	Descrambler synchronization status

Table 2: Core Parameters (VHDL Generics)

Parameter	Description
DMODE	Data transfer mode (8/16 bit)
NBYTES	ATM cell size (in bytes)
HECFIRST	First cell byte covered by the HEC field
HECLAST	Last cell byte covered by the HEC field (also, HEC field byte)
SRGDEG	Degree of the SRG feedback polynomial
SRGPOL	Binary coefficients of the SRG feedback polynomial
SRGRVAL	SRG reset value
SCRPOL	Binary coefficients of the scrambling sequence generation polynomial

Verification Methods

Extensive functional (pre-synthesis) and timing (post-synthesis) simulation has been performed for different values of the core parameters, using the Synopsys VSS simulator. Simulation scenarios (including data and command files) and parametric test bench used for design verification are provided with the core.

The parametric test bench is composed of a programmable ATM cell generator. The generated cell stream is customized; cell generation commands are read from a text file. Cell stream customizability includes header data, (random or user-defined), payload data (random, counter, fixed or user-defined), period and size of transmission holes, error injection (data errors, cell length errors).

Recommended Design Experience

Experience with the Xilinx design flow and ATM transmission system design is recommended to the users of the netlist version of the core. For the source code version, users should also be familiar with the Synopsys FPGA synthesis tools (VHDL Compiler, FPGA Compiler) and simulator (VSS).

Available Support Products

A copy of the ITU-T Recommendation I.432 *B-ISDN User-Network Interface – Physical Layer Specification* can be purchased from the International Telecommunication Union. Contact:

International Telecommunication Union
Sales and Marketing Service
Place des Nations
CH -1211 Geneva 20, Switzerland
Phone: +41 22 730 6141
Fax: +41 22 730 5194
E-mail: sales@itu.int
URL: www.itu.int/publications

Ordering Information

The DSD core is provided under license by CSELT S.p.A for use in Xilinx programmable logic devices. Please contact CSELT S.p.A for information about pricing, terms and conditions of sale.

CSELT S.p.A reserves the right to change any specification detailed in this document at any time without notice, and assumes no responsibility for any error in this document.

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logiccore/alliance/tblpart.htm



DSD Implementation Request Form

To: CSELT S.p.A.
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 E-mail: viplibrary@cse.lt

CSELT configures and ships Xilinx netlist versions of the DSD core customized to your specification. Please fill out and fax this form so that CSELT can respond with an appropriate quotation that includes performance and density metrics for the target Xilinx FPGA.

Implementation Issues

1. Data transfer mode (8 bit / 16 bit):

2. Cell size (bytes):

3. First cell byte covered by the HEC:

4. HEC byte position:

5. SRG feedback polynomial:

6. SRG reset value:

7. Scrambling sequence generation polynomial:

8. Reset mode (sync/async):

From: _____
 Company: _____
 Address: _____
 City, State, Zip: _____
 Country: _____
 Phone: _____
 FAX: _____
 E-mail: _____

Business Issues

1. Indicate timescales of requirement:
 _____ date for decision
 _____ date for placing order
 _____ date of delivery

2. Indicate your area of responsibility:
 _____ decision maker
 _____ budget holder
 _____ recommender

3. Has a budget been allocated for the purchase?
 Yes _____ No _____

4. What volume do you expect to ship of the product that will use this core? _____

5. What major factors will influence your decision?
 _____ cost
 _____ customization
 _____ testing
 _____ implementation size

6. Are you considering any other solutions?