# EP201 PowerPC Bus Master

December 5, 2000 Product Specification


## Eureka Technology, Inc.

4962 El Camino Real, Suite 108
Los Altos, CA 94022 USA
Phone: +1 650-960-3800
Fax: +1 650-960-3805
E-Mail: info@eurekatech.com
URL: www.eurekatech.com


## Features

- Fully supports PowerPC™ 60x bus protocol, including PowerPC 603, 604, 740, 750 and 8260
- Automatic bus arbitration for address bus and data bus based on internal bus request
- Separate address bus and data bus tenure with individual grant signals
- Supports address bus retry and data transfer error
- Qualified address bus grant and data bus grant through the use of bus busy signals
- User specified burst data transfer and single beat data transfer
- Supports two back-end user request ports with automatic arbitration
- Efficient back-end bus for internal data transfer
- Supports bus parking

## Applications

The PowerPC bus slave is used in a wide variety of fields. The following are just a few examples:

- Defense
- Medical
- Communication
- Any peripheral device using PowerPC microprocessor

## AllianceCORE™ Facts

| Core Specifics | |
|---|---|
| Supported Family | Virtex |
| Device Tested | V400-6 |
| CLB Slices | 139 |
| Clock IOBs[1] | 1 |
| IOBs[1] | 333 |
| Performance (MHz) | 80 |
| Xilinx Tools | 3.2i |
| Special Features | None |
| **Provided with Core** | |
| Documentation | User guide |
| Design File Formats | EDIF netlist |
| Constraints File | Top201.ucf |
| Verification | VHDL or Verilog test bench |
| Instantiation Templates | VHDL, Verilog |
| Reference designs & application notes | None |
| Additional Items | None |
| **Simulation Tool Used** | |
| Model Technology Modelsim™ 5.4b | |
| **Support** | |
| Support provided by Eureka Technology | |

Notes:
1. Assuming all core I/Os are routed off-chip

## General Description

The PowerPC bus master is a bus interface unit designed for the PowerPC host bus. It is designed to work on any 60x compliant bus architecture. It performs all the data transfer functions necessary for any master device reside directly on the PowerPC host bus. It supports separate arbitration for the address bus and data bus to improve bus performance.

Single beat and burst data transfer are supported. Different data size and transfer types are allowed and can be specified through an internal back-end bus. The back-end bus provides a very simple interface to the internal logic to initiate bus operations.

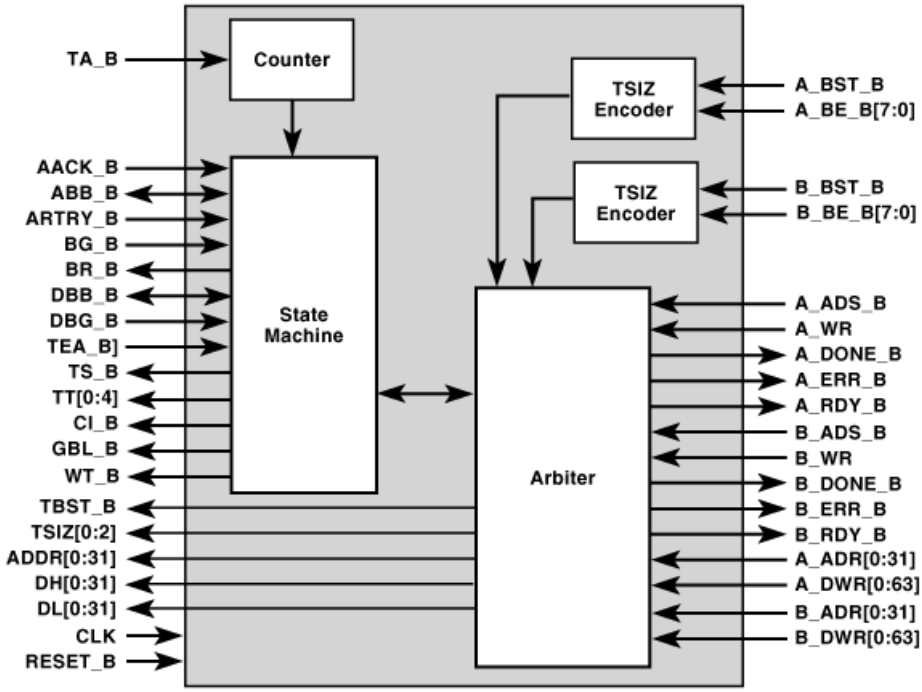


**Figure 1: EP201 PowerPC Bus Master Block Diagram**

## Functional Description

The PowerPC master device performs the complex address and data tenure of the PowerPC host bus from the simple user interface. The following is a brief description of each individual block with respect to Figure 1.

### Arbiter

The two backend bus requests A_ADS_B and B_ADS_B need to go to the arbiter to decide which request is to be served first. The arbiter used in the PowerPC bus master is on first-come first-serve basis. If both requests are received at the same cycle, the arbiter will give the previously served requestor a lower priority. The information will then pass to the state machine. The address and data bus go directly to the PowerPC bus from the arbiter.

### TSIZ Encoder

A TSIZ encoder is used for each backend requestor to determine the information of TBST_B and TSIZ[0:2] based on BST_B and BE_B[0:7]. This information will then go to the arbiter before it goes to the PowerPC bus.

### State Machine

The state machine will be triggered whenever it receives a request from the arbiter in idle state. Then it will follow the PowerPC bus protocol to initiate a request to the PowerPC bus. Once the data transfer is completed or there is an abnormal termination, the state machine will go back to idle.

### Counter

This counter helps to inform the state machine when the data transfer is completed so that the state machine can go back to idle.

## Pinout

The pinout of the EP201 core has not been fixed to specific FPGA I/O, thereby allowing flexibility with a user's application. Signal names are shown in Figure 1 and described in Table 2.

## Core Modifications

The PowerPC bus master is designed in XCV400FG676 FPGA. Cores for other packages can also be supported. Eureka Technology will contract to modify the core to your specifications.

## Verification Methods

Functional simulation has been done using Model Technology ModelsimTM 5.4b. Static timing analysis has been done for all paths using the timing analyzer in Xilinx Foundation Series 3.2i.

## Recommended Design Experience

Users should decide the target device and there is no requirement in using the PowerPC bus master core.

## Ordering Information

If you have inquiries or want to license our core, please contact Eureka Technology directly. Eureka Technology retains the right to make changes to these specifications at any time without notice.

Phone : (650)960 3800
Email : info@eurekatech.com

## Related Information

### Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: 408-231-3386 (inside the USA)
408-879-5017 (outside the USA)
Email: literature@xilinx.com

**Table 1: Core Signal Pinout**

| Signal | Signal Direction | Description |
|---|---|---|
| A_ADR[0:28] | Input | Port A Address |
| A_ADS_B | Input | Port A address strobe |
| A_BST_B | Input | Port A burst request |
| A_BE_B]0:7] | Input | Port A byte enable |
| A_DONE_B | Output | Port operation done |
| A_DWR[0:63] | Input | Port A write data |
| A_ERR_B | Output | Port A operation error |
| A_RDY_B | Output | Port A transfer ready |
| A_WR | Input | Port A write/read request |
| B_ADR[0:28] | Input | Port B address |
| B_ADS_B | Input | Port A address strobe |
| B_BST_B | Input | Port A burst request |
| B_BE_B[0:7] | Input | Port A byte enable |
| B_DONE_B | Output | Port operation done |
| B_DWR[0:63] | Input | Port A write data |
| B_ERR_B | Output | Port A operation error |
| B_RDY_B | Output | Port A transfer ready |
| B_WR | Input | Port A write/read request |
| AACK_B | Input | Address acknowledge |
| ABB_B | Input/Outpout | Address busy busy |
| ADDR[0:31] | Output | PowerPC bus address |
| ARTRY_B | Input | Address retry |
| BG_B | Input | Bus grant |
| BR_B | Output | Bus request |
| CI_B | Output | Cache inhibit |
| CLK | Input | System clock |
| DBB_B | Input/output | Data bus busy |
| DBG_B | Input | Data bus grant |
| DH[0:31] | Output | PowerPC bus data high |
| DL[0:31] | Output | PowerPC bus data low |
| GBLB | Output | Global |
| RESET_B | Input | System reset |
| TA_B | Input | Transfer acknowledge |
| TBST_B | Output | Transfer Burst |
| TEA_B | Input | Transfer error acknowledge |
| TS_B | Output | Transfer start |
| TSIZ[0:2] | Output | Transfer size |
| TT[0:4] | Output | Transfer type |
| WT_B | Output | Wrote through |