GV & Associates, Inc.

23540 Oriente Way
Ramona, CA 92065 USA
Phone: +1 760-789-7015
Fax: +1 760-789-7015
E-mail: loop@gvassociates.com
Web: www.gvassociates.com

Features

- 65 MHz maximum input A/D sample rate
- Dedicated A/D and D/A FPGA
- Dedicated External Communication FPGA
- Secondary Processing FPGA
- 5V CMOS Tolerant 86-bit External I/O
- FPGA Logic Expansion (50K to 1M gates)
- Each FPGA has a Dedicated 256K x 18 ZBT SRAM
- Up to 393,216 bits of internal Block RAM

- Eight Delay Locked Loops (DLL)
- 40-bit FPGA Local Bus
- Slave Serial and Download Cable (Model DLC4) Configurable
- 120 MHz maximum output D/A sample rate
- Separate FPGA Power Plane for Power Measurement
- External 1.8V Jack for High Current FPGAs
- Programmable A/D Sample Clock
- On-board 65 MHz Clock Oscillator
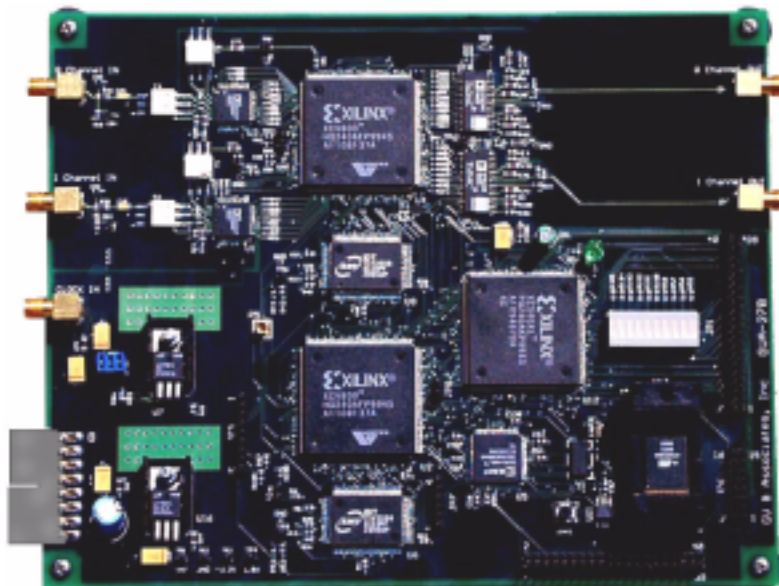- External High Stability Clock Input
-

Figure 1:   GVA-270 Revision A Virtex-E DSP Hardware Accelerator

General Description

The GVA-270 Digital Signal Processing Hardware Accelerator is designed for the implementation of complex DSP or other channel coding designs. This platform provides a highly flexible environment for the integration of various software and hardware DSP applications using the Xilinx Virtex™-E FPGA family.

The GVA-270 supports the following Xilinx Virtex-E and Virtex FPGAs:

Virtex-E	Virtex
XCV50E-6PQ240C	XCV50-6PQ240C
XCV100E-6PQ240C	XCV100-6PQ240C
XCV200E-6PQ240C	XCV200-6PQ240C
XCV300E-6PQ240C	XCV300-6PQ240C
XCV400E-6HQ240C	XCV400-6HQ240C
XCV600E-6HQ240C	XCV800-6HQ240C
XCV1000E-6HQ240C	

Functional Description

The general configuration of the platform consists of an I and a Q channel which are digitized by two 12-bit A/D converters. The sample rate (maximum of 65 MHz) of the A/D is programmable, since it is generated by the Xilinx FPGA. The digitized signals are now ready to be processed by the customer's algorithm that is implemented in hardware by either of the two Xilinx FPGAs. Once the signals have been processed, a 120 MSPS D/A via the Xilinx FPGA can convert them back to an analog waveform. The processed data may also be sent to the external data port. The analog signal is connected to a 50 ohm SMA output for viewing

The Xilinx FPGA has access to an external 256K x 18 ZBT SRAM that could be used for temporary data storage. Each Xilinx FPGA has up to 393,216 bits of internal Block RAM.

The Virtex/Virtex-E FPGA used for analog control may be accessed by the data processing Virtex/Virtex-E FPGA via a 40-bit local bus. An 84-bit bus also connects the data processing FPGA to a SpartanXL FPGA.

The Spartan XL FPGA, XCS40XL-4QC240C, is used primarily to provide a 5V CMOS tolerant interface between the Virtex-E FPGAs and other external devices. However, this FPGA could be used for additional processing as determined by the user.

The Xilinx FPGAs may also access unused address space in the configuration EPROM by interfacing to the CPLD via the local bus. Using the 86 bit external bus interface, the GVA-270 could be configured to have an off-board interface to an external processor such as a TMS320C31 or other Digital Signal Processor; or the GVA-270 could use the 86-bit bus for the direct transfer of data between the on-board FPGAs and other external devices. For non-specific clock requirements, an external clock source is available. Each

Xilinx FPGA has eight Delay Locked Loops (DLL) for system clock synchronization.

Ordering Information

This product is available directly from GV & Associates. Please contact them for pricing and more information.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
               +1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/ tblpart.htm
URL: www.xilinx.com/products/logicore/alliance/ tblpart.htm
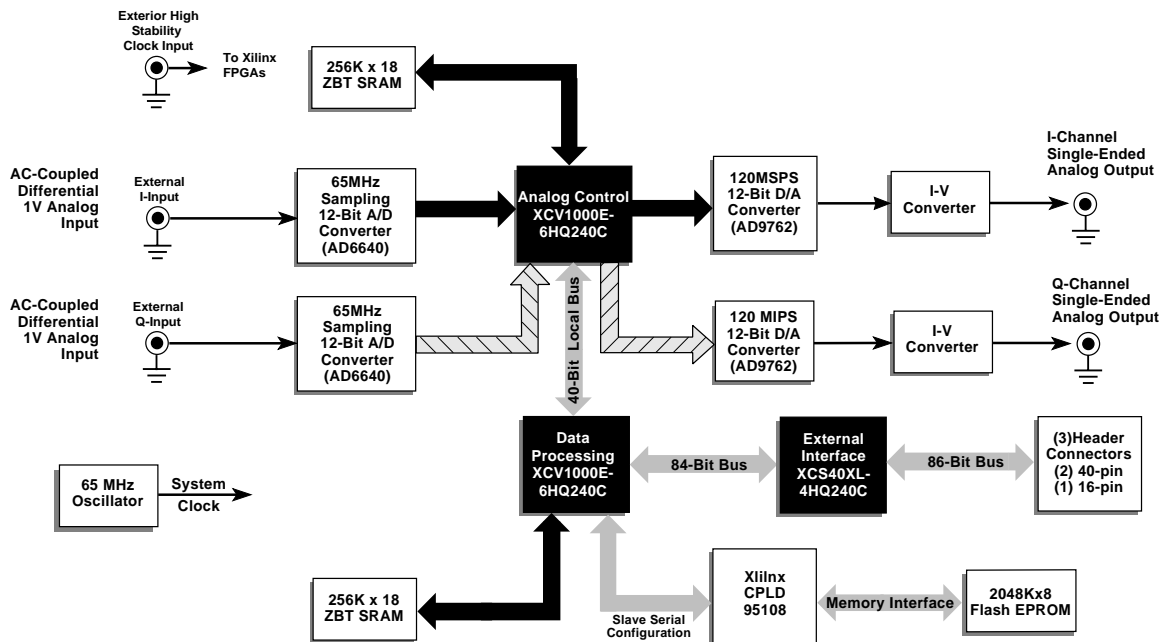
Figure 2: GVA-270 Revision A Virtex-E FPGA Block Diagram