XF-RSDEC Reed Solomon Decoder

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Memec Design Services

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Features

- Supports 4000X, Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Core design is customized using the following specifications:
  - Primitive polynomial
  - Generator polynomial
  - Message and codeword length (fixed or variable)
  - Number of parity symbols (fixed or variable)

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core Documentation, User Guide, Sample Design
Design File Formats	VHDL/Verilog RTL source files
Constraints File	.ucf
Verification	VHDL/Verilog Testbench Test vector files
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	Sample Implementation in VHDL or Verilog
Additional Items	Warranty by MDS
Simulation Tool Used	
Model Technology, Silos	
Support	
Support provided by Memec Design Services.	

Table 1: Example Implementations

	XF-RSDEC-INTELSAT Example #1	XF-RSDEC Example #2	XF-RSDEC Example #3
Parity Symbols	14,16,18,20	4	4
Bits/Symbol	m=8	m=8	m=8
Erasure	Yes	No	No
Supported Family	Virtex	Virtex	4000
Device Tested	V50-4	V50-6	4036XL-1
CLBs: Core	684[2]	636[2]	729
CLBs: Core +Ext Logic	684[2]	636[2]	729
IOBs: Core[1]	26	22	22
IOBs: Core +Ext Logic	26	22	22
Clock IOBs	1	1	1
Max Data Rate	10 Mbit	584 Mbit	376 Mbit
Performance	40 Mhz	73 MHz	47 MHz
Xilinx Tools	M1.5i	M1.5i	M1.5i
Special Features	BlockRAM	BlockRAM	SelectRAM

Notes:
1. Assume all core signals are routed off-chip.
2. Virtex utilization numbers are in CLB slices.

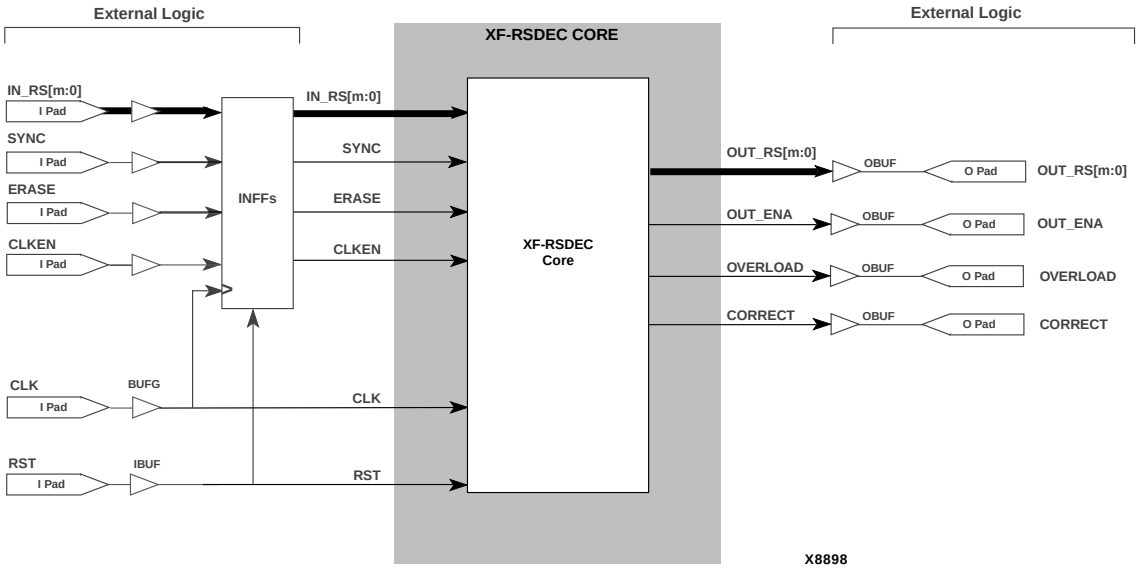

Figure 1: XF-RSDEC Core with External Logic (Examples 2 and 3)

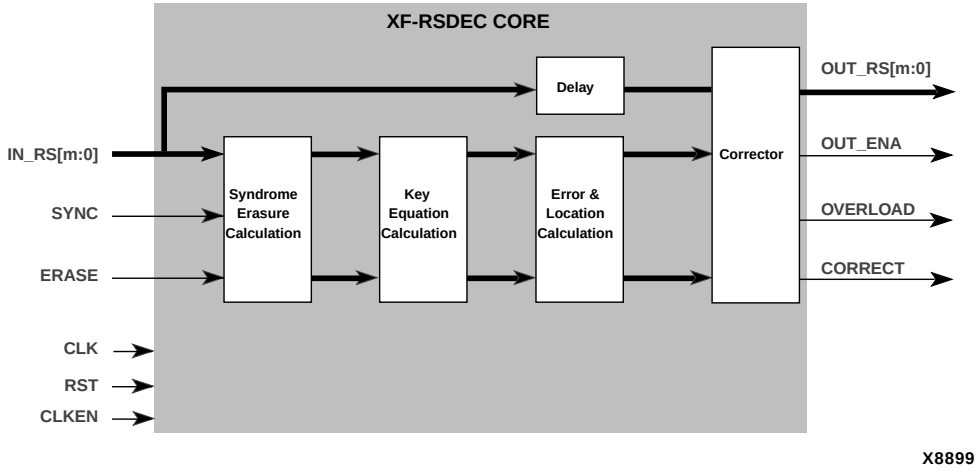

Figure 2: XF-RSDEC Core Block Diagram (Examples 2 and 3)

- Symbol size
- Symbol clock rate
- System clock rate
- Erasure Support

- Continuous or burst mode operation
- Supports high speed applications (>580Mbps)
- Simple core interface for ease of integration
- Includes Verilog or VHDL source code

Applications

- Data communication channels
- DTV/HDTV broadcast
- Data storage systems
- Satellite communications

General Description

Reed-Solomon coding is a method of forward error correction in the form of block coding. Block coding consists of

calculating a number of parity symbols over a number of message symbols. The parity symbols are appended to the end of the message symbols forming a codeword. Reed-Solomon coding is described in the form RS(n,k), where k is the number of message symbols in each block and n is the total number of symbols in the codeword. The value t defines the number of symbol errors, e, and the number of erasures, s, that can be corrected by the Reed-Solomon code, where n-k=2t and $2e+s \leq 2t$. An erasure is defined as a symbol error in which the location of the error is known.

Reed-Solomon codes are calculated in a finite field of elements, or Galois fields GF(2^m). The Galois field is defined by a primitive polynomial P(X) and a generator polynomial G(X). The degree of the primitive polynomial, m, defines the number bits per data symbol (m = bits per symbol) and the maximum length of the codeword (2^m-1=maximum codeword length n).

XF-RSDEC is a “core” logic module specifically designed for Virtex and XC4000 FPGAs.

Various forms of the core have been developed. One supports high data rates where area is a secondary concern. Another supports low data rates where a high-speed system clock is available and area is a primary concern.

The cores use the most efficient decoder algorithm, based on the number of parity symbols and whether erasure support is required or not.

The cores can be customized to support either fixed or variable values of parity symbols, message symbols, and codeword length.

Each core includes the Verilog or VHDL RTL source code, an example design instantiation, sample synthesis and simulation project files, test bench, test vectors, and User’s Guide.

The XF-RSDEC-INTELSAT is a precustomized core that is compliant with the IESS-308 Intelsat standard. The primitive polynomial and generator polynomial implemented is $P(x)= x^8+x^7+x^2+x^1+1$ and $G(x)= (x-a^{120})(x-a^{121})\ldots(x-a^{119+2t})$ over a Galois field of GF(256). A 2-bit input control signal selects between four different codeword/message lengths: RS(126,112), RS(194,178), RS(219,201), and RS(225,205). The XF-RSDEC-INTELSAT core is delivered as Verilog or VHDL RTL source code. Detailed timing and pin descriptions of the XF-RSDEC-INTELSAT can be found in the User’s Guide available from Memec Design Services.

MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance, where one of our cores generates a clock, that signal is brought out of the core, run through a global buffer, and then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this philosophy is that the cores are not self-contained. External logic must be connected to the core in order to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality. This datasheet describes both the core and the supplied external logic.

The Absolute Maximum Ratings, Operating Conditions, DC Electrical Specifications, and Capacitance are device dependent and can be found in the Xilinx datasheet for the target device.

Functional Description

The Reed-Solomon decoder core is partitioned into modules as shown in Figure 2, and described below.

Syndrome Erasure Calculation

The Syndrome Erasure Calculation block treats the input codeword as a series of polynomial coefficients and calculates a syndrome polynomial of 2t coefficients (t is the maximum number of errors that can be corrected by the Reed-Solomon Code). The syndrome polynomial contains the location and magnitude of up to t errors in an invalid codeword. A valid codeword generates a syndrome polynomial with all zero coefficients. Decoder cores that include erasure support calculate an erasure polynomial.

Key Equation Calculation

The Key Equation Calculation block generates the key equations (locator polynomial and evaluator polynomial) from the syndrome and erasure polynomials. The locator polynomial contains information about the location of bad symbols in the codeword. The evaluator polynomial contains information about the error magnitude of the bad symbols.

Error & Location Calculation

The Error & Location Calculation block determines the error locations and error magnitudes from the locator polynomial and evaluator polynomial.

Delay

The Delay block compensates for latency through the syndrome calculation, key equation calculation, and error & location calculation blocks. The output of the Delay drives the corrector block.

Corrector

The Corrector block corrects the bad symbols in the delayed input Codeword. The corrector also generates the output signals OUT_ENA, OVERLOAD, and CORRECT. OUT_ENA is active when message symbols are present at OUT_RS[m:0]. CORRECT flags a symbol, at OUT_RS[m:0], that has been corrected. OVERLOAD flags an entire codeword that was determined uncorrectable.

Core Modifications

Memec Design Services will customize and deliver a Xilinx version of the XF-RSDEC core that meets your requirements. To do so use the fax-in request form, included at the end of this data sheet, or email the information to Memec Design Services at "info@memecdesign.com".

Pinout

The pinout of the XF-RSDEC core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are provided in Table 2.

Verification Methods

Functional and timing simulation has been performed on the XF-RSDEC using Verilog or VHDL. (Simulation vectors used for verification are provided with the core).

Recommended Design Experience

A basic understanding of Reed-Solomon encoding is suggested. Users should be familiar with Verilog or VHDL synthesis and simulation as well as Xilinx design flows.

Ordering Information

The Reed-Solomon Decoder core is available for purchase directly from Memec Design Services. The implementation will vary depending upon the application. The attached Fax form has been included to request further information from Memec Design Services.

Memec Design Services warrants that the design delivered by Memec Design Services will conform to the design specification. This warranty expires 3 months from the date of delivery of the design database. Contact Memec De-sign Services for the Design License Agreement with complete Terms and Conditions of Sale.

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Table 2: Core Signal Pinout

Signal	Signal Direction	Description
IN_RS[m:0]	Input	Input data symbol
SYNC	Input	Sync flag
ERASE	Input	Erasure flag (Optional)
CLKEN	Input	Clock enable
CLK	Input	System clock
RST	Input	Asynchronous reset
OUT_RS[m:0]	Output	Output data symbol
OUT_ENA	Output	Output symbol valid flag
OVERLOAD	Output	Overloaded code flag
CORRECT	Output	Corrected symbol flag

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

Reed-Solomon
Implementation Request Form

To: **Memec Design Services**

FAX: 602-491-4907

E-mail: info@memecdesign.com

Memec Design Services will customize and deliver a Xilinx version of the XF_RSDEC core that meets your requirements. To do so use this fax-in request or email the information to Memec Design Services at:

info@memecdesign.com.

From: _____

Company:_____

Address:_____

City,State,Zip:_____

Country:_____

Phone:_____

FAX:_____

E-mail:_____

Implementation Issues

1. Primitive Polynomial
(e.g. $P(x)=x^8+x^4+x^3+x^2+1$)

2. Generator Polynomial
(e.g. $G(x)= (x+a^0)(x+a^1)\ldots(x+a^{15})$)

3. System Clock Rate

4. Symbol Rate

5. Bits per symbol (m)

6. Message and Codeword Length (e.g. RS(204,188))

7. Number of parity symbols

8. Fixed or variable codeword length

9. Fixed or variable number of parity symbols

10. Decoder erasure support (yes/no)

11. Xilinx target part & speed grade

12. Source Code (Verilog/VHDL)

13. Do you need Encoder, Decoder or both?

Business Issues

1. Indicate timescales of requirement
a. date for decision____
b. date for placing order____
c. required delivery date____

2. Indicate your area of responsibility
a. decision maker____
b. budget holder____
c. recommender____

3. Has a budget been allocated for the purchase?

4. What volume do you expect to ship of the product that will use this core?

5. What major factors will influence your decision?

6. Are you considering any other solutions?