Memec Design Services

Memec Design Services

7810 South Hardy Drive, Suite 104
Tempe, Arizona 85284 USA
Phone: +1 888-845-5585 (USA)
+1 480-753-5585
Fax: +1 480-753-5899
E-mail: info@memecdesign.com
URL: www.memecdesign.com

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core Documentation
Design File Formats	VHDL/Verilog RTL files
Constraints File	.ucf
Verification	testbench, Test vectors
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	Sample Implementation in Verilog or VHDL
Additional Items	Warranty by MDS
Simulation Tool Used	
Model Technology, Silos	
Support	
Support provided by Memec Design Services.	

Features

- Supports 4000X, Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Core design is customized using the following specifications
  - Primitive polynomial
  - Generator polynomial
  - Number of parity symbols

Table 1: Example Implementations

	XF-RSENC-DVB Example #1	XF-RSENC-DVB Example #2	XF-RSENC-DVB Example #3	XF-RSENC-INTELSAT Example #4
Parity Symbols	16	16	16	14,16,18,20
Bits/Symbol	m=8	m=8	m=8	m=8
Supported Family	Spartan	4000XL	Virtex	Virtex
Device Tested	S05-3	4005XL-09	V50-6	V150-4
CLBs: Core +Ext Logic	76[2]	101[3]	94[3,4]	138[2,4]
IOBs: Core[1]	19	19	19	24
IOBs: Core +Ext Logic	19	19	19	24
Clock IOBs	1	1	1	1
Max Data Rate	368 MBit	624 MBit	904 MBit	10 MBit
Performance	46 MHz	78 MHz	113 MHz	44 MHz
Xilinx Tools	M1.5i	M1.5i	M1.5i	M1.5i
Special Features	None	None	None	SelectRAM

Notes:
1. Assume all core signals are routed off-chip.
2. Optimized for area during synthesis.
3. Optimized for speed during synthesis.
4. Virtex utilization numbers are in CLB slices.

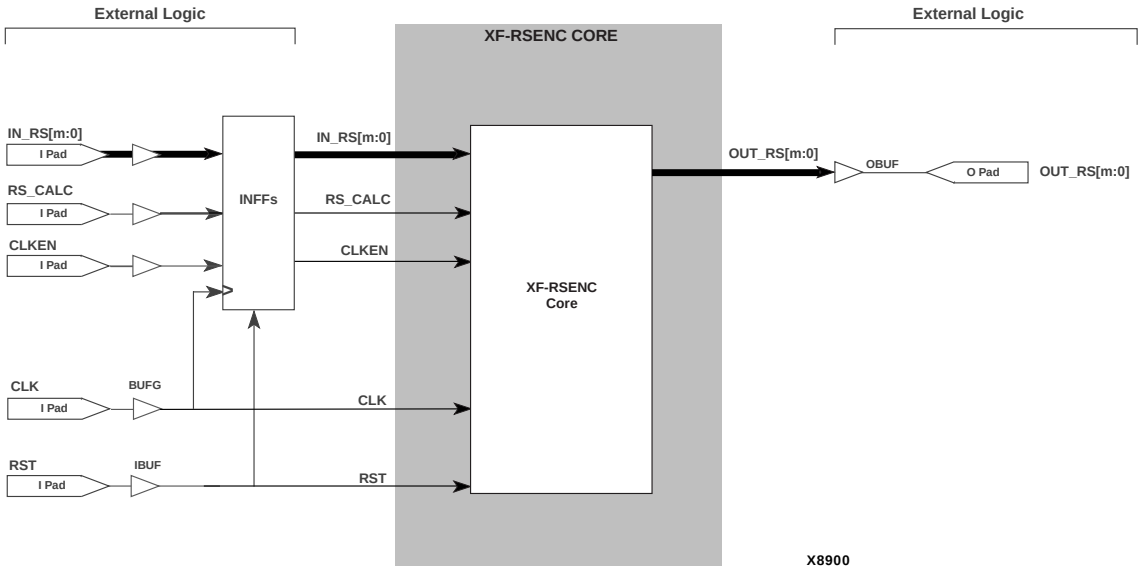

Figure 1: XF-RSENC Core with External Logic (Examples 1, 2, 3)

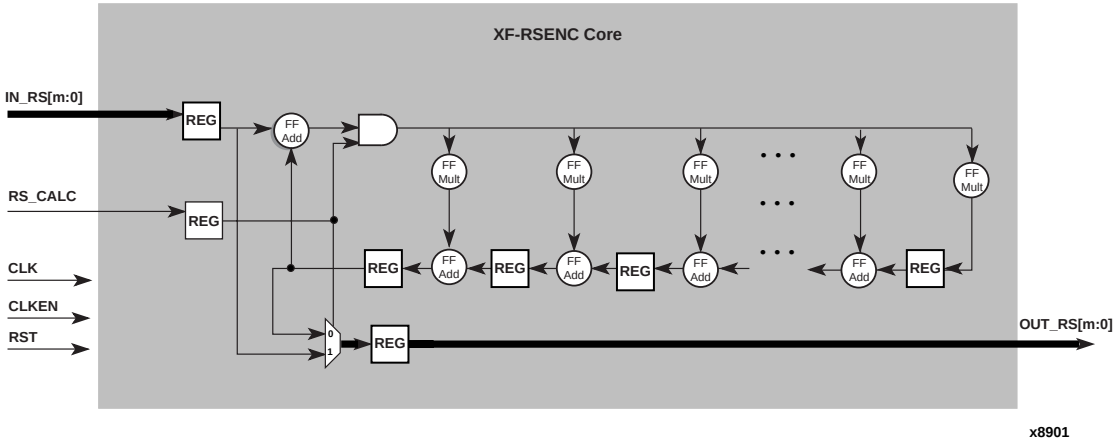

Figure 2: Reed Solomon Encoder Functional Block Diagram (Examples 1, 2, 3)

  - Symbol size
  - Symbol clock rate
  - System clock rate
- Message Block length configured by end user
- Continuous or burst mode operation
- Supports high speed applications (>900Mbps)
- Simple core interface for ease of integration
- Includes Verilog or VHDL source code

Applications

- Data communication channels
- DTV/HDTV broadcast
- Data storage systems
- Satellite communications

General Description

Reed-Solomon coding is a method of forward error correction in the form of block coding. Block coding consists of calculating a number of parity symbols over a number of

message symbols. The parity symbols are appended to the end of the message symbols forming a codeword. Reed-Solomon coding is described in the form RS(n,k), where k is the number of message symbols in each block and n is the total number of symbols in the codeword. The value t defines the number of symbols that can be corrected by the Reed-Solomon code, where t=(n-k)/2.

Reed-Solomon codes are calculated in a finite field of elements, or Galois fields GF(2^m). The Galois field is defined by a primitive polynomial P(X) and a generator polynomial G(X). The degree of the primitive polynomial, m, defines the number of bits per data symbol (m = bits per symbol) and the maximum length of the codeword (2^m-1=maximum codeword length n).

XF-RSENC is a "core" logic module specifically designed for Xilinx FPGAs.

Various forms of the core have been developed. One supports high data rates where area is a secondary concern. Another supports low data rates where a high-speed system clock is available and area is a primary concern.

The cores work for any valid codeword length and can be customized to support either fixed or variable values of parity symbols.

Each core includes the Verilog or VHDL RTL source code, an example design instantiation, sample synthesis and simulation project files, test bench, test vectors, and User's Guide

The core has been developed in two different approaches. One approach is optimized for encoders with a single value of t. The other approach is optimized for encoders with selectable values of t. Both approaches are optimized for speed and area to the Spartan, XC4000 and Virtex family of Xilinx FPGAs. Each core is delivered as Verilog or VHDL RTL source code.

The XF-RSENC-INTELSAT is a precustomized core that calculates a selectable 14, 16, 18, or 20 parity symbols (t = 7, 8, 9, or 10) and is compliant with the IESS-308 Intelsat standard. The primitive polynomial and generator polynomial implemented is $P(x)= x^8+x^7+x^2+x^1+1$ and $G(x)= (x-a^{120})(x-a^{121})\ldots(x-a^{119+2t})$ over a Galois field of GF(256). A 2-bit input control signal selects between four different codeword/message lengths: RS(126,112), RS(194,178), RS(219,201), and RS(225,205). The XF-RSENC-INTELSAT core is delivered as Verilog or VHDL RTL source code. Detailed timing and pin descriptions of the XF-RSENC-INTELSAT can be found in the User's Guide available from Memec Design Services.

The XF-RSENC-DVB is a precustomized core that calculates 16 parity symbols and is compliant with the DVB standard. The primitive polynomial and generator polynomial implemented is $P(x)= x^8+x^4+x^3+x^2+1$ and $G(x)= (x-a^0)(x-a^1)\ldots(x-a^{15})$ over a Galois field of GF(256). The core is adaptable to any message/codeword length RS(n,k) where n-k=16. Thus, the largest code supported by this core is R(255,239). The DVB standards specify a code of RS(204,188). The XF-RSENC-DVB core is delivered as a netlist version on the enCORE CD-ROM or as Verilog or VHDL RTL source code, both from Memec Design Services. Detailed timing and pin descriptions of the XF-RSENC-DVB can be found in the User's Guide available from Memec Design Services.

MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance, where one of our cores generates a clock, that signal is brought out of the core, run through a global buffer, and then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this philosophy is that the cores are not self-contained. External logic must be connected to the core in order to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality. This datasheet describes both the core and the supplied external logic.

The Absolute Maximum Ratings, Operating Conditions, DC Electrical Specifications, and Capacitance are device dependent and can be found in the Xilinx datasheet for the target device.

Functional Description

The Reed-Solomon encoder core is partitioned into modules as shown in Figure 2, and described below.

All registers are driven by common clock (CLK), clock enable (CLKEN), and asynchronous reset (RST) signals. This provides ultimate flexibility in integration of the core into larger systems. The registers are clocked on the rising edge of CLK, enabled by a high on CLKEN, and asynchronously reset by a high on RST.

The RS_CALC signal controls whether the core is calculating the parity (high) or shifting out the calculated parity (low). Logic external to the core is required to generate this control signal. This allows the user to vary the message block length as desired for shortened codes. The RS_CALC pin must be held at a low for 2t enabled clock cycles to ensure all parity register values are shifted out and the registers are cleared.

FFADD

This block performs modulo 2 addition of the input symbols.

FFMULT

This block performs a finite field multiplication, over the Galois field, of a constant and the input symbol.

Core Modifications

Memec Design Services will customize and deliver a Xilinx version of the XF-RSENC core that meets your requirements. To do so use the fax-in request form, included at the end of this data sheet, or email the information to Memec Design Services at “info@memecdesign.com”.

Pinout

The pinout of the XF-RSENC core has not been fixed to specific FPGA I/O, allowing flexibility with a user’s application. Signal names are provided in Figure 1 and Table 2.

Verification Methods

Functional and timing simulation has been performed on the XF-RSENC using Verilog or VHDL. Simulation vectors used for verification are provided with the core.

Recommended Design Experience

A basic understanding of Reed-Solomon encoding is suggested. Users should be familiar with Verilog or VHDL synthesis and simulation as well as Xilinx design flows.

Ordering Information

The Reed-Solomon Decoder core is available for purchase directly from Memec Design Services. The implementation will vary depending upon the application. The attached Fax form has been included to request further information from Memec Design Services.

Memec Design Services warrants that the design delivered by Memec Design Services will conform to the design specification. This warranty expires 3 months from the date of delivery of the design database. Contact Memec De-sign Services for the Design License Agreement with complete Terms and Conditions of Sale.

Information furnished by Memec Design Services is believed to be accurate and reliable. Memec Design Services reserves the right to change specifications detailed in this data sheet at any time without notice, in order to improve reliability, function or design, and assumes no responsibility for any errors within this document. Memec Design Services does not make any commitment to update this information.

Memec Design Services assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction, if such be made, nor does the Company assume responsibility for the functioning of undescribed features or parameters. Memec Design Services will not assume any liability for the accuracy or correctness of any support or assistance provided to a user.

Memec Design Services does not represent that products described herein are free from patent infringement or from any other third-party right. No license is granted by implication or otherwise under any patent or patent rights of Memec Design Services.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
IN_RS[m:0]	Input	Input data symbol
RS_CALC	Input	Parity calculate/shift
CLKEN	Input	System clock enable
CLK	Input	System clock
RST	Input	Asychronous reset
OUT_RS[m:0]	Output	Output data symbol

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

Reed-Solomon
Implementation Request Form

To: **Memec Design Services**

FAX: 1-602-491-4907

E-mail: info@memecdesign.com

Memec Design Services will customize and deliver a Xilinx version of the XF_RSENC core that meets your requirements. To do so use this fax-in request or email the information to Memec Design Services at info@memecdesign.com.

From: _____

Company:_____

Address:_____

City,State,Zip:_____

Country:_____

Phone:_____

FAX:_____

E-mail:_____

Implementation Issues

1. Primitive Polynomial
(e.g. $P(x)=x^8+x^4+x^3+x^2+1$)

2. Generator Polynomial
(e.g. $G(x)= (x+a^0)(x+a^1)\ldots(x+a^{15})$)

3. System Clock Rate

4. Symbol Rate

5. Bits per symbol (m)

6. Message and Codeword Length (e.g. RS(204,188))

7. Number of parity symbols

8. Fixed or variable codeword length

9. Fixed or variable number of parity symbols

10. Decoder erasure support (yes/no)

11. Xilinx target part & speed grade

12. Source Code (Verilog/VHDL)

13. Do you need Encoder, Decoder or both?

Business Issues

1. Indicate timescales of requirement
a. date for decision____
b. date for placing order____
c. required delivery date____

2. Indicate your area of responsibility
a. decision maker____
b. budget holder____
c. recommender____

3. Has a budget been allocated for the purchase?

4. What volume do you expect to ship of the product that will use this core?

5. What major factors will influence your decision?

6. Are you considering any other solutions?