M8254 Programmable Timer

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Features

- Supports Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Multiple, programmable, multi-mode timers
- Real-time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator

Applications

- Binary rate multiplier
- Complex waveform generator
- Complex motor controller
- Baud rate generator

General Description

The M8254 is a programmable interval timer/counter core designed for use with standard micro-processor systems. It has three 16 bit counters, each of which is programmable to generate an interrupt at the end of a user-defined interval.

AllianceCORE™ Facts

Core Specifics		
Supported Family	Spartan	Virtex
Device Tested	S40-3	V300-4
CLBs	260	244[2]
Clock IOBs	3	3
IOBs[1]	19	19
Performance (MHz)	12.4 MHz	34 MHz
Xilinx Core Tools	M1.3	M1.5i
Special Features	None	None
Provided with Core		
Documentation	Core Design Document	
Design File Formats	EDIF netlist, .ngd, Verilog Source RTL available extra	
Constraints File	m8254.ucf	
Verification	Test vectors	
Instantiation Templates	VHDL, Verilog	
Reference Designs & Application Notes	None	
Additional Items	None	
Simulation Tool Used		
Verilog XL, version 2.6		
Support		
Support provided by Virtual IP Group Inc.		

Notes:
1. Assuming all core I/O are routed off-chip.
2. Utilization numbers for Virtex are in CLB slices.

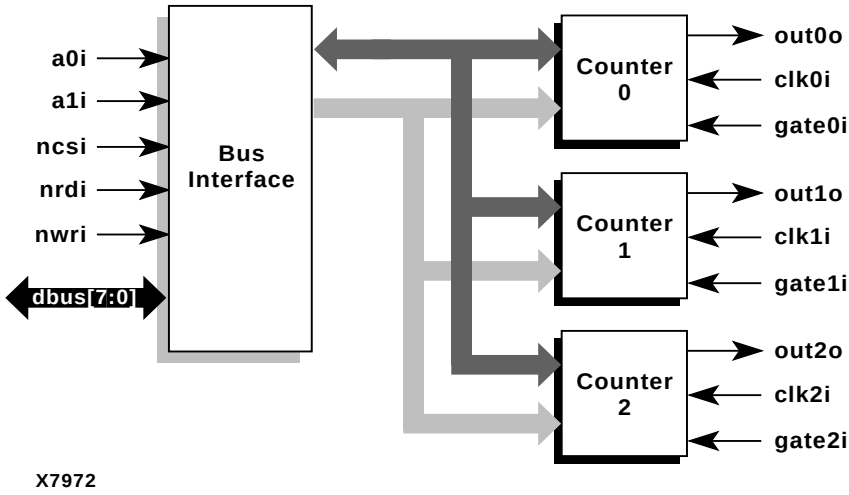

Figure 1: M8254 Block Diagram

Functional Description

The M8254 Core is partitioned into modules as shown in Figure1 and described below.

Bus Interface Block

This block contains decoders to generate counter select and the counter control select signals.

Counter 0-2 Blocks

These independently programmable counter blocks generate output based on the mode selected.

Core Modifications

Virtual IP Group, Inc. can modify this core to vary the number of timers.

Pinout

The pinout has not been fixed to specific FPGA I/O allowing flexibility with the user application. Signal names are provided in the block diagram shown in Figure 1 and described in Table 1.

Verification Methods

The core has been tested with in-house developed test vectors that are provided with the core.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Bus Interface Signals		
a0i, a1i	Input	Address Signals
ncsi	Input	Chip select, active low
nrdi	Input	Read signal, active low
nwri	Input	Write signal, active low
dbus[7:0]	In/Out	8-bit bidirectional CPU data bus[1]
Counter Signals		
out0o	Output	Output of counter 0
clk0i	Input	Clock input for counter 0
gate0i	Input	Gate input for counter 0
out1o	Output	Output of counter 1
clk1i	Input	Clock input for counter 1
gate1i	Input	Gate input for counter 1
out2o	Output	Output of counter 2
clk2i	Input	Clock input for counter 2
gate2i	Input	Gate input for counter 2

Notes:
1. Bus expanded into individual nets in the design.

Recommended Design Experience

Knowledge of microprocessor based systems is required. The user must be familiar with HDL design methodology, instantiation of Xilinx netlists in a hierarchical design environment and usage of Xilinx Alliance or Foundation development tools.

Ordering Information

This product is available from Virtual IP Group, Inc. Please contact them for pricing and additional information.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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