M8255 Programmable Peripheral Interface

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Features

- Supports Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Multi-mode programmable parallel I/O port peripheral interface
- 24 programmable general purpose I/O signals
- Functionally compatible with Intel 8255A
- Control word read-back facility
- Direct bit set/reset capability
- I/O data transfer with handshaking

Applications

- General purpose I/O ports used to control external peripherals

General Description

The M8255 Programmable Peripheral Interface (PPI) core is a general purpose I/O component to interface peripheral equipment with a microcomputer system bus. The functional configuration of the M8255 is programmable. This core is functionally compatible with the INTEL 8255.

AllianceCORE ™ Facts		
Core Specifics		
Supported Family	Spartan	Virtex
Device Tested	S40-3	V300-4
CLBs	111	80[2]
Clock IOBs	-	-
IOBs[1]	38	38
Performance (MHz)	15.2 MHz	50 MHz
Xilinx Core Tools	M1.3	M1.5i
Special Features	None	None
Provided with Core		
Documentation	Core Design Document	
Design File Formats	EDIF netlist, .ngd, Verilog Source RTL available extra	
Constraints File	m8255.ucf	
Verification	Test vectors	
Instantiation Templates	VHDL, Verilog	
Reference Designs & Application Notes	None	
Additional Items	None	
Simulation Tool Used		
Verilog XL, version 2.6		
Support		
Support provided by Virtual IP Group Inc.		

Notes:
1. Assuming all core I/O are routed off-chip.
2. Utilization numbers for Virtex are in CLB slices.

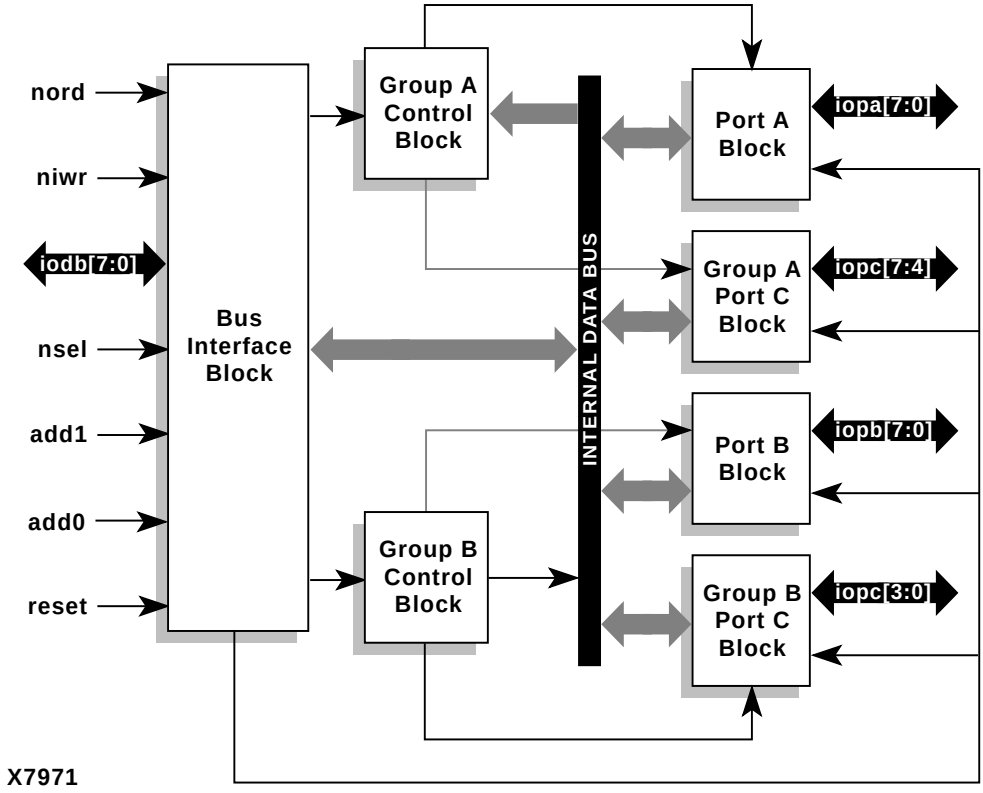

Figure 1: M8255 Functional Block Diagram

Functional Description

The M8255 core is partitioned into modules as shown in Figure 1 and described below.

Bus Interface Block

This block handles CPU Interface, and generates necessary control signals to pass CPU data to control and port blocks.

Group A Control Block

This block handles mode selection and control functions of Port A and Port C blocks for iopc[7:4].

Group B Control Block

This block handles mode selection and control functions of Port B and Port C blocks for iopc[3:0].

Port A Block

This block provides input and output latches to interface iopa[7:0] data to external peripherals.

Port B Block

This block provides input and output latches to interface iopb[7:0] data to external peripherals.

Group A Port C Block

This block provides the input and output latches to interface iopc[7:4] data to external peripherals. This block also provides the interface to handshake signals in modes 1 and 2.

Group B Port C Block

This block provides the input and output latches to interface iopc[3:0] data to external peripherals. This block also provides the interface to handshake signals in modes 1 and 2.

Core Modifications

Virtual IP Group, Inc. can integrate multiple M8255s to increase I/O capacity upon request.

Pinout

The pinout has not been fixed to specific FPGA I/O allowing flexibility with the user application. Signal names are provided in the block diagram shown in Figure 1 and described in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Bus Interface Signals		
nord	Input	Read Enable used by host processor to read a byte from selected data port register; active low.
niwr	Input	Write Enable used by host processor to write a byte to data port or control register; active low.
iodb[7:0]	In/Out	8 bit bi-directional CPU data bus[1].
nsel	Input	Chip Enable for accessing internal registers including Port registers for reads or writes; active low.
add1, add0	Input	Address lines from CPU to determine In/Out port accessed during Read or Write cycles.
reset	Input	Reset, active high.
Port Signals		
iopa[7:0]	In/Out	8 bit bi-directional Port A data bus[1].
iopb[7:0]	In/Out	8 bit bi-directional Port B data bus[1].
iopc[7:0]	In/Out	8 bit bi-directional Port C data bus[1].

Notes:
1. Bus expanded into individual nets in the design.

Verification Methods

The core has been tested with in-house developed test vectors that are provided with the core.

Recommended Design Experience

Knowledge of DMA interfaces in a microprocessor based systems is required. The user must be familiar with HDL design methodology, instantiation of Xilinx netlists in a hierarchical design environment and usage of Xilinx Foundation or Alliance development tools.

Ordering Information

This product is available from Virtual IP Group, Inc. Please contact them for pricing and additional information.

Related Information

Refer to Specification Document for programming of this core for a typical system application. The user should refer to the Desginer's Application Note for integrating this with other cores. Both documents are included with the Core Design Documentation.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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