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Appendix A

Application Notes

This section briefly describes relevant application notes. The latest versions of these documents are available online (at www.xilinx.com).

XAPP252: SigmaRAM DDR SRAM Interface for Virtex-II Devices

The SigmaRAM group, comprised of seven SRAM makers, recently defined SDR and DDR versions of separate I/O SRAM specifications. This application note describes a reference interface for separate I/O Sigma DDR SRAM modules (GS817xD series). GS817xD are 18,874,368 bits (16 MB) SRAMs. This reference interface, implemented for Virtex-II FPGAs, is targeted to support user configurable mode, late write, and early write features of SigmaRAM modules. The DDR SRAM operates at a clock frequency of 333 MHz, and the reference design is also supports 666 Mb/s throughput of Sigma DDR SRAM modules.

Fully synthesizable Verilog/VHDL code is available for the reference design.

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XAPP253: DDR SDRAM Controller for Virtex-II Devices

DDR (Double Data Rate) SDRAM is an enhancement to standard SDRAM. It activates output on both the rising and falling edge of the system clock rather than on just the rising edge, potentially doubling the output.

The presence of DDR registers in Virtex-II architecture makes it an ideal choice for implementing a controller for DDR SDRAM modules. This application note describes a reference controller design for a 64-bit DDR SDRAM. The aim of this reference design is to facilitate controller design using Virtex-II DDR and Digital Clock Manager (DCM) features.

Fully synthesizable Verilog/VHDL code is available for the reference design.

XAPP254: SiberCAM Interface for Virtex-II Devices

SiberCAM is a Content-Addressable Memory (CAM) for use with ternary data of variable widths. SiberCAM Ultra-2M is a full family of large capacity CAMs in a single device: array configurations of 64k x 36, 32k x 72, 16k x 144, and 8k x 288 are all supported in one 2M - ternary density chip. In addition, the chip can be configured for variable-width operation, where any combination of 36-, 72-, 144-, and 288- bit entries are stored efficiently on the same chip, without wasting any storage resources. All device configurations are register selectable.

Ternary (3-state: 0, 1, or X) data is stored at addresses inside the SiberCAM module using maintenance operations. Search data is presented to the SiberCAM module through the search data port. After several clock cycles, an address containing data that best matches the data inside the SiberCAM module is returned on the search address (results) port.

An RTL reference design is provided that demonstrates the interface between a 32-bit host and a SiberCAM module, or cascade of SiberCAM modules. This Verilog/VHDL code is fully synthesizable, and the design is implemented using a Virtex-II FPGA. The DDR registers in Virtex-II devices are used for bursting data streams into the CAM.

This example interface demonstrates a way to initiate searches, obtain search results, and perform maintenance operations on SiberCAM modules, via a single interface from a host system with 32-bit access. Whether using the separate maintenance port or the search data port in two-port mode, the SiberCAM module expects maintenance operations to be performed in 36-bit/72-bit multiplexed quantities. This interface provides a mechanism to perform these operations using a 32-bit interface that resembles an SRAM.

XAPP256: FIFOs Using Virtex-II Shift Registers

The RAM-based shift registers available in Virtex-II devices ideally serve to build synchronous FIFOs. FIFOs using the SRL16 shift registers are very flexible for cascading together FIFOs of any width (1-bit) and depth (in multiples of 16) . This application note describes a synchronous FIFO built using the SRL16 shift registers. It includes synthesizable code for configuring FIFOs of any desired width and depth.

Fully synthesizable Verilog/VHDL code is available for the reference design.

XAPP257: Asynchronous FIFO in Virtex-II Devices

Asynchronous FIFOs with independent clocks for writing and reading are a popular method of transferring data across asynchronous clock-domain boundaries. The true dual-port operation of the Virtex-II block RAMs is ideal for implementing asynchronous FIFOs. In this application, each block RAM is configured as a 18-bit wide, 1024-deep RAM, with independent addressing, clocking, and clock enable for both ports, one write port and one read port. Clock cycle time for either clock can be as short as 5 ns. This application note concentrates on the remaining tasks, generating the Grey-coded write and read addresses, and generating the FULL and EMPTY control flags.

Fully synthesizable Verilog/VHDL code is available for the reference design.

XAPP258: FIFOs Using Virtex-II Block RAM

This application note uses the fully synchronous dual-ported RAMs with 18K of memory cells available in Virtex-II devices. These blocks are ideal for FIFO applications, and each port can be configured independently as 16K x 1, 8K x 2, 4K x 4, 2K x 9, 1K x 18, or 512 x 36.

This application note describes a common-clock (synchronous) version and an independent-clock (asynchronous) version of a 511 x 36 FIFO, with the depth and width being adjustable within the Verilog or VHDL code. The size of the FIFO is 511 x 36 instead of 512 x 36 since one address is dropped out of the FIFO in order to provide distinct Empty/Full conditions. First the design for a 511 x 36 FIFO with common Read and Write clocks is described, and then the design changes required for the more difficult case of independent Read and Write clocks are presented.

Fully synthesizable Verilog/VHDL code is available for the reference design.

XAPP260: Using Block RAM for High Performance Read/Write CAMs

CAM (Content Addressable Memory) offers increased data search speed. In various applications based on CAM, there are differing requirements for data organinzatation and

read/write performance. The design described in this application note is suited for small embedded CAMs with high-speed match and write requirements.

The Virtex-II block RAM can be used as a 32-word deep by 8-bit wide (32 x 8) CAM using the innovative design techniques described in this application note. A reference design provides parameterizable Verilog and VHDL code to cascade several block RAMs configured as 32 x 8 CAM. CAM speed is equivalent to the access time of a Virtex-II block RAM for a single clock cycle match (read), and a one or two clock cycles write. Medium size CAMs can be implemented in Virtex slices with different design techniques.

Fully synthesizable Verilog/VHDL code is available for the reference design.

XAPP261: Data-Width Conversion FIFOs Using Virtex-II Block RAM Memory

This application note is an enhancement to XAPP258 (FIFOs using Virtex-II block RAM). In general, only the changes from XAPP258 will be covered. Four different data-width conversion FIFOs are described in this document. The first has a common clock with a 511 x 36 Write port and a 2044 x 9 Read port. The second has a common clock, a 2044 x 9 Write port, and a 511 x 36 Read port. The last two are similar FIFOs with independent Read and Write clocks.

Fully synthesizable Verilog/VHDL code is available for the reference design.

XAPP262: QDR SRAM Interface for Virtex-II Devices

Virtex-II series FPGAs provide access to a variety of on-chip and off-chip RAM resources. In addition to on-chip distributed RAM and block SelectRAM features, Virtex-II FPGAs can interface with a variety of external high-speed memory devices. The combination of high-speed SelectI/O resources and on-chip Digital Clock Manager (DCM) circuits enable a high bandwidth interface to Quad Data Rate (QDR) architecture SRAM modules. This application note describes an interface implemented between a Cypress xx QDR SRAM module and a Virtex-II device.

Fully synthesizable Verilog/VHDL code is available for the reference design.

XAPP266: FCRAM Controller for Virtex-II Devices

Delay-Locked Loop (DLL), SelectI/O, and enhanced DDR features make Virtex-II FPGAs the perfect choice for implementing a DDR FCRAM controller. This application note describes a controller implementation for Toshiba and Fujitsu FCRAMs. A reference design is provided with the following features:

- Utilization of the enhanced Virtex-II DDR interface
- Support for various FCRAM size offerings and scalable for next-generation FCRAM devices
- Maximum frequency of 154 MHz, with data throughput of 308 Mb/s per pin
- Programmable burst lengths
- Programmable column address strobe (CAS) latency
- Automatic refresh timer

Fully synthesizable Verilog/VHDL code is available for the reference design.

XAPP267: Parity Generation and Validation in Virtex-II Devices

Ensuring correct parity helps to determine the validity of data transmitted and received. This application note shows how to generate and validate parity in a design using a Virtex-II device. The parity generation block generates parity from input data and stores it in the block RAM on the DIP bus which is available for storing parity. The parity validation block also generates parity and compares it against the value available from the block RAM to ensure data validity. The application note details 8-bit, 16-bit, and 32-bit parity checks.

Fully synthesizable Verilog/VHDL code is available for the reference design.

XAPP268: Dynamic Clock Data Alignment

The phase alignment of clock and data inputs is an important feature available in Virtex-II devices. This application note explains the use of this feature by comparing the clock and data inputs and using the Digital Phase Shifter to align them.

Fully synthesizable Verilog/VHDL code is available for the reference design.

XAPP269: Fast CAM in Virtex-II Devices

Content Addressable Memories (CAM) allow fast searches for specific data in a memory. A wide variety of CAMs can be implemented in Virtex-II devices by using the basic LUT as a Shift Register (SRL16). Each CAM application will have different requirements. Designing CAMs with Virtex-II devices offers a flexible approach to specifying CAM depth and width.

This application note describes a fast CAM design finding a match in a single clock cycle. A methodology for designing flexible, small to medium size CAMs in Virtex-II slices. By using shift register primitives built into a Virtex-II slice, a reconfigurable LUT (two LUTs per slice) is used to implement a single-clock-cycle read CAM. A 4-bit CAM word fits into each LUT. A 32-word by 16-bit CAM would require 128 LUTs. The write operation uses the shift register mode and requires 16 clock cycles.

Fully synthesizable Verilog/VHDL code is available for the reference design.