Glossary

AQL

Acceptable quality level. The relative number of devices, expressed in parts-per-million (ppm), that might not meet specification or might be defective. Typical values are around 10 ppm,

ASIC

Application-specific integrated circuit, also called a *gate array.*

asynchronous

Logic that is not synchronized by a clock. Asynchronous designs can be faster than synchronous ones, but are more sensitive to parametric changes, and are thus less robust.

ATM

Asynchronous transfer mode. A very-high-speed (megahertz to gigahertz) connection-oriented bit-serial protocol for transmitting data and real-time voice and video in fixed-length packets (480byte payload, 5-byte header).

back annotation

Automatically attaching timing values to the entered design format after the design has been placed and routed in a field-programmable gate array (FPGA).

behavioral language

Top-down description from an even higher level than VDHL.

bitstream

The bitstream is a binary representation of an implemented FPGA design. The bitstream is generated by Xilinx bit generation tools (BitGen and Makebits) and is denoted with the **.bit** extension. For information on creating BIT files, refer to the *Hardware Debugger Reference/User Guide*.

block RAM

An 18-Kbit block of random access memory (RAM) inside the Virtex-II device. Dual-port and synchronous operation are desirable.

block SelectRAM

Fully-synchronous, dual-port memories in the Virtex-II FPGAs. Each of these memories contain 18 x 1024 (18,432) bits. The organization of each memory is configurable. Block SelectRAM resources complement smaller, distributed, LUT-based SelectRAM resources.

Boundary Scan interface

One of the configuration interfaces on the Virtex device. This is a bit-serial interface. The Boundary Scan interface is also known as the JTAG port. Also see *SelectMAP interface*.

capture data

The flip-flop and pad data saved from the logic cells and I/O blocks into the bitstream for readback. Use the CAPTURE_VIRTEX primitive in your HDL code to specify the trigger and clock for the capture operation.

compiler

Software that converts a higher-language description into a lower-level representation. For FPGAs, the complete partition, place, and process.

configurable logic block (CLB)

Xilinx-specific name for a block of logic surrounded by routing resources. The functional elements for constructing logic circuits. The Virtex-II CLB is made up of four slices, and each slice contains two Logic Cells.

configuration file

The internally stored file that controls the FPGA sot hat it performs the desired logic function. Also, the act of loading an FPGA with that file. That is, the process of programming Xilinx SRAM-based FPGAs with a bitstream.

configuration bitstream

Configuration commands with configuration data.

configuration clock (CCLK)

During configuration, the configuration clock (CCLK) is an output in Master modes or in the Asynchronous Peripheral mode but is an input in Slave, Synchronous Peripheral, Express, and SelectMAP/Slave Serial modes. After configuration, CCLK has a weak pull-up and can be selected as the readback clock.

configuration commands

Instructions for the Virtex-II device. There are two classes of Configuration Command — Major and Minor. The Major Commands read and write data to configuration registers in the Virtex-II device. The Minor commands instruct the Virtex-II configuration logic to perform specific functions.

configuration data

Bits that directly define the state of programmable logic. These are written to a Virtex-II device in a configuration bitstream, and read as readback data from a Virtex-II device.

configuration frame

The configuration bits in a Virtex-II device are organized in columns. A column of CLBs with the I/O blocks above and below the CLBs contain 48 frames of configuration bits. The smallest number of bits that can be read or written through the configuration interfaces is one frame.

configuration interface

A logical interface on the Virtex-II device through which configuration commands and data can be read and written. A interface consists of one or more physical device pins.

configuration readback

The operation of reading configuration data (also known as readback data) from a Virtex-II device.

constraints

Performance requirements imposed on the design, usually in the form of maximum allowable delay, or the required operating frequency.

$\overline{CS}$ pin

The $\overline{CS}$ pin is the Chip Enable pin for Virtex-II devices. It is used only in SelectMAP mode. When $\overline{CS}$ is asserted (Low) the device examines data on the Data bus. When $\overline{CS}$ is de-asserted (High), all CCLK transitions are ignored.

DataFrame

A DataFrame is a block of configuration data. A configuration bit-stream contains many such frames, each with a start bit and stop bits. Also see *configuration frame*.

device pin

One of the electrical connections on the package containing the Virtex-II device.

digital signal processing (DSP)

The manipulation of analog data that has been sampled and converted into a digital representation. Examples are filtering, convolution, Fast-Fourier-Transform, and so on.

DIN pin

During serial configuration, the DIN pin is the serial configuration data input receiving data on the rising edge of CCLK. During parallel configuration, DIN is the D0 input. After configuration, DIN is a user-programmable I/O pin.

DONE pin

The DONE pin on a Xilinx FPGA is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a low level on DONE can be configured to delay the global logic initialization and the enabling of outputs.

DOUT pin

During configuration in any mode except Express and SelectMAP, the DOUT pin is the serial configuration data output that can drive the DIN pin of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it is received at the DIN pin (in Master Serial Mode only).

DOUT/BUSY pin

For Virtex-II devices, the DOUT/BUSY pin has a dual purpose, depending on device mode. When the device is in Serial mode, this pin functions as DOUT. When the device is in SelectMAP/Slave Parallel mode, this pin functions as a handshaking signal. If BUSY is asserted (High) on a rising edge of CCLK, the data is not seen on the data bus, and should be held until the data is accepted.

dynamic random access memory (DRAM)

A low-cost read-write memory where data is stored on capacitors and must be refreshed periodically. DRAMs are usually addressed by a sequence of two addresses, row address, and column address, which makes them slower and more difficult to use than SRAMs. Also see *SRAM*.

electronic data interchange format (EDIF)

Industry standard for specifying a logic design in text (ASCII) form.

electrostatic discharge (ESD)

High-voltage discharge can rupture the input transistor gate oxide. ESD-protection diodes divert the current to the supply leads.

failure in time (FIT)

Describes the number of device failures statistically expected for a certain number of device-hours. Expressed as failures per one billion (10^9) device hours. Device temperature must be specified. Mean time between failure (MTBF) can be calculated from FIT. 10 FITs are good; 100 FITs are bad.

first-in first-out (FIFO)

FIFO memory where data is stored in the incoming sequence and is read out in the same sequence. Input and output can be asynchronous to each other. A FIFO needs no external addresses, although all modern FIFOs are implemented internally with RAMs driven by circular read and write counters.

flash

Non-volatile programmable technology, and alternative to electrically-erasable programmable read-only memory (EEPROM) technology. The memory content can be erased by an electrical signal. This allows in-system programmability and eliminates the need for ultraviolet light and quartz windows in the package.

flip-flop

Single-bit storage cell that samples its data input at the active (rising or falling) clock edge, and then presents the new state on its Q output after that clock edge, holding it there until after the next active clock edge.

frame

Also see *configuration frame*.

field programmable gate array (FPGA)

An integrated circuit that contains configurable (programmable) logic blocks and configurable interconnect between these blocks. Xilinx FPGAs are SRAM- based programmable logic devices (PLDs).

function generator

Also called a look-up table (LUT), with N inputs and one output. Can implement any logic function of its N inputs. N can be between 3 and 6; 4-input function generators are most popular.

gate

Smallest logic element with several inputs and one output. The AND gate output is High when all inputs are High. The OR gate output is High when at least one input is High. The NAND gate output is Low when all inputs are High. A 2-input NAND gate is used as the measurement unit for gate array complexity.

gate array

ASIC where transistors are predefined, and only the interconnect pattern is customized for the individual application.

graphical user interface (GUI)

The way of representing the computer output on the screen as graphics, pictures, icons, and windows. Pioneered by Xerox and the Apple Macintosh, now universally adopted, e.g., by Windows95 and others.

HDL

Hardware Description Language.

HardWire

Xilinx name for a low-cost derivative of an FPGA, where the configuration is fixed, but functionality and footprint are identical with the original FPGA-based design.

HDC pin

The High during configuration (HDC) pin is driven High until the I/Os become active in the Startup sequence. It is available as a control output indicating that configuration is not yet complete. After configuration, HDC is a user-programmable I/O pin.

hierarchical design

Design description in multiple layers, from the highest (overview) tot he lowest (circuit details). An alternative is flat design, where everything is described at the same level of detail.

$\overline{\text{INIT}}$ pin

The $\overline{\text{INIT}}$ pin is a quadruple function signal. Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 - 10 kΩ external pull-up resistor is recommended. As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O become active in the Startup sequence, $\overline{\text{INIT}}$ becomes a user-programmable I/O.

intellectual property (IP)

In the legal sense, patents, copyrights, and trade secrets. In integrated circuits (ICs), predefined large functions, called “cores,” that help the user complete a large design faster.

JTAG

Joint Test Action Group. Previous name for IEEE 1149.1 boundary scan, a method for testing boards and integrated circuits. Also see *Parallel Cable III*.

LogiBLOX

Library of logic modules, often with user-definable parameters, like data width. Similar to LPM.

logic cell (LC)

Metric for FPGA density. The basic building block of the Virtex-II CLB. An LC includes a 4-input function generator, carry logic, and a storage element.

LDC pin

Low during configuration (LDC) is driven Low until the I/Os become active in the Startup sequence. It is available as a control output indicating that configuration isn't complete. After configuration, LDC is a user-programmable I/O pin.

LPM

Library of Parametrized Modules. Library of logic modules, often with user-definable parameters, like data width. Similar to LogiBLOX.

LUT

Look-up table, also called a function generator with N inputs and one output. Can implement any logic function of its N inputs. N is between 3 and 6; most popular are 4-input LUTs.

LUT SelectRAM

Shallow RAM structure implemented in CLB look-up tables (LUTs). Also see *block SelectRAM*.

mapping

Process of assigning portions of the logic design to the physical chip resources (CLBs). With FPGAs, mapping is more demanding and more important a process than with gate arrays. Also see *synthesis*.

MTBF

Mean Time Between Failure. The statistically relevant up-time between equipment failure. Also see *failure in time (FIT)*.

MultiLINX cable

The MultiLINX cable provides many complex functions and can be loaded with new firmware as it becomes available. It can be connected to the host computer in two ways: via a Serial port or a USB port. The MultiLINX cable is supported by the Hardware Debugger software for Slave Serial and SelectMAP/Slave Parallel programming (as appropriate), as well as readback/verify. It is also supported by the JTAG programmer software for JTAG programming of both CPLDs and FPGAs.

netlist

Textual description of logic and interconnects. Also see *XNF file* and *electronic data interchange format (EDIF)*.

NRE

Non-Recurring Engineering charges. Start-up cost for the creation of an ASIC, gate array, or HardWire. Pays for layout, masks, and test development. FPGAs and CPLD do not require NRE.

optimization

Design change to improve performance. Also see *synthesis*.

pad

Pad bits are extra bits used to make the total number of bits in a frame an integral multiple of 32, the number of bits in a configuration word. A pad word is an extra word used at the end of a configuration frame for pipelining. A pad frame is an extra configuration frame used at the beginning of a configuration readback and at the end of a configuration write for pipelining.

Parallel Cable III

The Xilinx Parallel Cable III (model DLC5) is a serial download cable. The Parallel cable uses a serial 25-pin interface to the parallel port of a host computer and two 6-pin headers for flying-wire connectors to a target board. The Parallel cable is supported by the Hardware Debugger software for performing Slave Serial configuration of FPGAs only. The Parallel cable is also supported by the JTAG Programmer software for performing Slave Serial and Boundary Scan configuration of FPGAs, and Boundary Scan programming of CPLDs. For more information on using the Parallel cable, refer to Chapter 8 or this guide, the Hardware Debugger Reference/Users Guide, and the JTAG Programmer Guide.

partitioning

In FPGAs, the process of dividing the logic into subfunctions that can later be placed into individual CLBs. Partitioning precedes placement.

PCI

Peripheral Component Interface. Synchronous bus standard characterized by short range, light loading, low cost, and high performance. __?-MHz PCI can support data byte transfers up to ___? megabytes per second (Mb/s) on __? parallel data lines (including parity) and a common clock.

PCMCIA

Personal Computer Memory Card Interface Association. Physical and electrical standard for small plug-in boards for portable computers.

pin-locking

Rigidly defining and maintaining the functionality and timing requirements of device pins while the internal logic is still being designed or modified. Pin-locking has become important, since circuit board fabrication times are longer than PLD design implementation times.

PIP

Programmable Interconnect Point. In Xilinx FPGAs, a point where two signal lines can be connected, as determined by the device configuration.

placement

In FPGAs, the process of assigning specific parts of the design to specific locations (CLBs) on the chip. Usually done automatically. Also see *partitioning*.

PLD

Programmable Logic Device. Generic name for all programmable logic: PALs, CPLDs, and FPGAs.

preamble

The Preamble is a 4-bit binary sentinel (“0010”b) used to indicate the beginning of the LengthCount in the Header portion of the bitstream. At the beginning of configuration, FPGAs ignore all data prior to the preamble but counts the number of data bits preceding the preamble, and the LengthCount counter increments for every rising CCLK edge, even the ones proceeding the preamble.

programmable interconnect point

See *PIP*.

$\overline{\text{PROGRAM}}$ pin

The $\overline{\text{PROGRAM}}$ pin is an active-Low input that forces clearing of the FPGA configuration memory and is used to initiate a configuration cycle. While $\overline{\text{PROGRAM}}$ is held Low, the FPGA drives $\overline{\text{INIT}}$ Low and continues to clear the configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle, executes another complete clear cycle, goes into a WAIT state, and releases $\overline{\text{INIT}}$.

readback

Initiating a readback causes the configuration memory to become accessible to be serially clocked out and read from the device, or (byte-wide in SelectMAP/Slave Parallel modes). The configuration memory contains the configuration data, facilitating a Read-Verification of the data. The configuration memory can also contain the CLB output logic states facilitating a Read-Capture of the internal logic states.Read-Verification and Read-Capture are used by the Hardware Debugger for hardware verification. For information on the readback specification and timing, refer to *The Programmable Logic Data Book*. For information on using the readback component in a design, refer to the *Libraries Guide*. For information on enabling the readback function in the Implementation Software, refer to the *Development System Reference Guide*. For information on using the Hardware Debugger refer to the *Hardware Debugger Reference/User Guide*. For information on connecting the XChecker cable for readback, refer to the *Hardware Users Guide*.

readback data

Configuration data read from a Virtex-II device. The data is organized as configuration frames.

routing

The interconnection or the process of creating the desired interconnection of logic cells to make them perform the desired function. Routing follows after partitioning and placement.

schematic

Graphic representation of a logic design in the form of interconnected gates, flip-flops, and larger blocks. Older and more visually intuitive alternative to the increasingly more popular equation-based or high-level language textual description of a logic design.

SelectMAP interface

One of the configuration interfaces on the Virtex-II device. This is a byte-serial interface. The pins in the SelectMAP interface can be used as user I/O after configuration has been completed or remain configured as a configuration interface.

SelectRAM

Xilinx-specific name for RAM implemented in CLBs.

simulation

Computer modeling of logic and (sometimes) timing behavior of logic driven by simulation inputs (stimuli or vectors).

slice

A subdivision of the Virtex-II CLB. There are four vertical slices in each Virtex-II CLB. Each slice contains two Logic Cells.

SRAM

Static random access memory. Read-Write memory with data stored in latches. Faster than DRAM and with simpler timing requirements, but smaller in size and about four times more expensive than DRAM of the same capacity.

static timing

Detailed description of on-chip logic and interconnect delays.

submicron

The smallest feature size is usually expressed in micron (µ = millionth of a meter, or a thousandth of a millimeter). The state of the art is moving from 0.35µ to 0.25µ and soon may reach 0.18µ. The wavelength of visible light is 0.4µ to 0.8µ. 25.4µ = 1 mil, a thousandth of an inch.

synchronous

Circuitry that changes state only in response to a common clock, as opposed to asynchronous circuitry that responds to a multitude of derived signals. Synchronous circuits are easier to design, debug, modify, and better tolerate parameter changes and speed upgrades than asynchronous circuits.

sync word

A 32-bit word with a value that is used to synchronize the configuration logic.

synthesis

Optimization process of adapting a logic design to the logic resources available on the chip, like look-up tables, Longline, and dedicated carry. Synthesis precedes mapping.

TBUFs

Buffers with a 3-state option, where the output can be made inactive. Used for multiplexing different data sources onto a common bus. The pulldown-only option can use the bus as a "wired AND" function.

timing

Relating to delays, performance, or speed.

timing driven

A design or layout method that takes performance requirements into consideration.

UART

Universal asynchronous receiver/transmitter. An 8-bit parallel-to-serial and serial-to-parallel converter, combined with parity and start-detect circuitry, and sometimes even FIFO buffers. Used widely in asynchronous serial communications interface, e.g., modems.

USB

Universal Serial Bus, A low-cost, low-speed, self-clocking bit-serial bus (1.5 MHz and 12 MHz) using four wires (V_{CC}, ground, differential data) to daisy-chain up to 128 devices.

VME

Older bus standard, popular with MC68000-based industrial computers.

$\overline{\text{WRITE}}$ pin

The $\overline{\text{WRITE}}$ pin is an input to Virtex-II devices in the SelectMAP/Slave Parallel mode, indicating to the device which direction data is flowing on the Data bus. When $\overline{\text{WRITE}}$ is asserted (Low), data is entering the device (configuration). When $\overline{\text{WRITE}}$ is de-asserted (High), data is leaving the device (readback). If $\overline{\text{WRITE}}$ changes state when the device isn't expecting it, an abort occurs. For more information on the $\overline{\text{WRITE}}$ pin, refer to *The Programmable Logic Data Book* and "Design Considerations" on page 141.

XChecker cable

The Xilinx XChecker Cable (model DLC4) is a serial download cable. The XChecker uses a serial 9-pin interface to the communication port of a host computer and two 8-pin headers for flying-wire connectors to a target board. The XChecker cable is supported by the Hardware Debugger software for performing Slave Serial configuration and readback of FPGAs. The XChecker cable is also supported by the JTAG Programmer software for performing Slave Serial and Boundary Scan configuration of FPGAs, and Boundary Scan programming of CPLDs. For more information on using the XChecker cable refer to the *Hardware Users Guide* and the *Hardware Debugger Reference/Users Guide*.

XNF file

Xilinx-proprietary description format for a logic design. Alternative is EDIF.