Xilinx Fine-Pitch BGA and CSP Packages: The Technological Edge

Introduction

Rapid evolution of complex electronic systems and the demand for improved functionality at lower cost have resulted in the need for silicon products with smaller footprints. Advanced packaging options for the Virtex Series of FPGAs, such as the widely offered Xilinx fine-pitch Ball Grid Arrays (FG), have a tighter, 1.00-mm pitch versus the 1.5-mm and 1.27-mm pitches of conventional Ball Grid Arrays (BGAs). Xilinx is the first company in the programmable silicon market to offer Chip Scale Packages (CSPs) with a 0.8-mm pitch. This small form factor packaging solution has been used successfully with Xilinx XC9500 series CPLD products that contain up to 100,000 system gates, and it is being implemented for Virtex Series FPGAs with up to 200,000 system gates.

Xilinx Fine-Pitch BGA and CSP Advantages

A significant advantage of using fine-pitch BGAs and CSPs is the dramatic reduction in printed circuit board (PCB) real estate with an increase in I/O counts. Fine-pitch BGAs and CSPs are ideally suited for space-sensitive applications that provide package area reductions greater than 50% compared to traditional BGAs. Those packages also increase the I/O count (over 200%) in the same real estate compared to the previous generation of BGAs. Table 1 compares various features of the three package types discussed.

Table 1: **BGA/ Fine-Pitch BGA/ CSP Features Comparison**

Feature/Package	BGA	FG	CSP
Pin Count	256	256	280
Lead Pitch	1.27-mm	1.0-mm	0.8-mm
Package Dimension	27 x 27	17 x 17	16 x 16
Lead Count	1x	1x	1.1x
Package Area	1x	.4x	.35x

Additional Critical Package Features and Advantages

Xilinx fine-pitch BGAs are available in 256, 456, 676, 680, 860, 900, and 1156 solder ball arrays.

- The Xilinx fine-pitch BGA packages are based on the original Motorola BGA technology, which has a well-established worldwide supply base and infrastructure that ensures abundant substrate and assembly sources. These packages have a lower overall cost structure as well as the potential for rapid cost reductions in the future due to multiple sourcing.
- Board-level reliability of Xilinx fine-pitch BGA packages is far superior to that of Flex-based (polymide tape with one or two metal layers) packages for similar applications. Although Flex-based products have a smaller form factor, the package mechanical reliability is usually dominated by the die properties. Reliability worsens as the ball array is fully populated and the die size increases. For Flex-based packages, the coefficient of thermal expansion (CTE) mismatch between the package and the board is larger, resulting in a less reliable product than the Xilinx fine-pitch BGA solution.
- Table 2 illustrates the board-level reliability of fine-pitch BGAs compared to that of Flex-based packages of similar size. The data was gathered using a thermal cycling range of -40 to +125 °C. Almost all (approximately 98%) of the 484-pin Flex-based packages (23 mm x 23 mm) failed after 800 cycles at 1 cycle per hour in this temperature range. The

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676-pin fine-pitch BGAs from Xilinx, although larger in dimension (27 mm x 27 mm) than the 484-pin Flex-based BGAs, did not show any failure until 1350 cycles under the same conditions. Xilinx fine-pitch BGA packages comfortably meet the widely accepted industry requirement of 1000 cycles within a thermal range of -40 to +125 °C, whereas comparable Flex-based alternatives do not. This clearly indicates superior board-level performance of Xilinx fine-pitch BGA packages over Flex-based package alternatives adopted by other FPGA vendors.

Table 2: **System Reliability Comparison Between Flex-Based BGA And Xilinx Fine-Pitch BGA Packages**

Package Type (mm x mm) (1.00 mm ball pitch)	Number of Cycles at Which 10% of the Sample Population Failed	Number of Cycles at Which 98% of the Sample Population Failed
484-pin Flex BGA (22x22)	500	800
676-pin Fine-Pitch BGA (27x27)	1500	2000

- Xilinx fine-pitch BGA packages meet the JEDEC Level-3 moisture level specifications and are proven to be reliably manufacturable. Component reliability of Flex-based solutions is limited to smaller die sizes and packages. Xilinx Flex-based 0.8-mm pitch CSP solutions are offered with up to a 16 mm x 16 mm body size with JEDEC Level-3 moisture resistance. Larger Flex-based packages with greater than 450 I/Os can meet only JEDEC Level-4, at best.
- The Xilinx fine-pitch BGA packages have dedicated power and ground planes that enable improved noise immunity. Integral to the design are differential pairs and split planes for multiple references, which provide the superior electrical performance of fine-pitch BGAs, whereas single-layer or two-metal-layer Flex-based packages have serious limitations in thermal and electrical capacity enhancements.

  The Xilinx fine-pitch BGA is a BT-Laminate BGA, which means that the cavity-up FG can support relatively high power dissipation (approximately 4 watts) and the cavity-down FG has an added heat sink to further enhance its thermal and power dissipation capabilities.

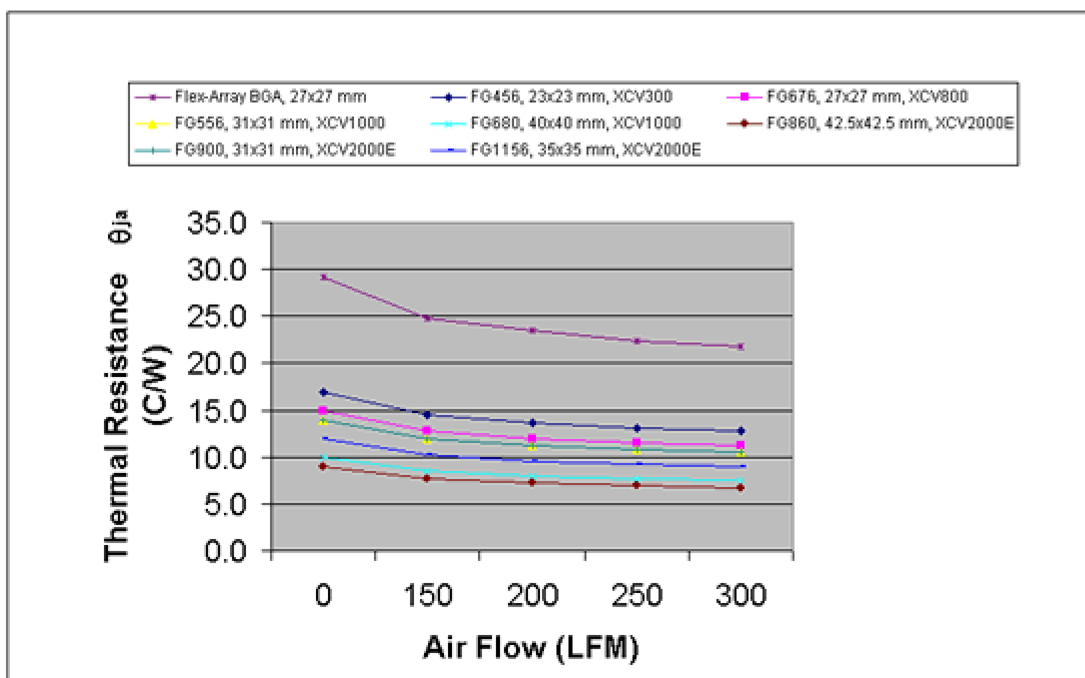


Figure 1: **Thermal Resistance Comparison Between Xilinx FG Products and Flex-Based Products**

- Figure 1 compares package thermal resistance data at different air flow rates for Flex-based packages and Xilinx fine-pitch BGA packages. Clearly, the fine-pitch BGA solution from Xilinx has lower thermal resistance than the Flex-based alternatives, which translates to better thermal performance and higher reliability.
- The fine-pitch BGA solution is capable of accommodating high performance future Xilinx products, especially in the Flip Chip format, with minimal changes in mechanical features. This package technology provides a smoother transition to high performance, high I/O solutions for our customer base, whereas Flex-based solutions are limited in their capacity to accommodate the additional I/O of future products.

Xilinx CSP/Fine-Pitch BGA Strategy

CSP

Xilinx has chosen the Flex-based technology for low-pin-count CSPs. Flex-based packages enable die shrink migration, while providing lower profile advantages for low-pin-count packages. Xilinx is the first company in the programmable logic industry to provide CSP packages for FPGAs and CPLDs adhering to the JEDEC Level-3 Moisture Resistance specification.

Fine-Pitch BGA Pin Array Compatibility

Xilinx provides flexibility by supplying Pin Array Compatibility (PAC) between the FG456 and FG676 packages. The PAC feature provides system designers the flexibility to lay out one printed circuit board (PCB) for these two fine-pitch BGA packages. Figure 2 demonstrates the compatibility of the two fine-pitch BGA packages.

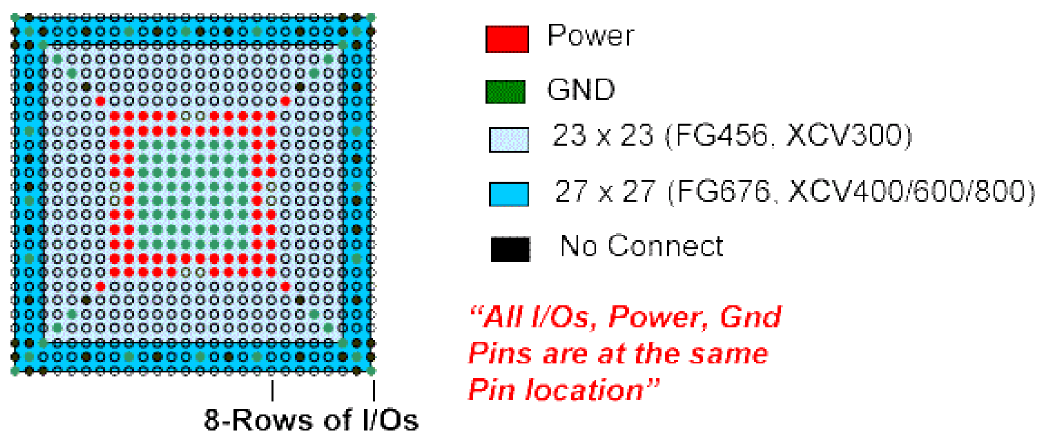


Figure 2: **Fine-Pitch BGA Pin Array Compatibility**

Xilinx Fine-Pitch BGA PCB Routability Advantage

The industry has recently started to adopt fine-pitch BGAs as a mainstream packaging technology. The 1.00-mm pitch packages can present both routing and silicon mount technology process challenges for users. Xilinx fine-pitch BGAs solve these challenges and present a definite advantage over Flex-based packages.

Figure 3 compares the I/O layout of a FG676 fine-pitch BGA package and a Flex-based package option. The fine-pitch BGA package is offered with I/Os that are 8 rows deep. This enables customers to use standard 6-mil trace/6-mil spacing manufacturing technology. Comparable Flex-based BGAs have I/Os that are 10-11 rows deep resulting in problems accessing all the pins using the standard board manufacturing technology.

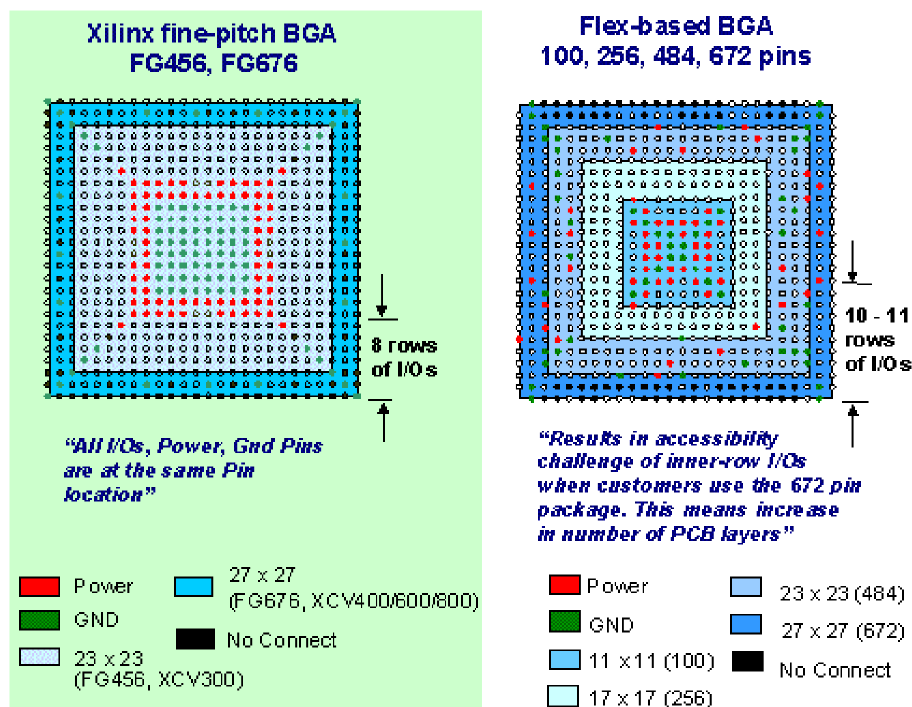
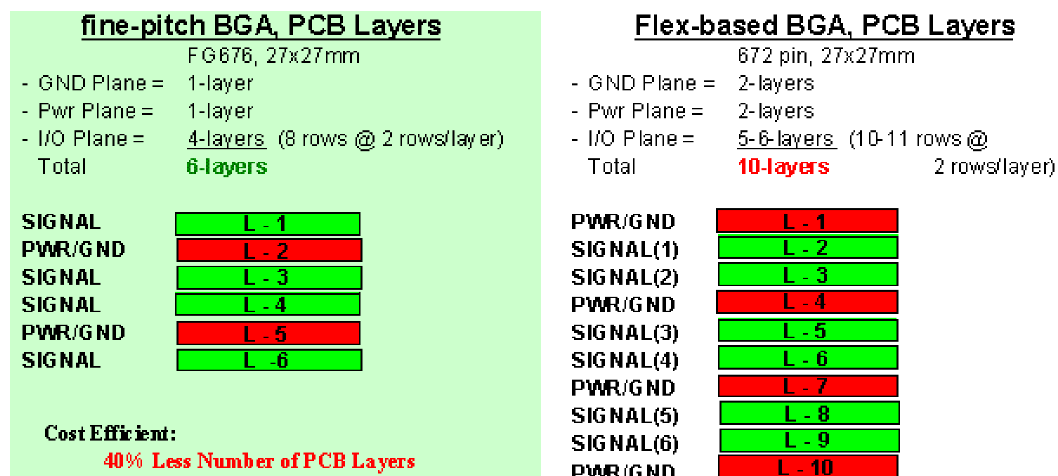


Figure 3: **I/O Layout Comparison of Xilinx Fine-Pitch BGA and Flex-based BGA Packages**

The result is more expensive 4-mil lines/trace technology, often with microvias or additional PCB layers for routing, (see Figure 4). This more complex manufacturing leads to higher system costs and lower reliability for customers using large Flex-based packages.



PCB Design Rules Used (1.0mm Ball Pitch)

	Trace Width/Spacing	I/O Rows	Lines per Channel	PCB Layer	Ball Pad	Via Hole	Via Pad
fine-pitch™ BGA	6/6 (current tech)	8	1	6	20	14	24
Flex-based BGA	6/6	10 - 11	1	10	20	14	24
	4/4 * (micro-via)	10 - 11	2	6	20	14	24

* micro-via = availability, higher cost, may require User qualification

Figure 4: **PCB Routing Comparison of Xilinx FG and Comparable Flex-Based BGA Package**

Mechanical samples with daisychained dies are available from Xilinx for evaluation purposes. Contact your local sales representative for details on ordering parts with package codes starting with FG (pin count)(daisychained).

Xilinx Fine-Pitch BGA and CSP Support

Table 3 summarizes the fine-pitch BGAs and CSP offerings available for the Virtex series Spartan series, and CPLD products.

Table 3: **Xilinx CSP and Fine-Pitch BGA Offering**

Package Type	Ball Count	Package Size	Max I/O	Height	Package Technology
Chip Scale (0.8 mm)	144	12x12 mm	94	1.10 mm	Flex-based CSP
	280	16x16 mm	196	1.20 mm	Flex-based CSP (Spartan™, CPLD)
Fine Pitch (1.00 mm)	256	17x17 mm	176	2.30 mm	Plastic Molded BGA
	456	23x23 mm	312	2.30 mm	Plastic Molded BGA
	676	27x27 mm	444	2.30 mm	Plastic Molded BGA
	680	40x40 mm	512	1.38 mm	Cu-Based "SBGA"
	860	42.5x42.5 mm	660	2.30 mm	Cu-Based "SBGA"
	900	31x31 mm	700	2.30 mm	Plastic Molded BGA
	1156	35x35 mm	804	2.30 mm	Plastic Molded BGA

Virtex and Virtex-E FPGAs, ranging in density from 50,000 to 3,200,000 system gates are the first FPGAs to fully support these advanced packaging options. The 144-ball CSP package option is provided for devices in the 50,000 and 200,000 gates densities, while the FG package option is provided for all devices in the family. The FG offering includes the FG256, FG456, FG680, FG860, FG900, and FG1156 packages.

To maximize system design flexibility, the Virtex series provides multiple device densities within a given fine-pitch BGA package. This vertical migration capability enables designers to lay out their boards prior to finalizing the FPGA design, thus gaining time-to-market advantages.

Table 4 illustrates the footprint compatibility of the 2.5V Virtex series, and Table 5 illustrates the footprint compatibility of the 1.8V Virtex-E series.

2.5V Virtex Family:

Table 4: **2.5V Virtex Series Package Offering Summary**

Package		Product								
		XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
CS144 (12mmx12mm)	I/O	94	94							
TQ144 (20mmx20mm)	I/O	98	98							
PQ240/HQ240 (32mmx32mm)	I/O	166	166	166	166	166	166	166	166	
BG256 (27mmx27mm)	I/O	180	180	180	180					
BG352 (35mmx35mm)	I/O			260	260	260				
BG432 (40mmx40mm)	I/O					316	316	316	316	
BG560 (42.5mmx42.5mm)	I/O						404	404	404	404
FG256 (17mmx17mm)	I/O	176	176	176	176					
FG456 (23mmx23mm)	I/O			260	284	312				
FG676 (27mmx27mm)	I/O						404	444	444	
FG680 (40mmx40mm)	I/O							512	512	512

1.8V Virtex-E Family:

Table 5: **1.8V Virtex-E Series Package Offering Summary**

Package	Differential Pairs		Product					
			XCV50E	XCV100E	XCV200E	XCV300E	XCV400E	XCV600E
CS144 (12mmx12mm)	30	I/O	94	94	94			
PQ240/HQ240 (32mmx32mm)	64	I/O	158	158	158	158	158	158
BG432 (40mmx40mm)	137	I/O				316	316	316
BG560 (42.5mmx42.5mm)	183	I/O						
FG256 (17mmx17mm)	83	I/O	176	176	176	176		
FG456 (23mmx23mm)	119	I/O			284	312		
FG676 (27mmx27mm)	183	I/O					404	444
FG680 (40mmx40mm)	247	I/O						512
FG860 (42.5mmx42.5mm)	281	I/O						
FG900 (31mmx31mm)	260	I/O						512
FG1156 (35mmx35mm)	344	I/O						

Package	Differential Pairs		Product				
			XCV1000E	XCV1600E	XCV2000E	XCV2600E	XCV3200E
CS144 (12mmx12mm)	30	I/O					
PQ240/HQ240 (32mmx32mm)	64	I/O	158				
BG432 (40mmx40mm)	137	I/O					
BG560 (42.5mmx42.5mm)	183	I/O	404	404	404		
FG256 (17mmx17mm)	83	I/O					
FG456 (23mmx23mm)	119	I/O					
FG676 (27mmx27mm)	183	I/O					
FG680 (40mmx40mm)	247	I/O	512	512	512		
FG860 (42.5mmx42.5mm)	281	I/O	660	660	660		
FG900 (31mmx31mm)	260	I/O	660	724			
FG1156 (35mmx35mm)	344	I/O	660	724	804	804	
CG1156 (35mmx35mm)	344	I/O					804

Virtex Advantages Summary

Xilinx packaging leadership addresses the industry demand for reduction in both system costs and size for portable systems. Xilinx offers 0.8-mm pitch CSP and 1.00-mm fine-pitch BGA packages that dramatically reduce board real estate and increase I/O counts for Virtex series FPGAs.

Designed with proven mainstream manufacturing flows optimized to handle these low-pitch packages, Xilinx CSPs and fine-pitch BGAs provide the following advantages for customers:

- Meeting the JEDEC Level-3 Moisture Resistance specification, thus enabling customers to maintain standard manufacturing flow/cycle time
- Lower thermal resistance data, translating to better thermal performance and eliminating cost for additional board-level cooling components (ex. Fan)
- Better board-level reliability, as indicated in the thermal cycle analysis in Table 2, providing higher system reliability and reduced cost for required rework
- Pin-out compatibility across the Virtex family, enabling customers to use the lowest cost package/device combination once the design is finalized
- Better routability, allowing customers to reduce overall system cost by reducing the number of layers needed per board and using standard board manufacturing technology

By combining these leading-edge CSP and FG packaging advantages with the Virtex high-performance system-level feature set, the Xilinx Virtex series FPGA is the ideal solution for creating reliable designs for next-generation high-performance systems.

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