High-Speed Transceiver Logic (HSTL)

Introduction

Virtex™ Series of FPGAs feature the Xilinx exclusive SelectI/O+™ technology integrating support for 20 single-ended and differential I/O standards. HSTL is one of the single-ended I/O interfaces supported by every Virtex device, eliminating the need for external level translators to interface with high-speed memories and reducing overall system design complexity and cost. Virtex FPGAs are the only PLD solutions with integrated HSTL I/Os for memory intensive designs.

The HSTL Standard

HSTL is a technology-independent interface standard for digital integrated circuits. It was developed for voltage scalable and technology independent I/O structures. The I/O structures required by this standard are; differential amplifier inputs (with one input internally tied to a user-supplied input reference voltage for single ended inputs), and outputs using output power supply inputs (V_{CCO}) that may differ from those operating the device itself.

Advantages

1. HSTL compliance does not specify device supply voltages, making it a process-independent I/O standard. The lower voltage-level swing associated with this standard makes high-speed HSTL I/O solutions possible for any core voltage level device.
2. A given circuit need not have all four classes of output drivers, but each circuit must have at least one of the four classes to claim HSTL output compliance.
3. The HSTL nominal logic switching range is 0.0 V to 1.5 V, resulting in faster outputs with reduced power dissipation, and minimized EMI concerns.
4. HSTL gives system designers enhanced flexibility in optimizing system performance with adjustable trip-point (V_{REF}) and output power supply voltage (V_{CCO}).

Applications

In computing, slow memory access times have traditionally hindered fast processor operations. In the mid-frequency range (between 100 MHz and 180 MHz), the I/O interface options for all single ended signals are; HSTL, GTL/GTL+, SSTL, and LVTTL. Beyond 180 MHz, the HSTL standard is the only single ended I/O interface available.

With HSTL speeds, faster I/O interface significantly improves overall system performance. HSTL is the I/O interface of choice for high-speed memory applications, and are ideal for driving address buses to multiple memory banks.

Terminated Loads

The HSTL I/O standard specifies the output characteristics for both series (Class II) and parallel (Class I, III, and IV) terminated loads. The limiting factors in high-speed digital I/O circuits are the typical transmission line effects (ringing, reflections, crosstalk, and EMI). Transmission line reflections are the greatest constraint. Controlling reflection requires impedance matching using parallel or series terminations.

There are four classes of HSTL output specifications depending on output drive requirements. Virtex devices support all the push-pull output buffers for parallel terminated loads (Class I, III, and IV.)

HSTL Class I Output Buffers

HSTL Class 1 output buffers have two types of loads:

- Push-pull output buffers for unterminated loads.
- Push-pull output buffers for symmetrically parallel terminated loads ($V_{TT} = V_{CCO}/2$).

It is not recommended to use the output buffers for unterminated loads because of signal integrity issues, specifically ringing, affecting overall performance by slowing down the outputs.

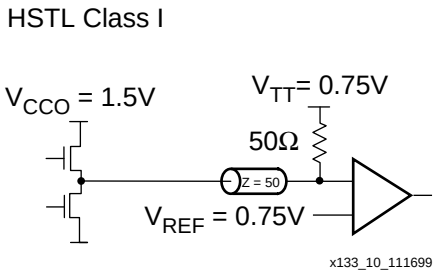


Figure 1: Symmetrically parallel terminated loads

Table 1: HSTL Class I Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}		$V_{CCO} \times 0.5$	
V_{IH}	V_{REF} + 0.1		
V_{IL}			V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4		
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	- 8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

HSTL Class III Output Buffers

Push-pull output buffers for asymmetrically parallel terminated loads ($V_{TT} = V_{CCO}$).

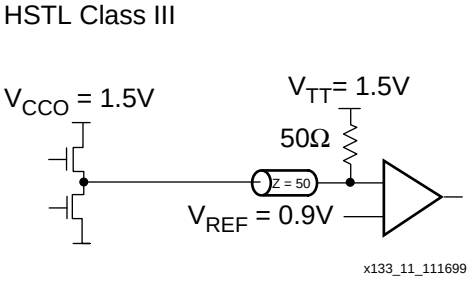


Figure 2: Asymmetrically parallel terminated loads

Table 2: HSTL Class III Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF} (1)		0.90	
V_{TT}		V_{CCO}	
V_{IH}	V_{REF} + 0.1		
V_{IL}			V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4		
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	- 8	-	-
I_{OL} at V_{OL} (mA)	24	-	-

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user.

HSTL Class IV Output Buffers

Push-pull output buffers for asymmetrically double parallel terminated loads (V_{TT} = V_{CCO}).

HSTL Class IV

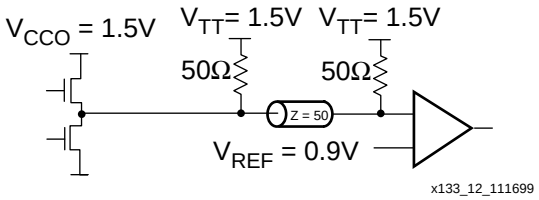


Figure 3: Asymmetrically double parallel terminated loads

Table 3: HSTL Class IV Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF} (1)		0.90	
V_{TT}		V_{CCO}	
V_{IH}	V_{REF} + 0.1		
V_{IL}			V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4		
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	- 8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user.

Notes

1. Customers may use IBIS models to compute the source impedance values.
2. Slew rate control is not provided for the HSTL I/Os.

Waveforms

The input pulse in Figure 6 is the input signal of Figures 4 and 5. This pulse was produced from a pulse generator. The output waveform shown in Figure 6 is observed at the node Z shown in Figures 4 and 5. As shown in Figure 6, the Virtex series HSTL I/O produces a substantial output swing from a very small input swing.

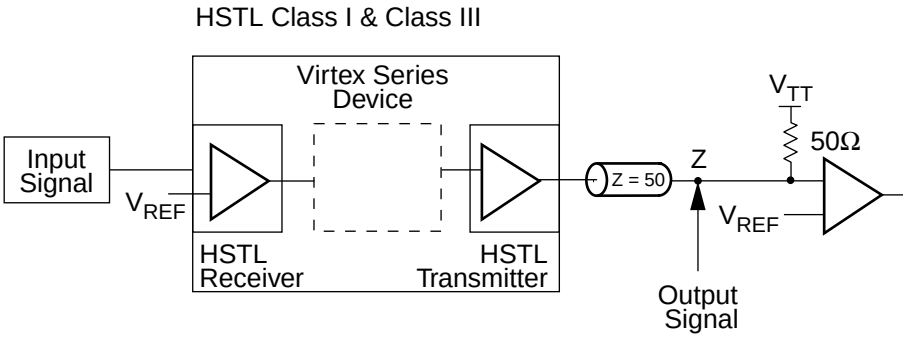


Figure 4: HSTL Class I and Class III Receiver/Transmitter

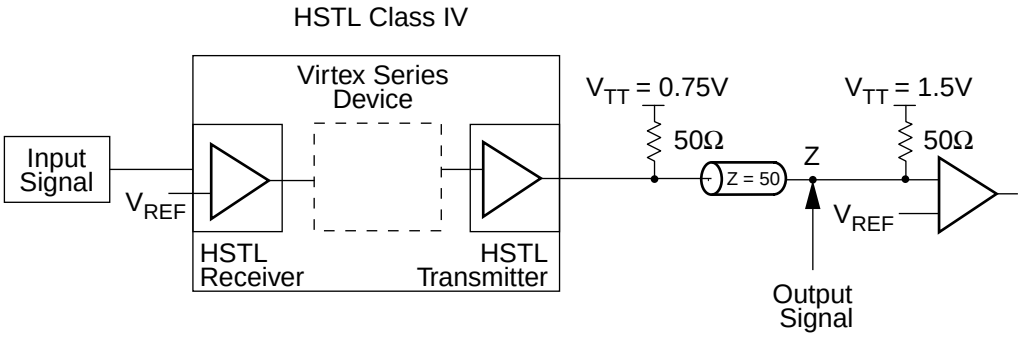
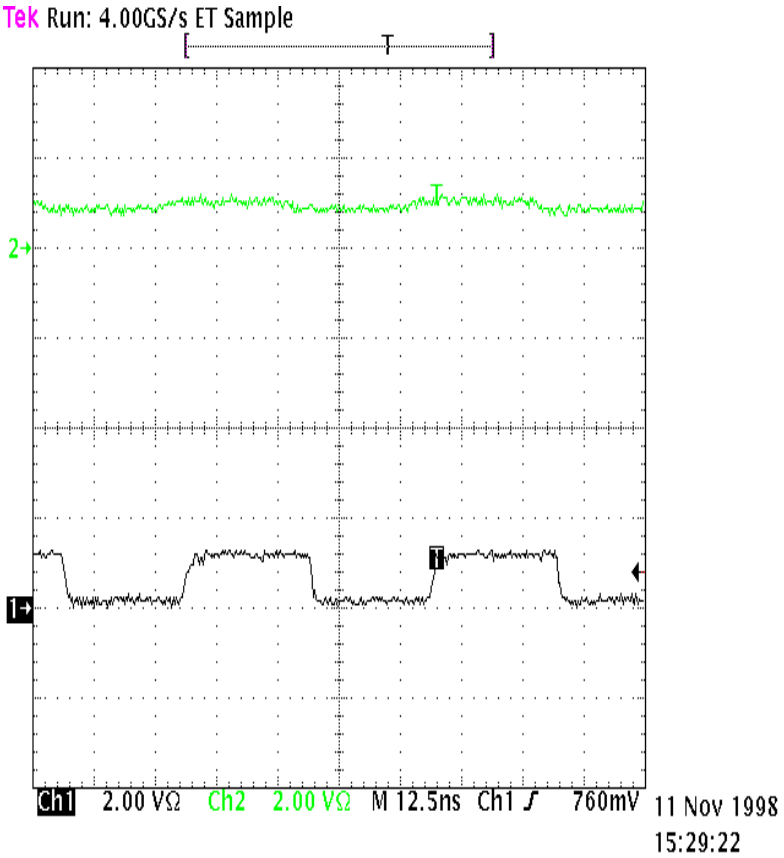


Figure 5: HSTL Class IV Receiver/Transmitter



Input Signal to Receiver

Output Signal from Transmitter

Figure 6: HSTL Signal Waveforms

Virtex Advantages

Using the Xilinx exclusive SelectI/O+ technology, the Virtex series delivers up to 804 single ended I/Os capable of supporting the HSTL standard listed in Table 4. With every I/O capable of supporting this array of I/O standards, the Virtex series of FPGAs provides maximum board lay-out flexibility. By reducing overall system design complexity and cost, the SelectI/O+ technology makes the Virtex series the ideal solution for direct interfacing to high performance memory devices. Virtex devices are the only FPGAs to support the HSTL I/O standard to seamlessly interface with other high performance HSTL standard devices.

Supported Standards

Table 4: HSTL standards supported by the Virtex series of devices

Standard	Virtex	Virtex-E
HSTL-I	√	√
HSTL-II	–	–
HSTL-III	√	√
HSTL-IV	√	√

References

Related Xilinx Documents

XAPP133: "Using the Virtex Select I/O" at: http://www.xilinx.com/xapp/xapp133.pdf

Standards

EIA/JEDEC STANDARD EIA/JESD8-6

http://www.jedec.org/download/freestd/jesd8-xx/default.htm

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