VIRTEX™

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5-Volt Tolerant I/Os

Introduction

To maintain technological leadership and continue to drive performance and logic density higher, chip manufacturers are constantly migrating to leading-edge fabrication processes. These processes continually decrease object geometry and consequently require lower core voltages to avoid damaging ever-smaller devices (3.3 V, 2.5 V, and 1.8 V are widely used).

While it is highly desirable to interface modern low-core-voltage devices with the older 5V devices that are still present on many customer boards, voltage and signaling differences frequently require the use of external voltage translator circuitry. The Virtex product family can interface directly with 5V systems without the need for translation circuitry. In fact, Virtex devices perform most efficiently in mixed-voltage systems. This tech topic addresses the Virtex and Virtex-E interfaces in mixed voltage systems.

In Virtex devices, all I/O standards have an intrinsic diode between the I/O pad and ground that limits undershoot to greater than -1 V. The LVCMOS 2.5V, LVTTL, and PCI 5V standards are all 5V tolerant (both inputs and outputs) and do not have a pull-up clamp enabled. The PCI 3.3V (both 33 MHz and 66 MHz) and AGP standards have the pull-up clamp enabled but are not 5V tolerant, because the clamp itself limits the output to 4.4 V maximum and sinks a significant amount of current when the pad voltage is raised above 4.4 V. The remaining I/O standards are not 5V tolerant and do not have the pull-up clamp diodes.

Note: This does not apply to the Virtex-II family of devices, which are 3.3 V compliant only.

Enhancements to the I/O structure of Virtex-E devices minimize pin capacitance and maximize performance. These differences, while conferring clear performance benefits for Virtex-E customers, also make the 5 V interface capability much more challenging.

Virtex-E devices are provided with a pull-up clamp diode between the I/O pad and V_{CCO}, which allows them to be 5V tolerant and reduces overshoot. The clamp diode is available with all I/O standards, excluding LVDS, LVPECL, GTL, GTL+, or LVCMOS1.8/2.5. To make Virtex-E devices using the LVCMOS I/O standard 5V tolerant, an external clamp diode must be provided. In Virtex-E devices, all I/O standards have an intrinsic diode between the I/O pad and ground that limits undershoot to greater than -1 V.

5V I/O Tolerance Definition

5V input tolerance is defined as the ability to connect an ideal 5.5V voltage source (assuming ±10% power supply tolerance) to the input pin of a device without damage. 5V-output tolerance is a little more complex, because there are two dominant 5V signaling standards: TTL and 5V CMOS.

Virtex and Virtex-E devices can each drive a 5V TTL input signal. Virtex-E devices cannot directly drive out 5V CMOS levels, because they cannot drive 5V CMOS V_{IH} levels. Table 1 summarizes the Virtex and Virtex-E capabilities as drivers of 5V-compatible signals.

Table 1: **Virtex Series FPGA 5V I/O Support Summary**

Driving Device	Receiving Device	Comments
Virtex	5V TTL	Yes
5V TTL	Virtex	Yes
Virtex	5V CMOS	Yes, provided the conditions in Note 1 are satisfied.
5V CMOS	Virtex	Yes
Virtex-E	5V TTL	Yes, provided nothing on the receiver device pulls a signal greater than 3.6 V.
5V TTL	Virtex-E	Yes, provided the conditions in Note 2 are satisfied.
Virtex-E	5V CMOS	No
5V CMOS	Virtex-E	Yes, provided the conditions in Note 3 are satisfied.

Notes:

1. Must tri-state outputs and use an external resistor to pull up to 5V.
2. Can drive only an input-only signal. The pin must be standard input (not GCLK, MODE, or JTAG), and the I/O standard must be clamp enabled (not LVDS, LVPECL, GTL, GTL+, or LVCMOS1.8/2.5).
3. Needs clamping to 3.6V, the selected I/O standard must not be LVCMOS1.8/2.5, LVDS, LVPECL, GTL, or GTL+. To use the LVCMOS1.8/2.5 standard, an external (voltage limiting) clamp diode must be provided in addition to the external resistor.

Using a Virtex Device to Drive 5V CMOS-Level Signals

To drive 5V CMOS-level inputs, a pull-up resistor must be applied to the 5V Virtex output. Prior to driving a logic 1 data signal, the Virtex output must be tri-stated. This ensures no overlap or crowbar current in the input buffers of the 5V-receiving device.

The required Virtex output pin configuration is commonly called “open collector”, or more correctly, “open drain”. This function is easily generated inside the chip by driving the data together with the active low Output Enable signal of the output block. The external low-to-high transition is then driven only by the pull-up resistor. For example, applying a 470-ohm pull-up resistor to 5V and a 50-pF load capacitance (as shown in Figure 1) creates a 0.4 to 4.5V rise time of about 40ns.

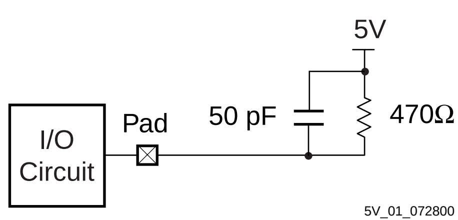

Figure 1: External Low-to-High Transition Example

For a faster rise time, the internal active low Output Enable signal is not driven directly from the internal data signal. Instead, it is driven from a two-input AND gate that is driven by both the internal data signal and the input signal returned from the same device’s output pin. On the rising edge, this assures that the output pull-up transistor is active for most of the rise time, resulting in a shorter output delay. The important part of the rise time from 0.4 to 3.0 V is reduced dramatically, from 20ns to 3ns (see Figure 2).

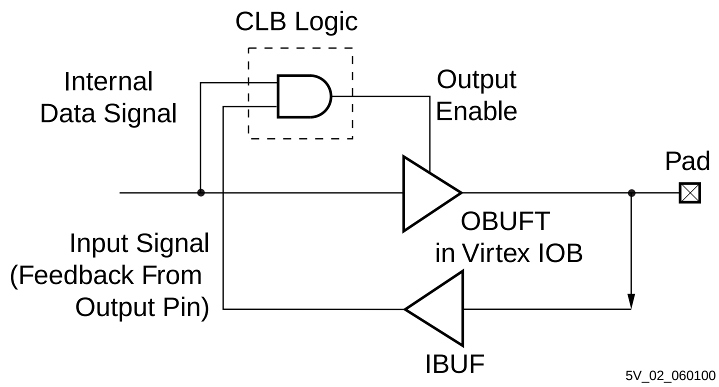

Figure 2: Transition Example Schematic

Ringing can be avoided by following proper board design practices. In most cases, the fast active edge enables the CMOS threshold to be passed with a propagation delay of less than 3ns. At worst, an additional pullup from the resistor is still needed to reach the threshold voltage reliably, but this enables at least 15ns to be saved.

Using a Virtex-E Device as a Receiver of a 5V TTL Signal

The internal clamp diode to V_{CCO} that is provided in Virtex-E devices with certain I/O standards, clamps the driving output to $V_{CCO} + V_{Diode}$ (approximately 4.4 V). This results in a large current sunk in the diode.

By inserting a series resistor, the current is limited to some reasonable value, for example 10 mA. An internal diode can clamp the I/O pad to the value of $V_{CCO} + V_{Diode}$. Including the series resistor minimizes the current sink created by the clamp. For example, the 100-ohm resistance value is applied to the Virtex-E inputs to ensure that Virtex-E device meets all specification for the LVTTL I/O standard. The 100-ohm resistance value needed on the Virtex-E inputs is calculated using the following formula:

$$R = (5V - V_{Diode} - V_{CCO}) / 10mA$$

Assumptions used to obtain the resistor values are as follows:

- Maximum current limit is 10mA.
- V_{Diode} is approximately 0.8V.

Note that applying a continuous voltage higher than 4.4V to the Virtex-E inputs that do not have a diode to V_{CCO} (for example; GCLK, MODE, and JTAG pins) is not allowed and damages the inputs. Although the damage might not be instantaneous, the long-term reliability of the design can be impacted.

A 5V device can drive a standard Virtex-E I/O pin (excluding GCLK, MODE, and JTAG pins), provided the following conditions are met:

- The Virtex-E pin is input only.
- The IBUF is configured to have a clamp to V_{CCO} (This is not possible with LVDS, LVPECL, GTL, GTL+, or LVCMOS1.8/2.5 I/Os).
- A current-limiting resistor (100 ohms) is placed in series with the pad.
- V_{CCOMAX} is 3.6V and V_{PADMAX} is 4.4 V. The Virtex-E device must never discharge a pad driver to a voltage higher than 3.6V. However, occasional ringing, which might cause the pad to rise above 3.6V momentarily, is not a problem.

Provided the above conditions are met, damage to Virtex-E devices can be avoided.

Possible Solutions for Clamping the Voltage to 3.6V

Solution 1: External Resistor Clamp Circuit

An external resistor divider circuit could be provided; however, the sizing of these resistors must be based on the I_{OH} and I_{OL} values specified for the 5V device. The I_{OH} and I_{OL} values are specified at V_{OH} and V_{OL} and are specified as worst-case low current, respectively. Since resistor clamps result in a voltage that is different from V_{OL}/V_{OH}, and drive current might exceed tested minimum values, drive current is likely to differ from the data sheet specification. The difference in the drive current makes this solution more difficult to implement.

Solution 2: External Active Clamp Circuit

Another solution that eliminates the need for external resistors is to have active clamp circuitry. Figure 3 shows a diode stack that limits the pad voltage to 3.6V or less.

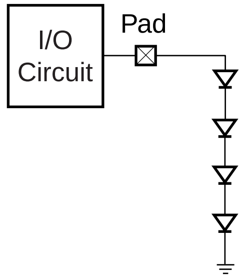

Figure 3: **Example** Diode Stack

Using a Virtex-E Device to Drive a 5V TTL Device

A Virtex-E part can drive an input-only signal on a 5V TTL device, provided that the 5V TTL V_{IL} and V_{IH} requirements are met. As long as no path to 5V exists for the driven device's pad, this solution works.

Virtex-E devices are not 5V PCI-compliant; however, a Virtex-E input-only signal can be driven by a 5V PCI part in a PCI system, provided that all of the requirements mentioned in Note 3 (see Table 1) are met. The effect of having a Virtex-E input-only signal on a PCI bus is to limit the maximum logic High value on that bus to V_{CCO} (for Virtex-E devices) + V_{Diode}. Another effect is the increased delay to the Virtex-E input-only pin, due to the current-limiting resistor. The current-limiting resistor can change the impedance of the bus, thereby impacting signal integrity.

Virtex Advantages

Virtex series FPGAs are capable of providing 5V-compatible I/Os. The original 2.5V Virtex family provided a direct interface to external 5V devices without any external glue logic/components, and the Virtex-E family can also interface with 5V devices when proper serial resistors or clamping circuitry are applied.

APEX devices have no recommendations for external clamping circuitry, since these devices are not characterized for 5V tolerance. For these reasons, Virtex series FPGAs are the ideal solution when designing high-performance systems with mixed voltage devices.

References

Refer to the following related Xilinx document:

- XAPP133: "Using the Virtex SelectI/O™ Resource" at: http://www.xilinx.com/xapp/xapp133.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/01/00	1.0	Initial Xilinx release.
02/07/01	2.0	Updated for Virtex-II release.