Superior Jitter Management with DLLs

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Summary

This Tech Topic presents the details and discusses the results of an experiment comparing the performance of Xilinx® Virtex™-E Delay-Locked Loops (DLLs) against Altera's Phase Locked Loops (PLLs) implemented in an FPGA. Designers get a better clock-skew management solution with DLLs on the Virtex Series FPGAs, compared with the high jitter amounts experienced when using APEX E PLLs in real applications.

Background

Two types of jitter described in Altera's technical brief are discussed in this Tech Topic, period jitter and cycle-to-cycle jitter. Period jitter is the deviation in time of any clock period from the ideal clock period (also known as "edge-to-edge" jitter). Peak-to-peak jitter defines an upper bound on the jitter. Cycle-to-cycle jitter is the deviation in clock period between adjacent or successive clock cycles

For the majority of digital systems, the most applicable jitter spec is period jitter. Digital designers consider this spec critical when the clock period determines the amount of data processing that can occur per clock cycle. For example, a 10.0 nsec period clock signal with period jitter of ±100 psec (min/max) can produce a clock period as low as 9.9 nsec and as high as 10.1 nsec. Guaranteeing flip-flop setup and hold times for tight timing budgets requires knowledge of the maximum period variation possible in the system clock signal.

Across a large number of samples, the cycle-to-cycle jitter can be either greater than or less than the "period jitter" of the same clock signal, depending on the characteristics of the clock signal. Cycle-to-cycle jitter is not as directly meaningful for digital systems as is period jitter.

Causes of Jitter

DLLs are completely digital circuits and, therefore, are much less susceptible to noise. Delay elements are inserted to remove skew from the clock and generate a new clock signal. Jitter on the input clock is directly passed on to the output clock leaving control to the designer over that aspect of the overall system design. Some random jitter is incurred by clock propagation through the DLL itself and the FPGA. In addition, as temperature and V_{CC} changes occur in the system, the clock signal drifts. To compensate, the DLL makes periodic adjustments of the delay elements. Thus, some deterministic jitter is added to the output clock in a periodic fashion.

In PLLs, noise causes the voltage controlled oscillator (VCO) to fluctuate in frequency. The control circuitry adjusts back to the specified frequency, but the change is seen as jitter. Other causes of jitter in PLLs are changes to V_{CC} and temperature.

In general, VCOs tend to be especially sensitive to switching digital circuitry surrounding the PLL, I/O switching, V_{CC}, and ground bounce. In fact, a less than optimal loop filter can amplify the jitter. Any noise can result in no lock or high jitter performance. On today's high-speed circuit boards, this puts an additional burden on the design and layout engineer to provide noiseless, separate power and ground connections. The DLL does not suffer from these limitations.

Therefore, the primary variable is noise. The noisier the environment, the greater the problem with analog PLLs. Altera has diagrams on their web site showing that their APEX E PLL jitter is less than the jitter for a DLL, based on measurements Altera took. However, the diagrams do not show that the measurements were taken in an ideal environment, with no analog system noise, and no switching of flip-flops. Xilinx obtained jitter measurements in a realistic environment for a true comparison of the jitter that designers see. The results are provided later in this document.

Experiment Details

To measure the true performance of a PLL implemented in an FPGA, the noise generated when a design switches digital circuits (flip-flops) was simulated. To run this experiment, the NIOS Development Board from Altera was selected. This board, designed and manufactured by Altera, was chosen to eliminate concerns about proper board layout technique. The board features a PLL-capable APEX EP20K200E-2X among other components, such as Memory, CPLD, clock distribution, and communications. In addition, various discrete components are on the board for decoupling and other tasks.

The clock source is a 33.3 MHz oscillator feeding a dual-clock distribution chip, which in turn feeds the APEX device. The APEX PLL output clock is fed to the other half of the clock distribution chip. Measurements were made at room temperature directly of the clock distribution chip. Two designs were loaded and the jitter was measured with a Wavecrest DTS2075, one of most accurate instruments on the market (±6 ps accuracy and resolution).

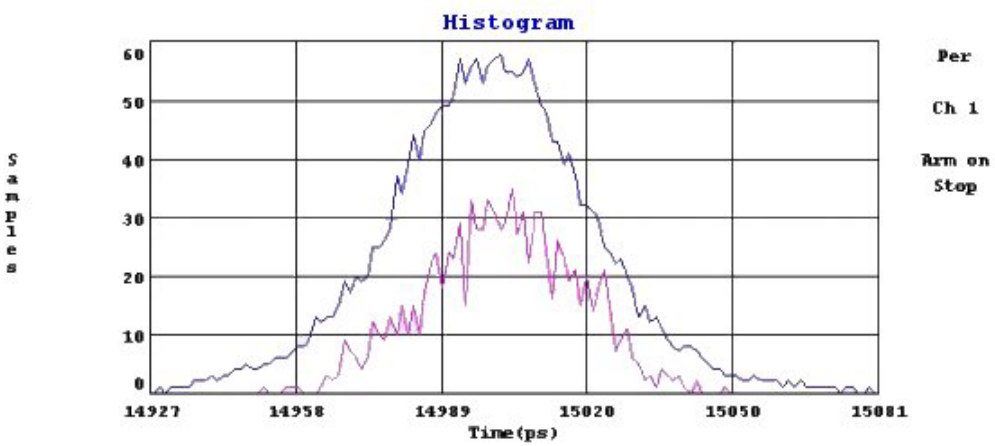
- **Design 1** used the PLL2 and a couple of flip-flops. The 33.3 MHz clock is multiplied by 2x and brought out on the dedicated clock output pin (CLKLK_OUT).
- **Design 2** also used the 33.3 MHz clock and 2x 66.6 MHz clock. In this design, 35% of the total available flip-flops were clocked by the 33.3 MHz clocked, and 35% of the flip-flops by the 66.6 MHz clock, for a total utilization of 70%. Again, we measured jitter on the 66.6 MHz clock.

None of the designs are toggling I/O to avoid any additional board-level noise that could make the clock jitter even worse. Of course, in a real application such noise does exist.

Results

Design 1

A single period with a peak at about 15 ns was observed. Jitter was 150 ps peak-to-peak at 1,000,400 clock samples. This jitter was expected and was well within the specification.



	Mean	1-Sigma	Pk-Pk	Maximum	Minimum	Samples	#Passes
Latest	15001.2	15.9	97.0	15048.2	14951.2	1000	
Overall	15000.8	15.7	151.4	15080.0	14928.6	1004000	1004

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Figure 1: **APEX E Peak-to-Peak Jitter with No Flip-Flops Switching**

Design 2

When measured, the jitter on the APEX E clock (see Figure 2) exhibited two peaks: a long one at 15.14 ns and a short one 14.87 ns. A total jitter of 665 ps peak-to-peak was observed when using the tail fitting option for 10E+12 clock cycles extrapolation. ***(Tail fitting fits a Gaussian right and left hand curve to the existing distribution to lessen the time it takes to get an accurate answer. Without tail fitting, such a measurement is likely to be far too optimistic. Wavecrest automatically calculates the Gaussian extension and reports it under the "TJ" header in the screen shot in each graph.)*** The 665 ps jitter clearly exceeds the data sheet specification by a factor of more than three times.

This means that the amount of jitter for a 66-MHz clock (with a period of 15015 ps) is about 4 percent of the clock period.

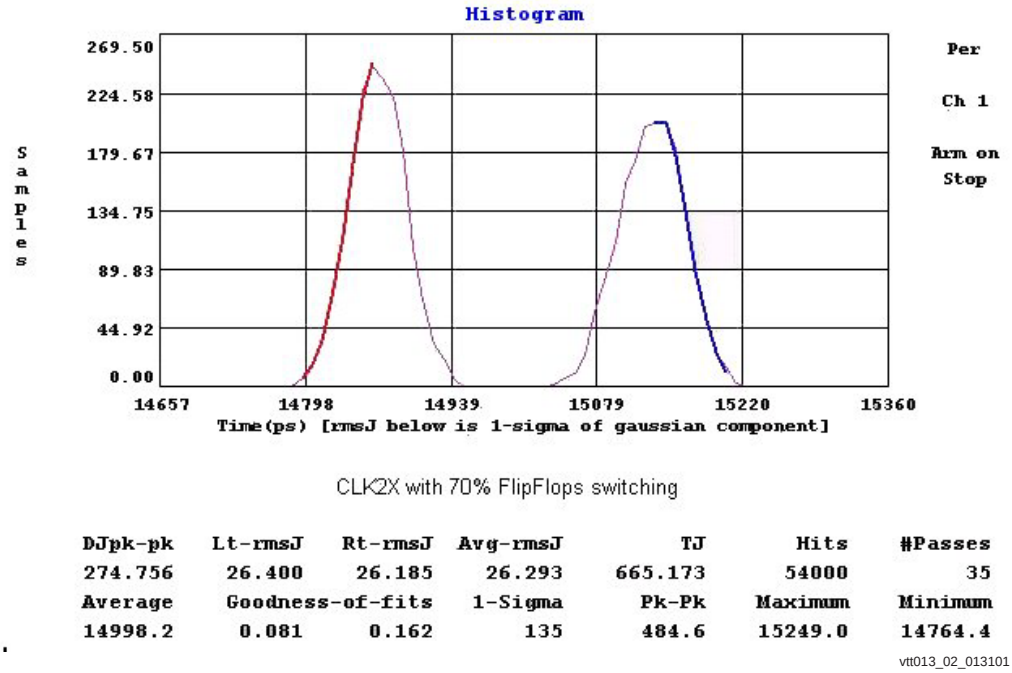
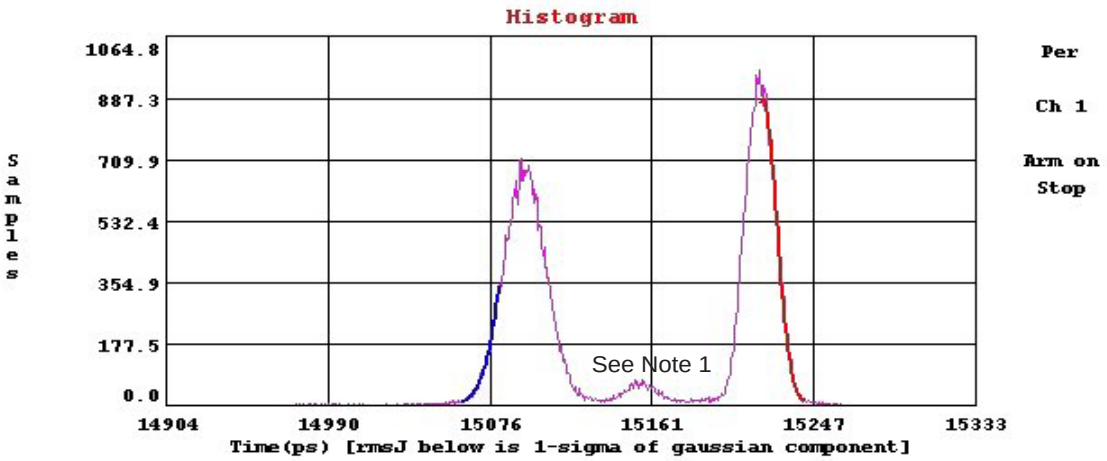


Figure 2: **APEX E Clock Skew with Flip-Flops Switching**

An identical experiment was run on the Virtex-E device. The part selected was the XCV300E, which has less flip-flops available than the EP20K200E. An identical amount of flip-flops was switched in exactly the same way as on the APEX E part, which resulted in a higher utilization than 70 percent. A Rode & Schwarz signal generator was used to produce the 33 MHz clock with a 57 ps jitter. When the jitter was measured on the Virtex-E clock, two peaks were also observed, but with a total jitter of 336 ps peak-to-peak (again using the tail fitting option). For the correct contribution of the DLL to the overall jitter, the input clock jitter of 57 ps needs to be subtracted from this number. See Figure 3 to compare that measurement to the 665 ps jitter measured in the exact same application in APEX E.



DJpk-pk	Lt-rmsJ	Rt-rmsJ	Avg-rmsJ	TJ	Hits	#Passes
187.264	13.309	7.256	10.282	336.157	65000	46
Average	Goodness-of-fits		1-Sigma	Pk-Pk	Maximum	Minimum
15156.8	0.740	1.338	62.1	289.3	15261.8	14972.5

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Note 1: A 33 MHz oscillator was used for the Virtex experiment, resulting in a period of 15151 ps and a higher center in the histogram.

Figure 3: **Virtex-E Jitter Measurement**

Conclusions

Conclusions of this experiment are as follows:

- DLLs control clock jitter caused by flip-flop switching better than PLLs.
- DLLs do not require separate power and ground planes on the PCB. Altera requires noise-free power and ground connections for APEX/APEX E PLLs.
- Using analog PLLs on an otherwise digital integrated circuit to manage clock skew presents a challenge. The designer needs accuracy and low noise, but has to make a trade off to achieve fast switching digital circuitry. The above experiment shows PLLs can work well if not much else is going on in the system. IHowever, if a majority of the flip-flops toggle at a high rate, then the switching modulates the VCO's frequency, resulting in an unacceptable amount of clock jitter. Adding I/O switching, or especially simultaneous switching I/Os, could compound the problem even further.
- DLLs give the designer control of the clock skew. Digital control is not susceptible to analog noise, voltage, or temperature variations, or the amount of on-chip I/O switching. In real applications, designers get a better clock-skew management solution with DLLs on Virtex Series FPGAs, compared with the high jitter amounts experienced when using APEX E PLLs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/31/01	1.0	Initial Xilinx release.
02/01/01	1.1	Minor edits done.