Xilinx and UMC Deliver Copper in New FPGA Family

Collaboration Sets Stage For Higher Performance FPGAs

Press Backgrounder

Over the past two years, Xilinx engineers have worked in close collaboration with UMC towards the development of copper-based FPGAs. Today, Xilinx is announcing the new Virtex-E Extended Memory FPGA family, the first programmable logic available with copper interconnect. This is a major breakthrough with long-term benefits for systems designers looking for maximum performance with minimum power dissipation. This document provides some technical background on UMC's damascene copper technology, its fabrication processes, and the corresponding benefits seen within Xilinx' FPGAs.

The natural evolution to copper

In order to meet ever-increasing bandwidth and density requirements, FPGAs must utilize the latest technologies to achieve the highest possible performance.

In today's leading-edge process technologies, the interconnect architecture is the key limitation for IC performance. Copper interconnect, with its superior resistivity and scalability over standard aluminum-based interconnect, will allow higher device performance and quicker migration into 0.15 micron and smaller geometries.

UMC and Xilinx have had a close technology partnership for many years, resulting in a tradition of technology leadership including:

- First FPGA shipped in 0.25 micron technology
- First FPGA shipped in 0.18 micron technology

Continuing this tradition, UMC and Xilinx delivers the first available FPGA employing leading-edge copper technology. The new Virtex™-EM family is manufactured in UMC's production fab, with the equipment and production facilities in place for production ramp-up.

This is a very significant step for the semiconductor industry, as UMC becomes the first dedicated foundry to ship product using copper technology. UMC joins an elite number of leading companies such as IBM, Motorola, and TI as among the first to have copper technology running in a production fab. The joint development between Xilinx and UMC on this technology allows Xilinx to ramp-up quickly on new high-performance FPGA families using copper technology for 0.18 micron and smaller geometries.

UMC's Damascene Copper Technology

- *Dual damascene copper interconnect*
- *Low-k dielectric*
- *Production fab*
- *Two layers moving to all layers*

Damascene copper processing is fundamentally different from aluminum processing. Copper is a softer metal than aluminum and is more difficult to deposit chemically and to remove with chemical etches. Therefore, damascene copper technology uses different steps and equipment than those used in aluminum processing. In the current copper process, trenches are created in the silicon dioxide insulator before the copper is applied. This is opposite to aluminum, where the insulator is patterned after the aluminum alloy is deposited. In the next step, inter-layer connections locations (electrical "vias") are patterned as open holes that expose the underlying metal layer at the bottom of certain trenches. A barrier metal is deposited to the entire wafer surface that covers not only the top side of the wafer, but also the trenches and the sides and bottom of the vias. Once the barrier metal covers the entire wafer evenly, copper is electroplated on top to the desired thickness.

The wafer then undergoes chemical-mechanical planarization (CMP), which is analogous to a chemically enhanced mechanical grinding process that levels the wafer. This step eliminates all copper and barrier metal except those within the trenched locations. The result is patterned islands of copper embedded within the insulator trenches, with an extremely flat surface suitable for further metal layers. The insulator uses a proprietary low-k dielectric material, which provides superior capacitance characteristics over standard silicon dioxide.

The initial copper and low-k dielectric is used in the top two of the six total layers of metal interconnect. This maximizes the benefits of copper for high performance devices by reducing internal voltage drops and clock skews while maintaining the mainstream aluminum capacity for faster production ramp-up.

New Technology Solutions

- *Copper CMP chemistry*
- *Metal pattern density*

A key requirement for copper technology is the clean removal of extraneous metal outside of the trenches without scratching the surface, which requires optimization of chemical slurries. Optimizing the CMP process to clean the surface without damaging the copper, one of the softest metals used in semiconductor processing, was a major challenge. The process must guarantee the uniformity of surface thickness of each layer. For example, large areas of copper will suffer a tapering effect whereby the center will be thinner than the edges. Xilinx and UMC engineers developed an algorithm for automatically equalizing the metal density, by adding dummy patterns in sparse areas and slotting large patches of metal.

Challenges of High Performance FPGAs

- *Interconnect limitations*
- *Power dissipation*
- *Power distribution*
- *Electromigration*

High-density field programmable gate arrays (FPGAs) have among the highest number of transistors of any integrated circuit. With continuing demand for faster time-to-market, shorter design cycles, and increasing logic complexity, this trend is expected to continue into the next decade. These complex FPGAs challenge process technologies to deliver increased transistor density, higher performance, and lower power dissipation per logic gate.

To understand the effects of exponentially increasing density and performance, consider the XCV2000E™ FPGA with over two million usable gates. These devices are typically used in systems with clock frequencies over 250 MHz and I/O speeds up to 622 Mbps. In such cases, the dynamic power dissipation of a fully utilized chip operating at 1.8 volts may exceed 10 watts, depending on the exact design and clock rates.

To support these types of designs, the internal chip is designed to withstand power dissipation substantially in excess of 20 watts over an operating lifetime in excess of 20 years. On-chip power distribution uses primarily the top two metal, which have the greatest metal thickness resulting in lower current density (i.e. amount of electrical current per cross-sectional area. Electromigration is caused by the flow of electrons that tend to push metal atoms out of the metal lattice, resulting in a gradual redistribution of the metallic lattice. If current density limits are exceeded over an extended period of time, the on-chip wiring can fail due to electromigration, whereby the wire becomes distorted and eventually disconnected.

With FPGA densities doubling approximately every 18 months, along with increasing internal clock frequencies, traditional process technologies are challenged to keep pace. For example, an FPGA that is twice the size of the XCV2000E device will have over 300 million transistors, with frequencies in excess of 500 MHz and dynamic power dissipation in excess of 15 to 20 watts. To meet such requirements using traditional aluminum alloy metalization, it would be necessary to either increase the power bus widths (which increasing overall chip size) or increase metal thickness (which reduces on-chip speeds). With both densities and performance increasing exponentially, the material limitations of aluminum are putting further Moore's Law predictions at risk.

Damascene Copper for High Performance FPGAs

- *Reduce voltage drop*
- *Minimize clock and signal skew*

The primary goal of the development effort between Xilinx and UMC was to provide an interconnect technology that enabled higher system performance. Two key areas that effect system speed degradation had to be addressed: (1) internal power supply voltage drop, and (2) clock and signal skew

For large, complex chips with substantial on-chip activity, there can be a significant difference between the external and internal power supplies. For example, a large chip driven by a stable 1.8-volt external power supply can operate at 1.6 volts or less internally, due to large operating currents that causes internal voltage drops. The performance of the internal circuitry can degrade by 15 percent or more if a 12 percent voltage reduction occurs. While this effect cannot be eliminated entirely, a substantially lower resistance power supply connection will minimize the performance degradation.

Clock and signal skew will also degrade system performance because of the need for added timing margin to neutralize their effect. This skew is caused by the relatively high resistance of the aluminum wiring compared to the variable capacitive loading at the outer reaches of the clock net. In a large chip, a key signal such as clock can experience on-chip skews of 0.5 to 1 nanosecond, which can degrade system performance by 10 percent for clock periods of 10 ns or less. The result is a localized RC delay effect at each destination that causes the clock signal to arrive at different nodes at different times. This effect can also be minimized with a lower resistance interconnection. Advanced copper interconnect technology can be used to replace aluminum alloy in the top two levels of metal to address these problems.

Looking Ahead

- *Damascene copper is the new standard*
- *All layer copper*

The advent of damascene copper for advanced interconnect is a revolutionary step, since the semiconductor industry that has used aluminum alloys since the invention of the integrated circuit. Xilinx and UMC will continue to develop processes that take advantage of copper for all metal interconnect layers, further improving performance and reducing power dissipation.

Conclusion

The drive toward further integration is causing a profound shift in interconnect technology. Copper is poised to take over the role of aluminum alloys for complex, high-density integrated circuits. UMC and Xilinx have jointly anticipated this need, and as a result of a two-year collaborative effort, developed production capabilities for new high-density FPGA products. This important milestone of being the first FPGA vendor to use production damascene copper technology will be key for both UMC and Xilinx to continue their respective leadership positions.

Figure 1: UMC/Xilinx Copper Interconnect Used in Production Fab.

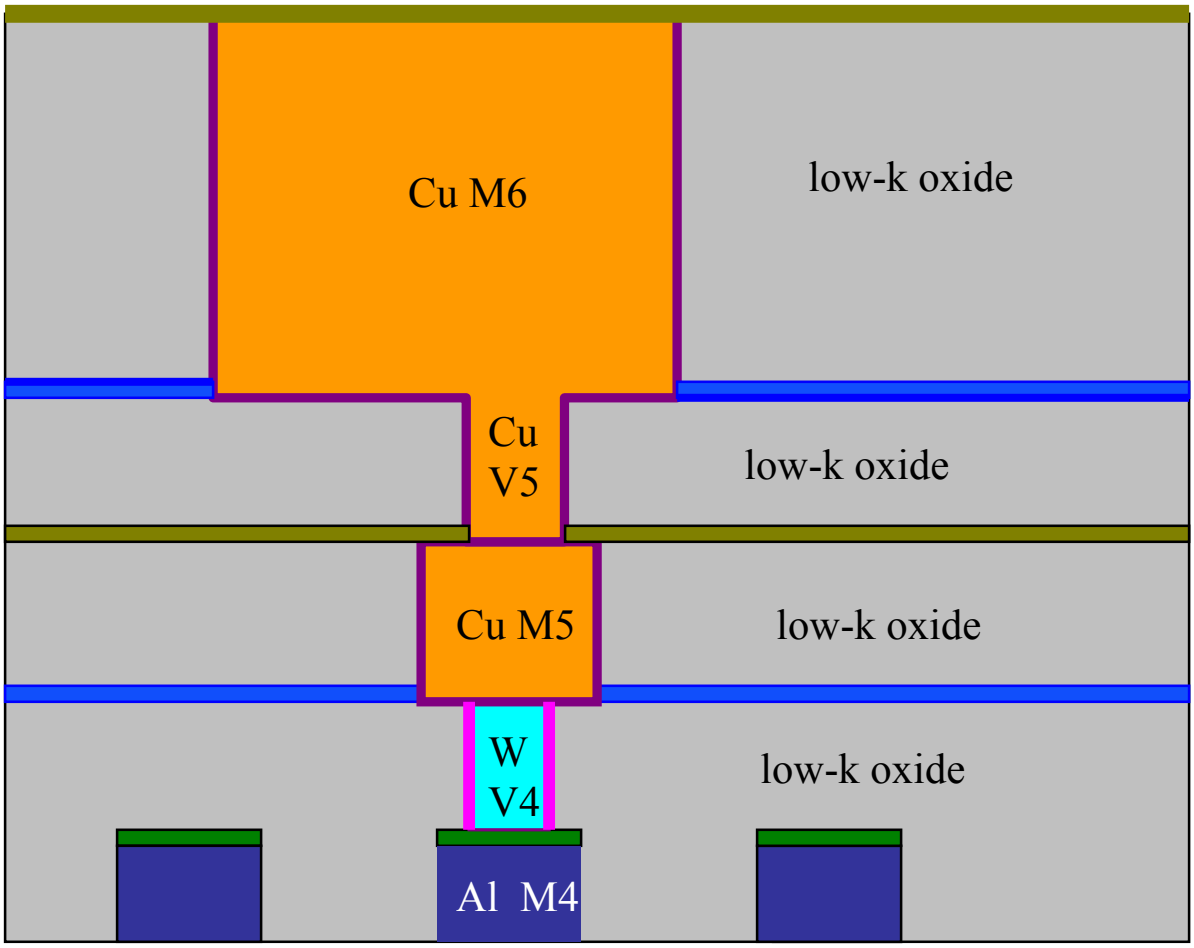

Figure 2: Copper Processing Steps.

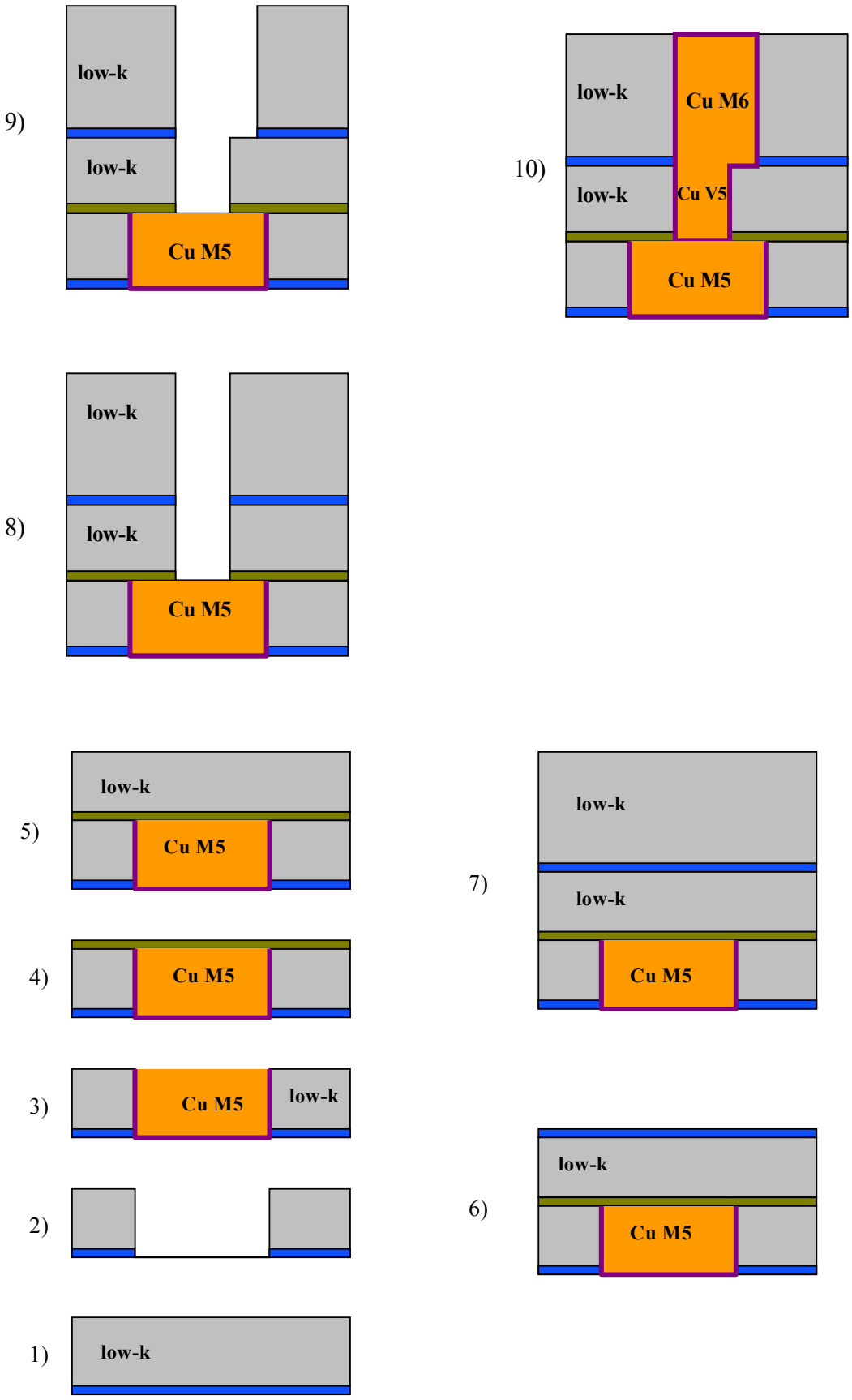

Figure 3: All-Layer Copper Interconnect.