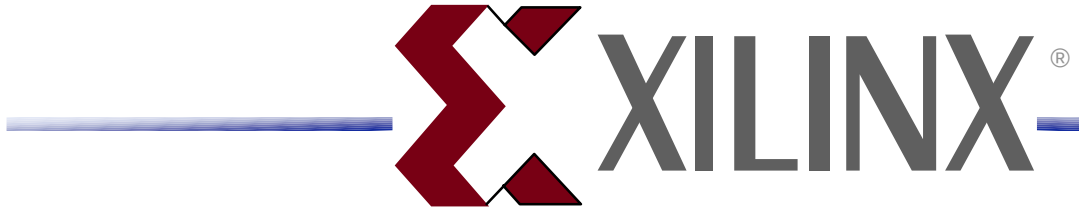


HDLC Controller Solutions with Spartan-II FPGAs - Customer Tutorial

February 2000

Agenda

- Introduction
- HDLC Overview
- HDLC Controller Applications
- Spartan-II IP Solutions for HDLC Controllers
- HDLC Controller ASSPs
- Spartan-II Family - Programmable ASSP
- Summary

Introduction

- Spartan-II FPGAs
  - 100,000 system gates at under $10
  - Extensive features: Block RAM, DLL, Select I/O
  - Vast IP portfolio
  - Provide Density, Features, Performance at ASIC prices

A Spartan-II FPGA Based Programmable HDLC Controller Solution Competes Effectively Against Stand-alone ASSPs

HDLC - the Protocol

- High-Level Data Link Control (HDLC) Protocol:
  - ISO defined
  - Bit-oriented, synchronous data link layer protocol
  - Specifies data encapsulation on synchronous serial links
  - Uses frame characters
  - Performs checksums (CRC)
  - Is a group of several protocols responsible for transmitting data between network points (nodes)
  - Organizes data into units and sends it across a network to a destination that verifies its successful arrival
  - Commonly used protocol in layer 2 of the OSI
  - Different variations are used in different networks

HDLC - The Protocol

- HDLC Protocol Structure:
  - Specifies a packetization standard for serial links
  - Supports several modes of operation, including a simple sliding window mode for reliable delivery
  - The Internet
    - Provides retransmission at higher levels (TCP)
    - Most Internet applications use HDLC's unreliable delivery mode, unnumbered information
- The Following Variations of HDLC Exist:
  - Both PPP and SLIP use a subnet of HDLC's functionality
  - ISDN's D-channel uses a slightly modified version of HDLC
  - Cisco routers' default serial link encapsulation is HDLC

HDLC - the Protocol

- HDLC Protocol's Frame Structure:
  - Flag characters
    - Marked at the beginning and end of HDLC frames - 01111110 binary
    - Do not appear in intervening data (enforced in a transparent manner)
  - FCS
    - Used at the end of the frame, to verify data integrity
    - Is a CRC calculated using the polynomial $x^{16} + x^{12} + x^5 + 1$
  - Between HDLC frames, the link remains idle
  - Synchronous links
    - Constantly transmit data
    - Transmit all 1s during the inter-frame period (mark idle), or all flag characters (flag idle)

What are HDLC Controllers?

- HDLC Controllers
  - Devices which perform the functionality of the HDLC Protocol
- General Functionality:
  - Handle bit oriented protocol structure
  - Format data as required by packet switching protocol
  - Transmit and receive data packets serially
  - Provide data transparency by zero insertion and deletion
  - Generate and detect flags that indicate HDLC status
  - Provide 16- or 32- bit CRC on data packets
  - Recognize the single byte address in the received frame

HDLC Controller Applications

- Frame Relay Switches (High Density Access & FRADs)
- ISDN (Basic-rate or primary-rate interfaces, D-channel)
- X.25 & V.35 Protocols
- High Bandwidth WAN Links:
  - Internet/Edge routers
  - Bridges and switches
- Cellular Base Station Switch Controller
- Error-Correction in Modems

HDLC Controller Applications

- T1/E1, T3/E3:
  - Channelized,
  - Clear channel (unchannelized)
- xDSL: Each Port can Support up to 10Mbps
- Dual HSSI
- SONET Termination
- Digital Sets, PBXs and Private Packet Networks
- C-channel Controller to Digital Network Interface Circuit
- Data Link Controllers and Protocol Generators

HDLC Controller Applications

- Inter-processor Communication
- Logic Consolidation
- CSU/DSU
- Protocol Converter
- Packet Data Switch
- Distributed Packet-based Communications System
- Multiplexer/Concenterators:
  - Remote Access
  - Multiservice Access

Spartan-II IP Solutions for HDLC Controllers

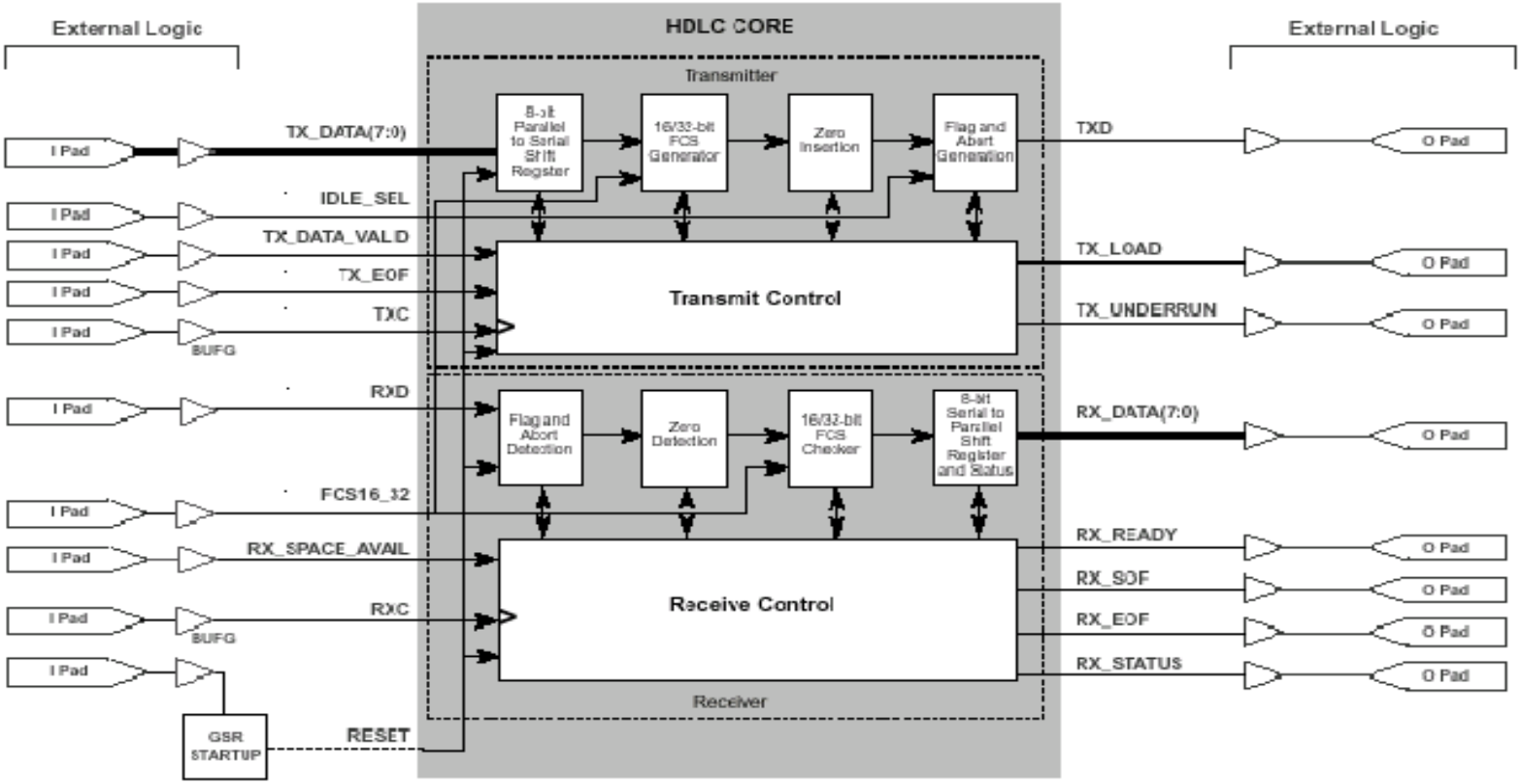
- AllianceCORE Partners
  - Memec Design Services
    - Single Channel XF-HDLC Controller core
  - CoreEl MicroSystems
    - PPP8 HDLC (CC318f) Controller core
- The Two IP Solutions are Crafted to Cater to Different Applications

Spartan-II + HDLC Controller IP =
Programmable HDLC Controller Solution

Spartan-II IP Solutions for HDLC Controllers

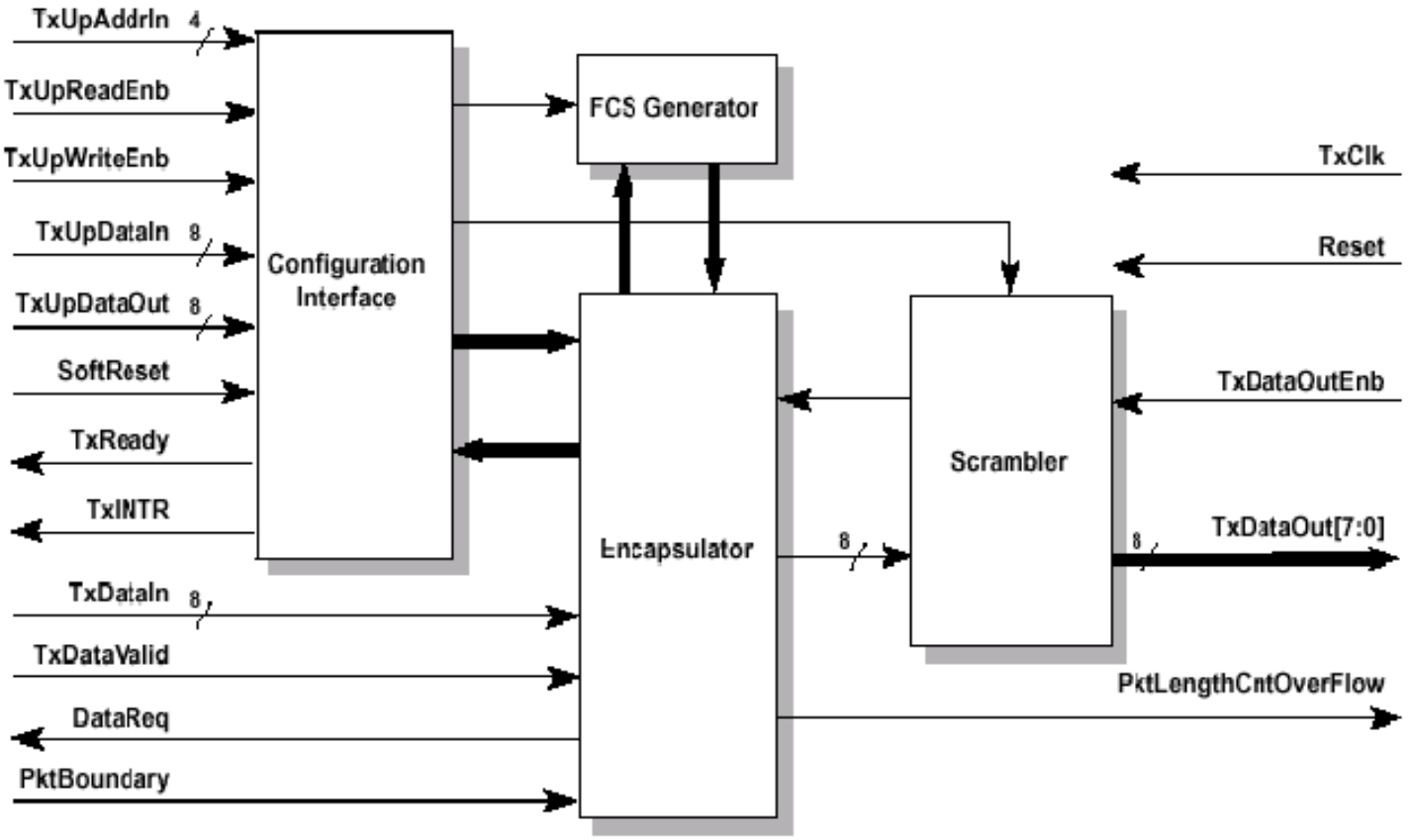
Xilinx IP Solutions for HDLC Controllers		
AllianceCORE Partners	**Memec Design Services**	**CoreEl MicroSystems**
Products/Cores	Single Channel XF-HDLC Controller	CC318f - PPP8 HDLC
Specification Standard	International ISO/IEC3309	RFC1619 PPP over SONET
Address Recognition	N.A.	N.A.
Data Rate	DC to 53Mbps (STS-1)	N.A.
CRC/FCS	16- & 32- Bit	16- & 32- Bit
FIFO customization	Yes	N.A.
DMA customization	Yes	N.A.
Multiple HDLC Scaling	Yes	Yes
Synchronous	Full	N.A.
Features	full duplex operation allowed	supports programmable address, control, protocol fields; supports 8-bit pkt & framer interface; error detection statistics
Supported Family	Spartan-II, Virtex	Spartan-II, Virtex, XC4000XL(-8)
Performance	N.A.	80MHz

Memec Design Services



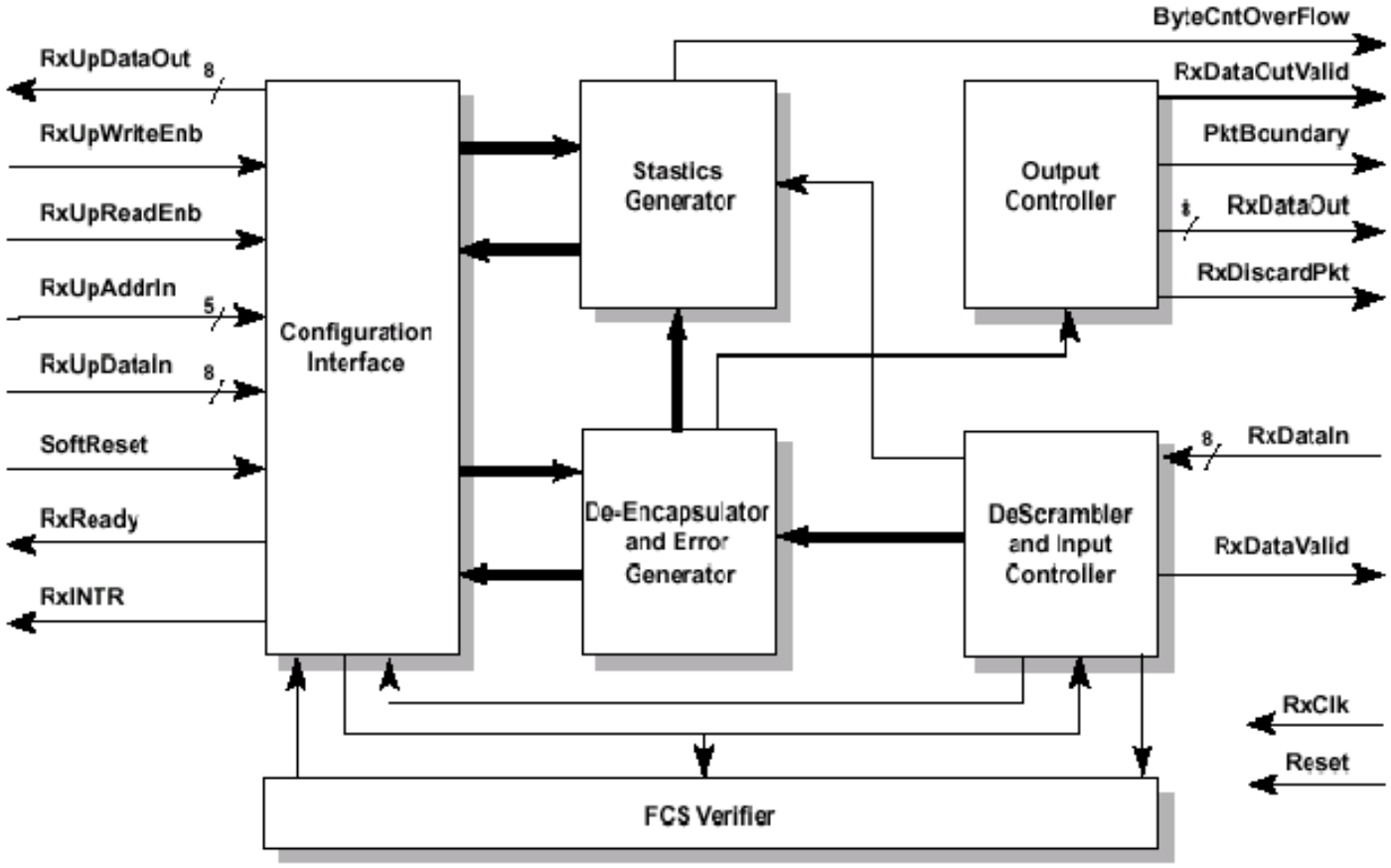
Single-Channel XF-HDLC Controller Block Diagram

CoreEl MicroSystems



CC318f HDLC Controller (Transmitter) Block Diagram

CoreEl MicroSystems



CC318f HDLC Controller (Receiver) Block Diagram

HDLC Controller ASSPs

- Some Key Players in the HDLC Controller Market:
  - Dallas Semiconductor Corporation
  - Mitel Semiconductor
  - Conexant Systems, Inc.
  - Infineon Systems - Siemens
  - PMC-Sierra, Inc.

Spartan-II Competitive Advantage

- Data Rate/Throughput for
  - Typical HDLC Controller ASSPs: ~ 2.5 - 8.192Mbps
  - Spartan-II HDLC Controller Solution: 53Mbps
- Flexibility in CRC Operation for
  - Typical HDLC Controller ASSPs: No flexibility
  - Spartan-II HDLC Controller Solution: 16- and 32-bit provided
- Cost (in 250k units) for
  - Typical HDLC Controller ASSPs: ~$4.56 (single channel), ~$60 - $120 (multi-channel)
  - Spartan-II HDLC Controller Solution: ~$3.95 (single channel), ~$10 (multi-channel)

Programmable ASSP - Value

- Benefits
  - Time to Market
  - Flexibility
    - Product Customization to meet customer needs
    - Adapt to Specification Updates
    - Feature Upgrades
    - Low risk evaluation of new market segments
  - Field Upgradability
    - Hardware and Software upgradability opens new applications
  - Efficiently Address Lower Volume Strategic Applications
  - Distribution and Inventory Management

Programmable ASSP Advantages

- Accommodate Specification Changes
  - Multiple standards and specification changes are accommodated
- Testing and Verification
  - What if the stand-alone ASSP does not perform as expected?
  - Being re-programmable, risk aversion is a tremendous value-add

Programmable ASSP Advantages

- Xilinx On-line - Field Upgradability
  - Remote update of Software and Hardware
  - Results in increased lifetime for a product
  - Enable product features per end-user needs
- Issues in Creating a Stand-Alone ASSP
  - Choosing the right ASSP
  - Product customization
  - Development cost and amortization
  - Spartan-II family has amortized cost by selling to the traditional PLD marketplace

Summary

- HDLC Controllers are Widely Used in a Range of Data Networking Applications
- The Spartan-II Family has Significant Strengths to Penetrate the Programmable HDLC Controller Marketplace:
  - Features
  - Performance
  - Scalability and Flexibility
  - Cost Effectiveness

Summary

A Programmable HDLC Controller Solution Competes Effectively Against Stand-Alone ASSPs