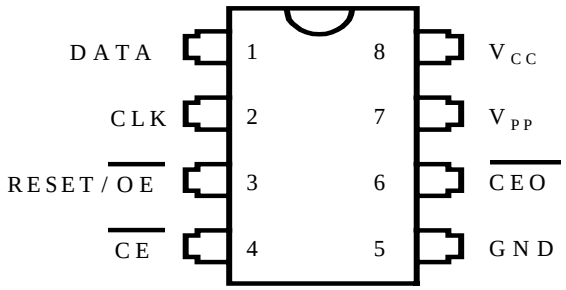
XILINX PROGRAMMER QUALIFICATION SPECIFICATION

1700E/X Family

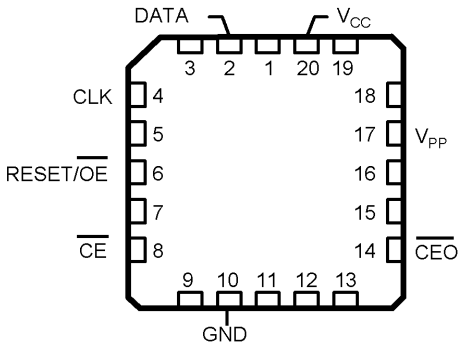
*Description

The XC1700E/X Families of Serial Configuration PROMs provide easy-to-use, cost-effective configuration memory for Xilinx Field Programmable Gate Arrays.

These devices use a simple serial-access procedure to configure one or more LCA devices. The user can select the polarity of the reset function by programming a special bit. These devices are fully compatible and can be cascaded with other members of the XC1700E or X Families.



8-Pin DIP/SOIC/VOIC Pin Assignments



20-Pin PLCC Pin Assignments

The XC1700E/X Family consists of one-time programmable (OTP) devices organized as follows:

XC1736E	36,288	x 1 bit
XC1765E	65,536	x 1 bit
XC1765X	65,536	x 1 bit
XC17128E	131,072	x 1 bit
XC17128X	131,072	x 1 bit
XC17256E	262,144	x 1 bit
XC17256X	262,144	x 1 bit

*** Note:** The low voltage devices, XC1765X, XC17128X, and XC17256X are also known as XC1765EL, XC17128EL, and XC17256EL

Programming Overview

All the XC1765E and XC1765X SPROMs are internally organized in rows, each row containing eight (8) 32-bit words. All of the XC17128E/XC17128X/XC17256E/ XC17256X SPROMs are internally organized in rows, each row containing eight (8) 64-bit words. Additional non-data rows are used to read the Manufacturer's/Device ID and set the Reset Polarity and cannot be used to store configuration data. The device programmer should prompt the user for the desired Reset Polarity.

Figure 1 shows the flow of how the SPROMs are programmed. See Figure 2 for the programming cycle overview and Figure 4 for the details of the programming cycle.

Enter Programming Mode

The programming mode is entered by holding $\overline{CE}$ and $\overline{OE}$ High with V_{PP} at V_{PP1} for two rising clock edges, then lowering V_{PP} to V_{PPNOM} for one more rising clock edge (See Figure 5). Once in the programming mode, the following functions are available.

Read Manufacturer's/Device ID

All of the SPROMs contain a Manufacturer's and Device identification code. Prior to attempting and to program or verify the device, the device programmer should read this code and verify that it is the correct code for the device selected by the user. If not, display message **"Manufacturing or Device ID Error."**

To read the Manufacturer's/Device identification code, first enter the programming mode.

For XC1736E/ XC1765E/ XC1765X:

While holding $\overline{CE}$ High and $\overline{OE}$ Low, apply 2056 clock signals to the clock pin to access the ID row.

For XC17128E/ XC17128X/ XC17256E/ XC17256X:

While holding $\overline{CE}$ High and $\overline{OE}$ Low, apply 4600 clock signals to the clock pin to access the ID row.

For All Devices

Then bring $\overline{OE}$ High and $\overline{CE}$ Low* . The first bit of the identification word is present when $\overline{CE}$ goes Low and does not require a clock. Apply 15 additional clock signals to the CLK pin to read the complete device ID.

The Manufacturer's/Device ID

Consisting of 2 bytes of data. The first byte contains the JEDEC assigned Manufacturer's ID code for Xilinx (C9). The first four bits of the second byte define the density of the PROM, while the last four bits of the second byte contain specific programming algorithm information (currently D for XC1700E and C for XC1700X). The data is read out MSB first.

The density codes are defined as follows:

XC1736E	E(1110)
XC1765E/X	F(1111)
XC17128E/X	8(1000)
XC17256E/X	A(1010)

Load a Data Word

The data word is shifted into the SPROM, one bit at a time, on the rising edge of the clock, while $\overline{CE}$ and $\overline{OE}$ are High. The data word is temporarily held in internal latches and is programmed into the memory as an entire word upon strobing the device with V_{PP} at V_{PP1} for $T_{PGM.}$

Increment the Address (Word) Counter

After programming a data word, the address counter must be incremented. This is done on the rising edge of the clock while $\overline{CE}$ is High and $\overline{OE}$ is Low.*

Set RESET Polarity

The polarity of the Reset/$\overline{OE}$ pin may be made active Low by writing zeros into a dedicated row.(See Figure 3).

For XC1736E/ XC1765E/ or XC1765X:
Reset/$\overline{OE}$ is located at row 257. Enter the programming mode, then lower Reset/$\overline{OE}$, hold the Data pin Low, strobe the clock 2048 times, load the data latches with all zeros (see Load a Data Word above), and strobe V_{PP} at V_{PP1} for 5 ms.

For XC17128E/ XC17128X/ XC17256E/ or XC17256X:

Reset/$\overline{OE}$ is located at row 514. Enter the programming mode, then lower Reset/$\overline{OE}$, hold the Data pin Low, strobe the clock 4104 times, load the data latches with all zeros (see Load a Data Word above), and strobe V_{PP} at V_{PP1} for 5 ms.

The reset polarity has to be verified (sensed) at V_{PP2} while in programming mode. To sense the polarity bit, set $\overline{CE}$ low and sense the $\overline{CEO}$ pin. If $\overline{CEO}$ is high, reset is active low (successfully programmed). If $\overline{CEO}$ is low, reset is active high (failed to program).

Writing ones or not writing anything maintains RESET active High.

Note:
The Reset Polarity is actually only the MSB of the data word.

* Be careful not to have $\overline{CE}$ and $\overline{OE}$ Low at the same time, as this causes the device to exit programming mode.

Sensing RESET Polarity

To sense or read the polarity of the Reset/$\overline{OE}$ pin, enter the programming mode, then lower Reset/$\overline{OE}$, hold the Data pin High, then:

For XC1736E/ XC1765E/ XC1765X:

Strobe the clock 2048 times.

For XC17128E/ XC17128X/ XC17256E/ XC17256X:

Strobe the clock 4104 times.

For all devices:

Set $\overline{OE}$ High, set $\overline{CE}$ Low and sense the $\overline{CEO}$ pin. If $\overline{CEO}$ is High, Reset is active Low. If $\overline{CEO}$ is Low, Reset is active High.

The reset polarity bit is defaulted (unprogrammed) to active high. When the reset bit is programmed, the “reset” polarity is active low.

Exit Programming Mode

To exit the programming mode, remove power from the device, per Figure 6.

Stand Alone Verify Of Data Bits (Normal Mode)

The verify operation should be performed after programming. Power up the device and read the data bits out serially in normal readout mode (see Figure 7). A margin voltage (difference between VPP and VCC) is applied to the device to ensure charge retention on each programmed bit. Set V_{CC} to V_{CCVFY} and V_{PP} to V_{PPVFY}. When in normal mode, the Reset/$\overline{OE}$ signal should be driven active high if the reset polarity bit was unprogrammed (logic “1”). It should be driven active low if the reset polarity bit was programmed (logic “0”).

At the end of the verify operation the programmer must confirm that the $\overline{CEO}$ pin has gone Low one clock after the last bit is read out.

If the data fails to verify, display message **“Failed Margin Verify”**. If the data verifies, display message **“Device Passed”**.

Programming Mode Pin Assignments

DIP/ SOIC/ VOIC Pin	PLCC Pin	Name	I/O	Description
1	2	Data	I/O	The rising edge of the clock shifts a data word in or out of the SPROM one bit at a time.
2	4	CLK	I	Clock input. Used to increment the internal address/word counter for reading and programming.
3	6	RESET/$\overline{OE}$	I	The rising edge of CLK shifts a data word into the PROM when $\overline{CE}$ and $\overline{OE}$ are High; it shifts a data word out of the PROM when $\overline{CE}$ is Low and $\overline{OE}$ is High. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held High and $\overline{OE}$ is held Low. Note: Any modified polarity of the RESET/$\overline{OE}$ pin is **ignored** in the programming mode.
4	8	$\overline{CE}$	I	The rising edge of CLK shifts a data word into the PROM when $\overline{CE}$ and $\overline{OE}$ are High; it shifts a data word out of the PROM when $\overline{CE}$ is Low and $\overline{OE}$ is High. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held High and $\overline{OE}$ is held Low.
5	10	GND		Ground pin
6	14	$\overline{CEO}$	O	The polarity of the RESET/$\overline{OE}$ pin can be read by sensing the $\overline{CEO}$ pin. Note: The polarity of the RESET/$\overline{OE}$ pin is ignored while in the programming mode. In final verification, this pin must be monitored to go Low one clock cycle after the last data bit has been read.
7	17	V_{PP}		Programming Voltage Supply. Programming mode is entered by holding $\overline{CE}$ and $\overline{OE}$ High and V_{PP} at V_{PP1} for two rising clock edges and then lowering V_{PP} to V_{PPNOM} for one more rising clock edge. A word is programmed by strobing the device with V_{PP} for the duration T_{PGM}. V_{PP} must be held at V_{CC} for normal operation.
8	20	V_{CC}		V_{CC} power supply input.

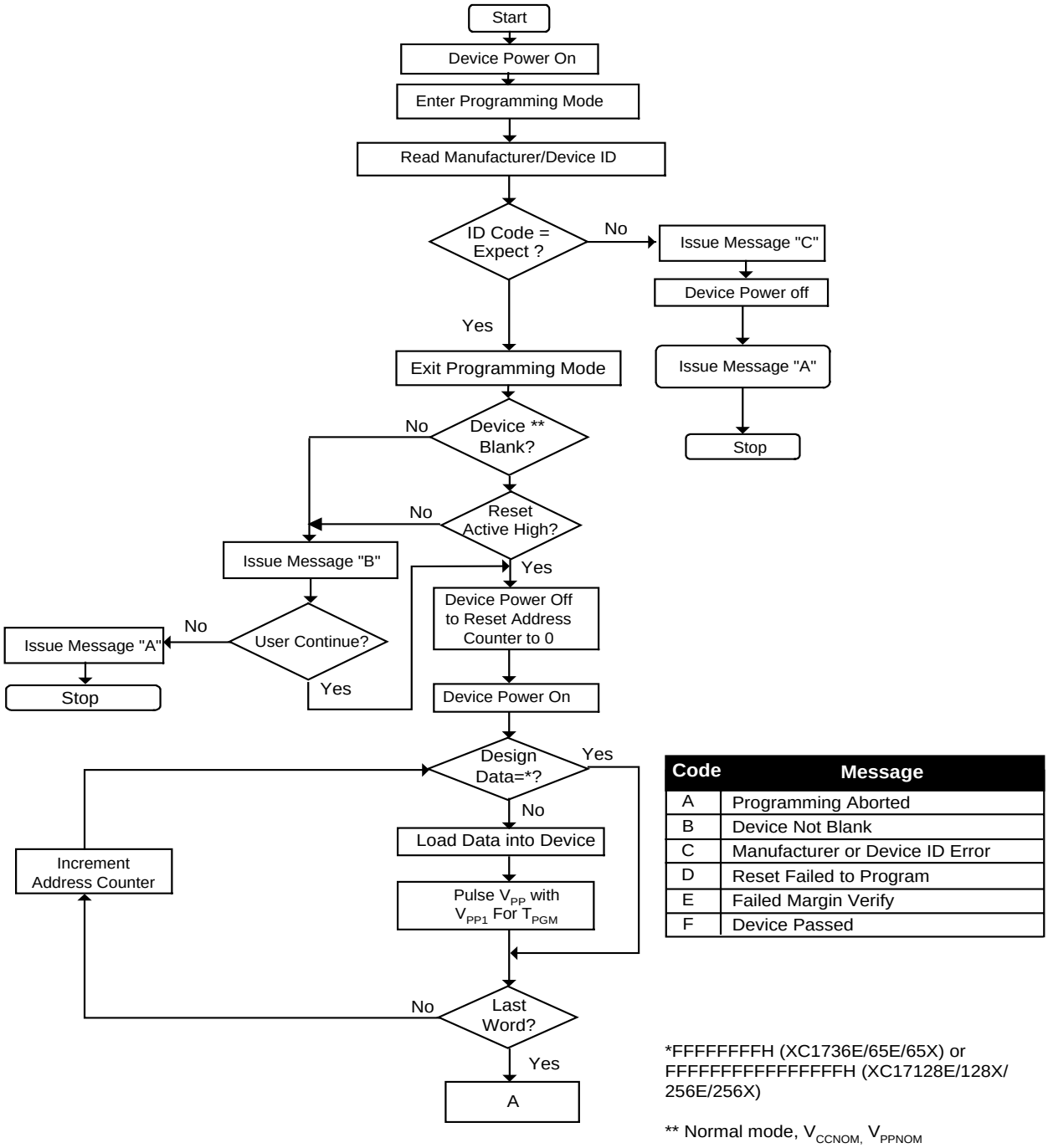
DC Programming Specifications

Symbol	Description	Min	Recommended	Max	Units
V_{CCP*}	Supply voltage during programming		5.0		V
V_{IL}	Low-level input voltage	0.0	0.0	0.5	V
V_{IH}	High-level input voltage	2.4	V_{CC}	V_{CC}	V
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	2.5			V
V_{PP1**}	Programming voltage	12.0	12.25	12.5	V
V_{PP2***}	Margin verify voltage during programming		5.4		V
I_{PPP}	Supply current on programming pin			60	mA
V_{CCNOM}/V_{PPNOM}	Nominal Voltage		5.0		V
V_{CCVFY} (1736E/65E/128E/256E)	Supply voltage during stand alone margin verify		5.0		V
V_{CCVFY} (1765X/128X/256X)	Supply voltage during stand alone margin verify		3.3		V
V_{PPVFY} (1736E/65E/128E/256E)	Margin voltage during stand alone margin verify		5.4		V
V_{PPVFY} (1765X/128X/256X)	Margin voltage during stand alone margin verify		3.7		V

* Noise and voltage deviation allowed: 5.0V ± 50 mV.
** No overshoot is permitted on signal. V_{PP} must not be allowed to exceed V_{PP1} max.
*** Noise and voltage deviation allowed: 5.4V ± 250 mV.

AC Programming Specifications

Symbol		Description	Min	Rec	Max	Units
1	T_{RPP}	10% to 90% rise time of V_{PP}	5	5	70	µs
2	T_{FPP}	90% to 10% fall time V_{PP}	5	5	70	µs
3	T_{PGM}	V_{PP} programming pulse width	0.95	1.0	1.05	ms
4	T_{SVC}	V_{PP} setup to CLK for entering programming	100			ns
5	T_{HVC}	V_{PP} hold from CLK for entering programming	300			ns
6	T_{SDP}	Data setup to CLK for programming	50			ns
7	T_{HDP}	Data hold from CLK for programming	0			ns
8	T_{SCC}	$\overline{CE}$ setup from programming/verifying	100			ns
9	T_{ON}	Reset Pulse Width	1			ms
10	T_{SCV}	$\overline{CE}$ hold from CLK for programming/verifying	100			ns
11	T_{HCV}	$\overline{CE}$ hold from V_{PP} for programming	50			ns
12	T_{SIC}	$\overline{OE}$ setup to CLK for incrementing address	100			ns
13	T_{HIC}	$\overline{OE}$ hold from CLK for incrementing address	0			ns
14	T_{CAC}	CLK to data valid			400	ns
15	T_{OH}	Data hold from CLK	0			ns
16	T_{CE}	$\overline{CE}$ low to data valid			250	ns

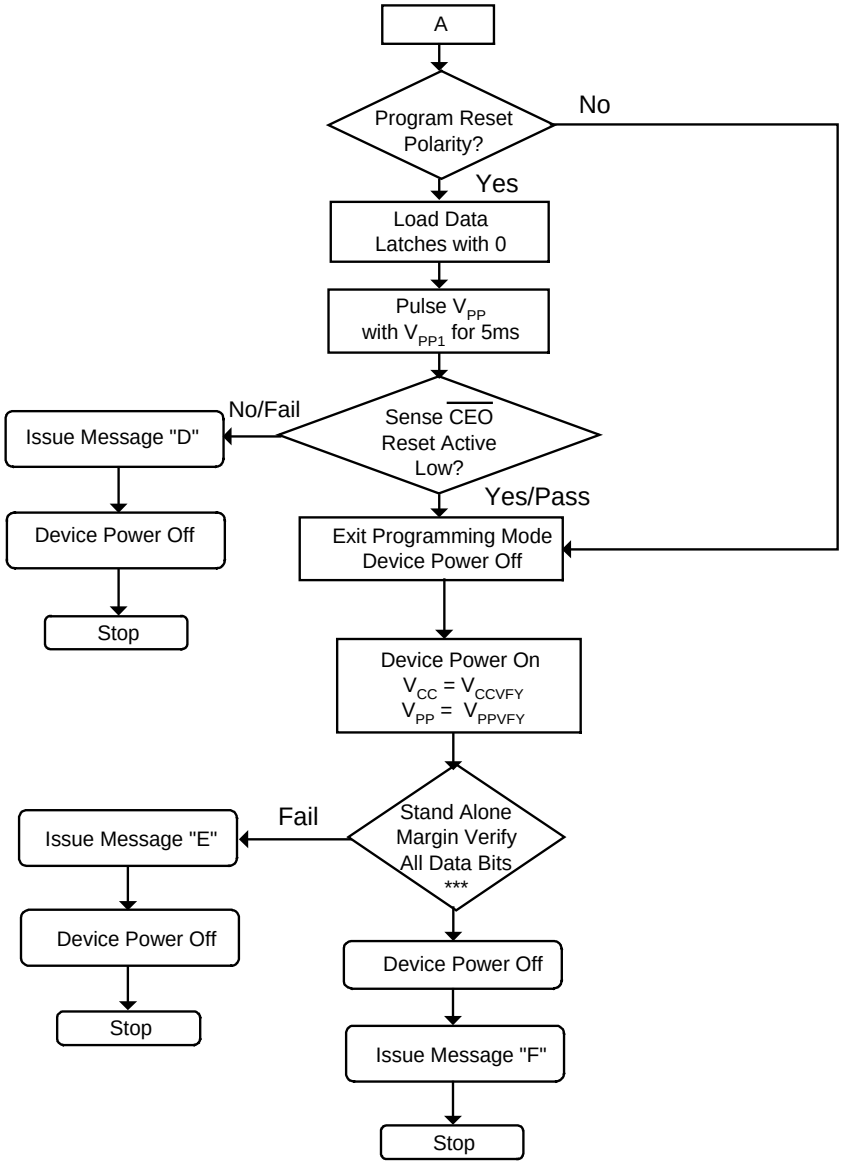


Code	Message
A	Programming Aborted
B	Device Not Blank
C	Manufacturer or Device ID Error
D	Reset Failed to Program
E	Failed Margin Verify
F	Device Passed

*FFFFFFFFH (XC1736E/65E/65X) or FFFFFFFFFFFFFFFFH (XC17128E/128X/256E/256X)

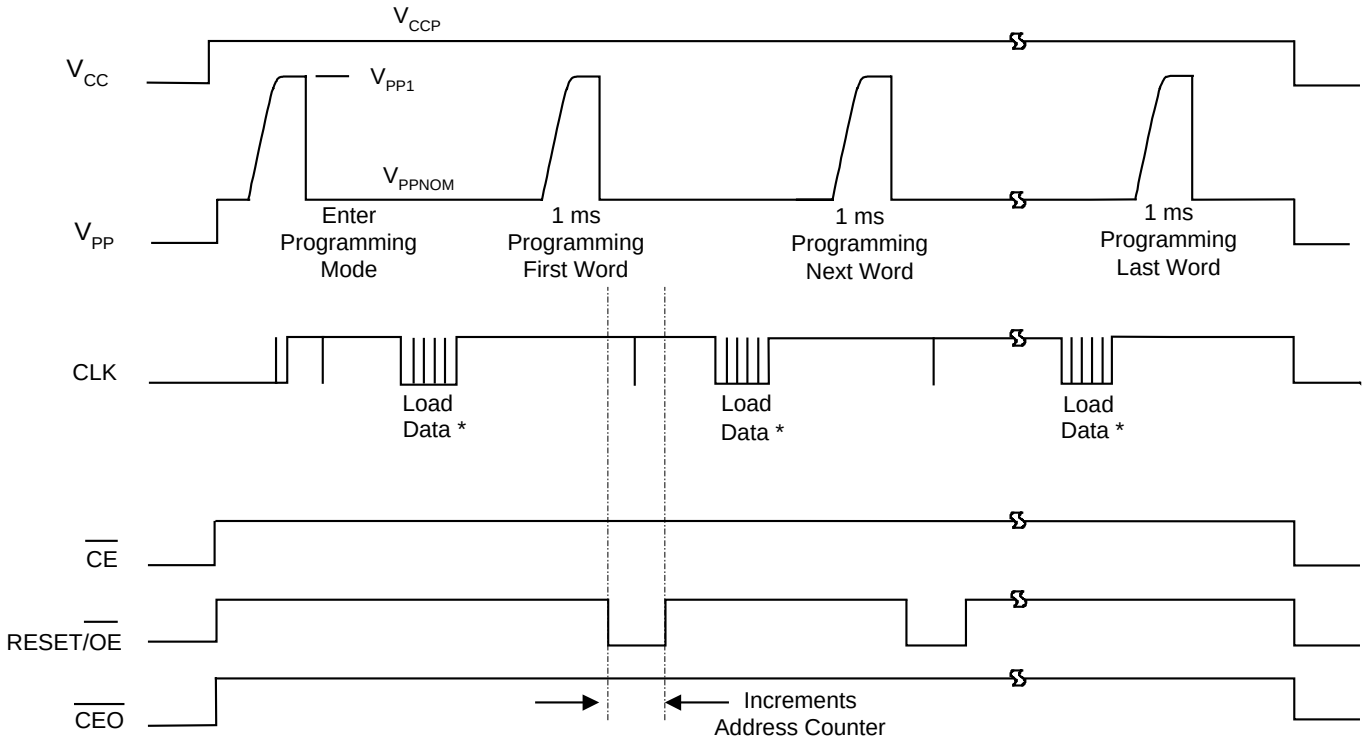
** Normal mode, V_{CCNOM}, V_{PPNOM}

Figure 1. Programming



*** Verify $\overline{CEO}$ has gone LOW one clock after last bit

Figure 1. Programming Sequence (Continued)



*Number Of Clocks For The Device Word

Figure 2. Programming Cycle Overview

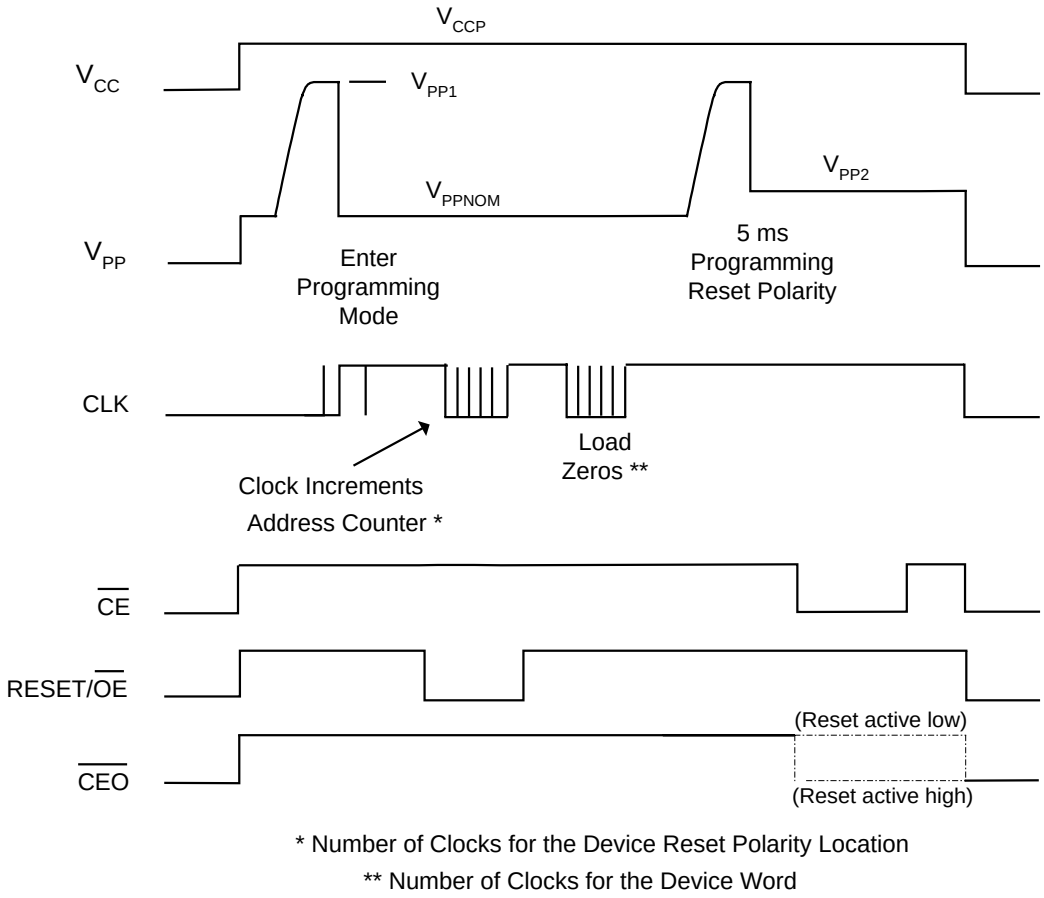


Figure 3. Programming Reset Polarity

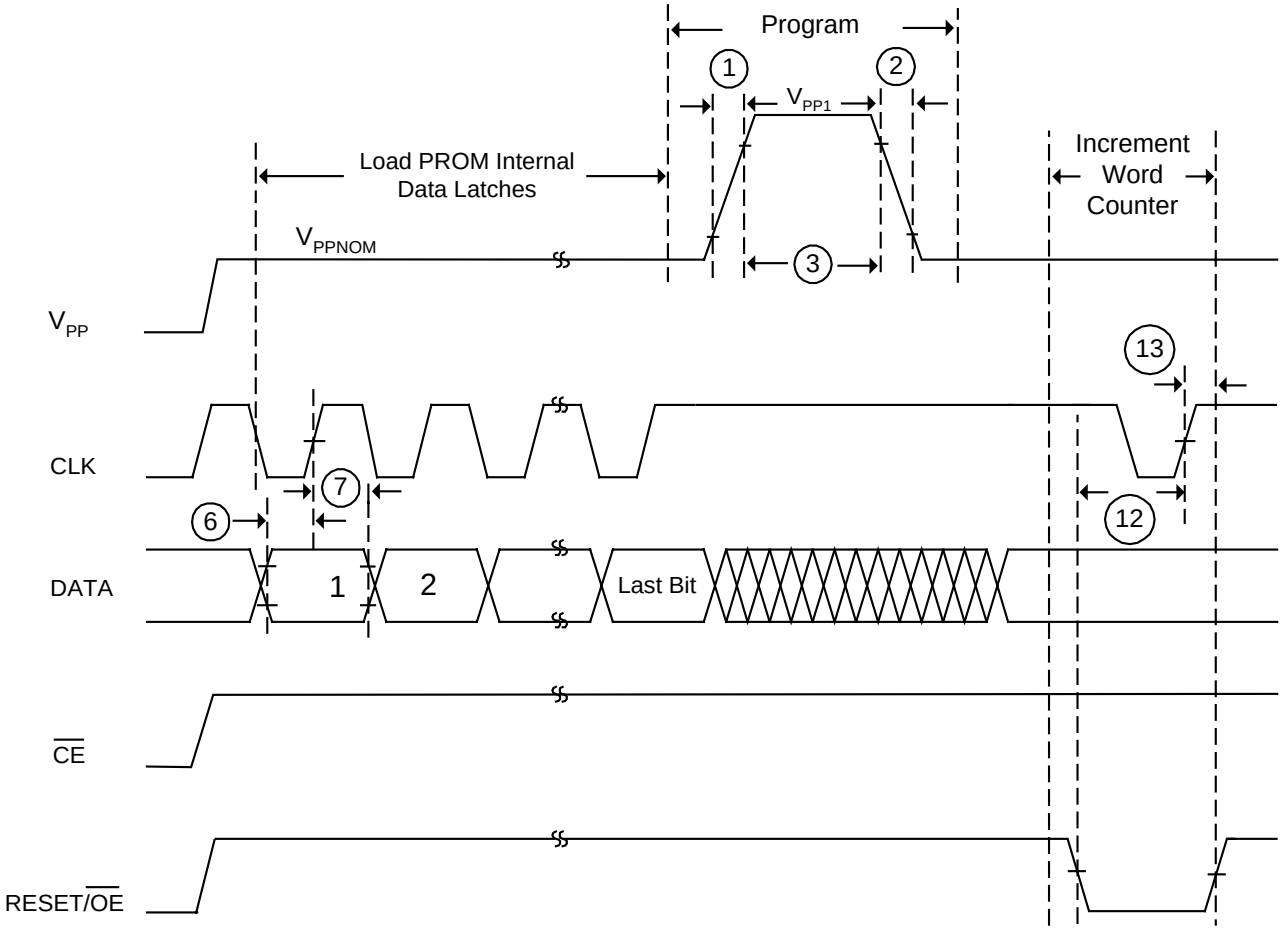


Figure 4. Details Of The Programming Cycle

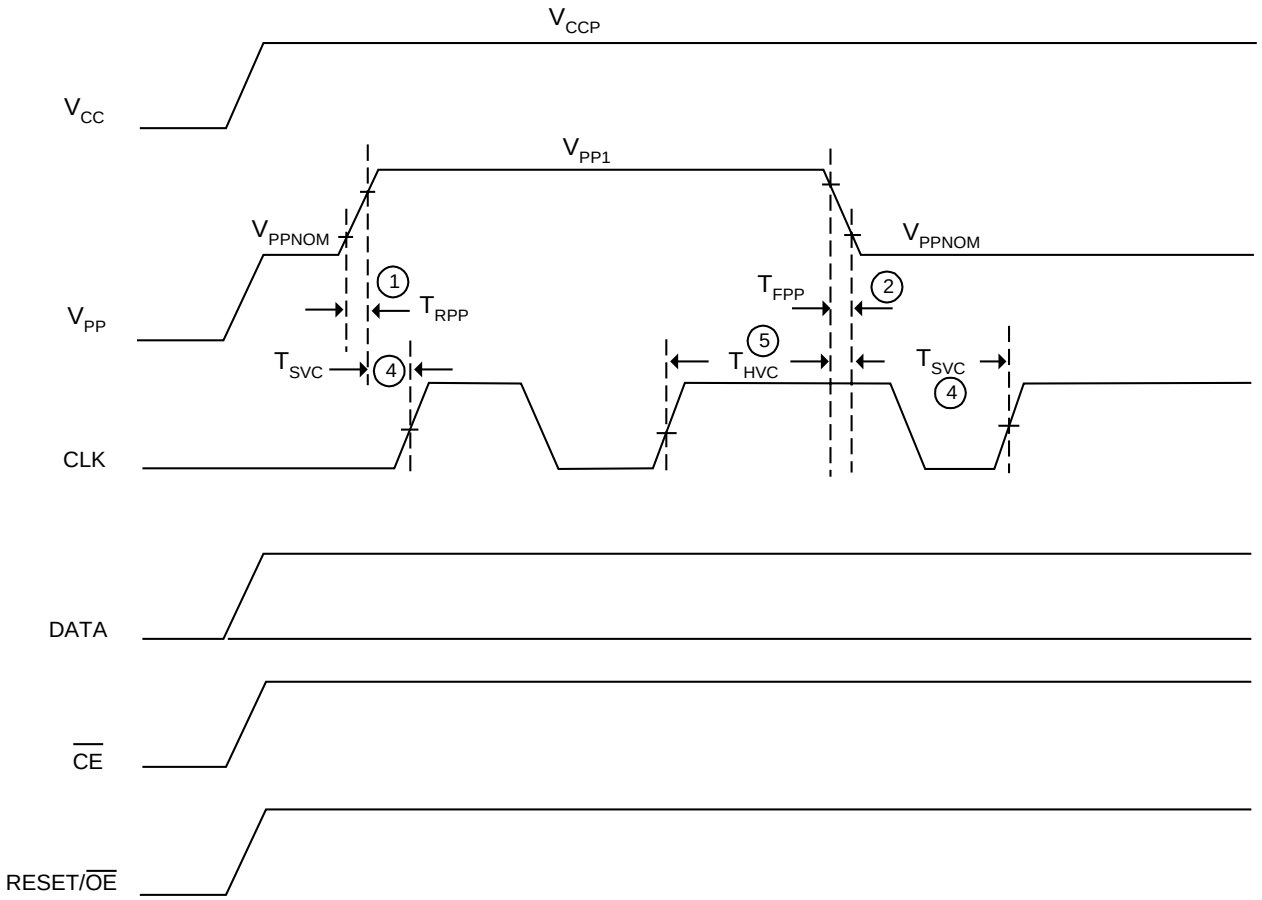


Figure 5. Enter Programming Mode

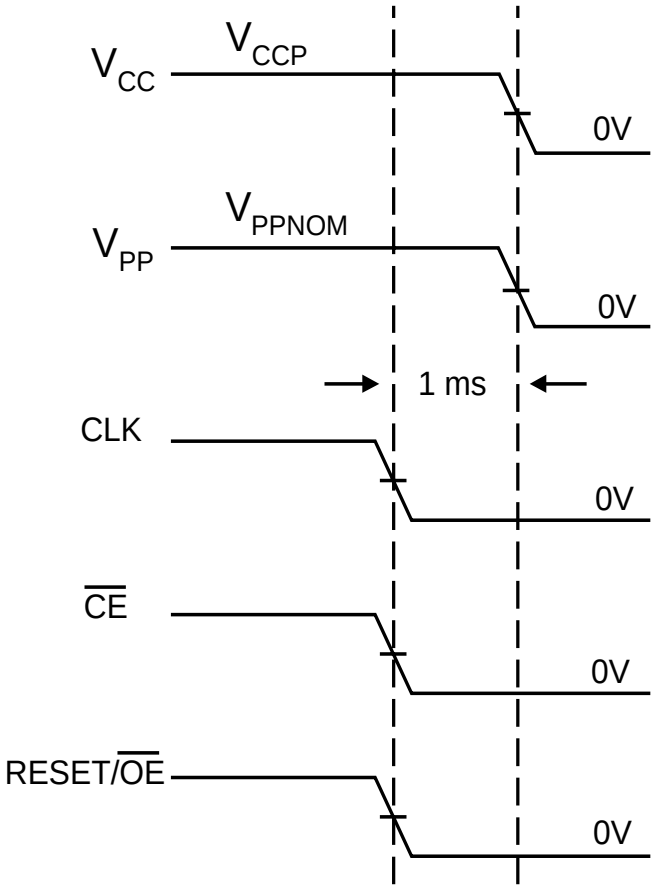


Figure 6. Exit Programming Mode

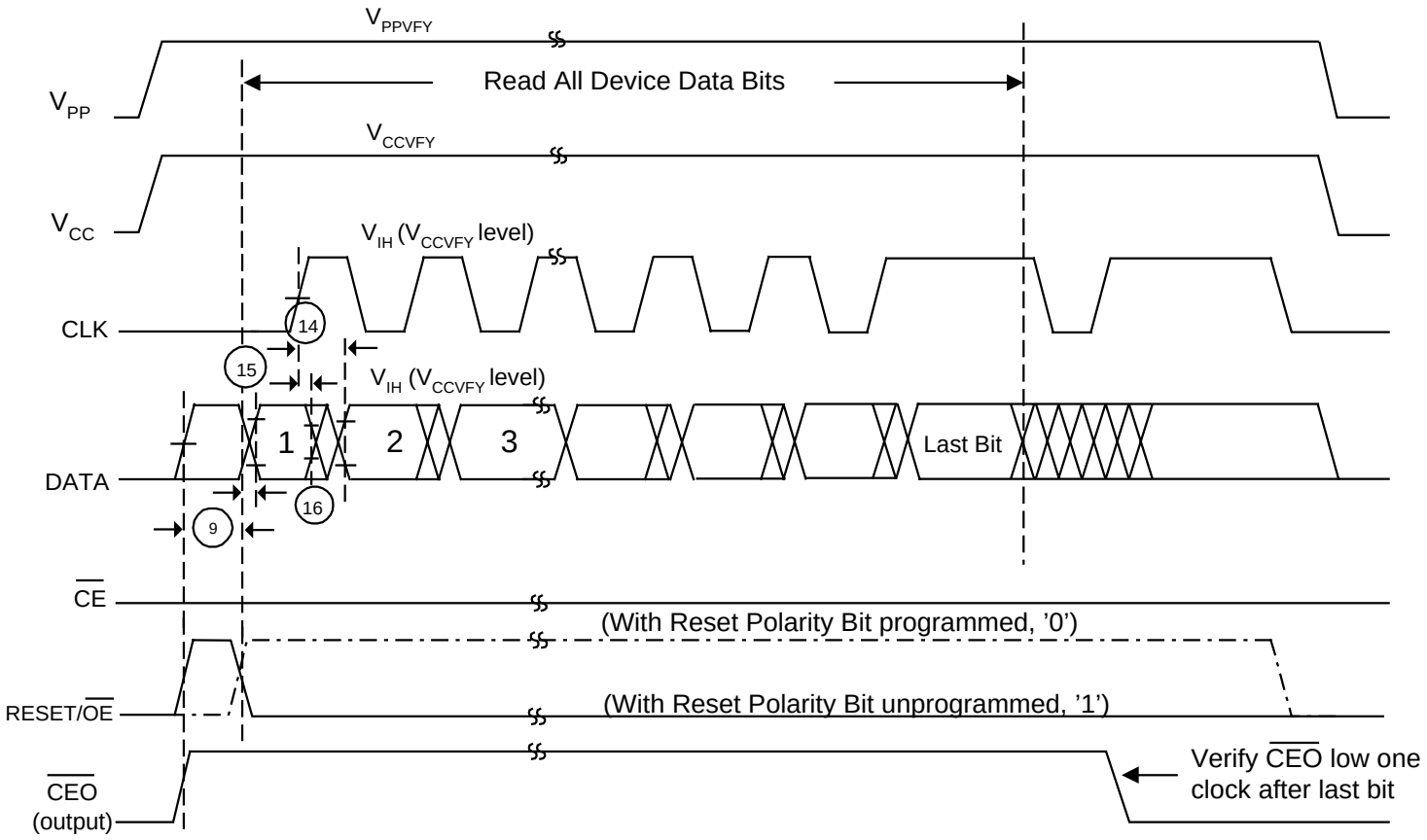


Figure 7. Details Of Verify Cycle

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