Set-up and Hold Times

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Introduction

Beware of hold-time problems, because they can lead to unreliable, temperature-sensitive designs that can fail even at low clock rates.

“Set-up time” and “hold time” describe the timing requirements on the data input of a flip-flop or register with respect to the clock input. The set-up and hold times describe a window of time during which data must be stable in order to guarantee predictable performance over the full range of operating conditions and manufacturing tolerances.

A positive set-up time describes the length of time that the data must be available and stable before the active clock edge. A positive hold time, on the other hand, describes the length of time that the data to be clocked into the flip-flop must remain available and stable after the active clock edge. A positive set-up time limits the maximum clock rate of a system, but a positive hold time can cause malfunction at any clock rate. Thus, chip designers and system designers strive to eliminate hold-time requirements.

The IC design usually guarantees that any individual flip-flop does not require a positive hold time with respect to the clock signal at this flip-flop.

Hold-time requirements between flip-flops or registers on the same chip can be avoided by careful design of the on-chip clock distribution network. If the worst-case clock-skew value is shorter than the sum of minimum clock-to-Q plus minimum interconnect delays, there is never any on-chip hold-time problem.

It is, however, far more difficult to avoid a hold time problem in the device input flip-flops, with respect to the device clock input pin. When specifying the data pin-to-clock pin set-up and hold times, the chip-internal clock distribution delay must be taken into consideration. It effectively moves the timing window to the right (see figure), thus subtracting from the specified internal set-up time (which is good), but adding to the hold time (which is very bad). If the clock distribution delay is any longer than the data input delay – and it easily might be – the device data input has a hold-time requirement with respect to the clock input.

This means that the data source, usually another IC driven by the same clock, must guarantee to maintain data beyond the clock edge. In other words, the data source is not allowed to be very fast. If it is, the receiver might erroneously input the new data instead of the data created by the previous clock, as it should. This is called a race condition, and can be a fatal system failure.

If the receiving device has a hold time requirement, the source of data must guarantee an equivalent minimum value for its clock-to-output delay. Almost no IC manufacturer is willing to do this, and in the few cases where it is done, the minimum value is usually a token 1 ns. Any input hold time requirement is, therefore, an invitation to system failure. Any clock distribution skew on the PC-board can compound this issue and wipe out even the specified short minimum delay.

Xilinx has addressed this problem by adding a deliberate delay to every FPGA data input. In XC3000, and XC3100 FPGAs, this delay is fixed and always present; in XC4000 and XC5200 FPGAs, this delay is optional, and its value is tailored to the clock distribution delay (i.e. it is larger for bigger devices). As a result we can claim that no Xilinx FPGA Data input has a hold-time problem (i.e., none has a positive hold time with respect to the externally applied clock), when the design uses the internal global clock distribution network (and, in XC4000 and XC5200, uses the delayed input option). Most competitive devices do not offer this feature.