

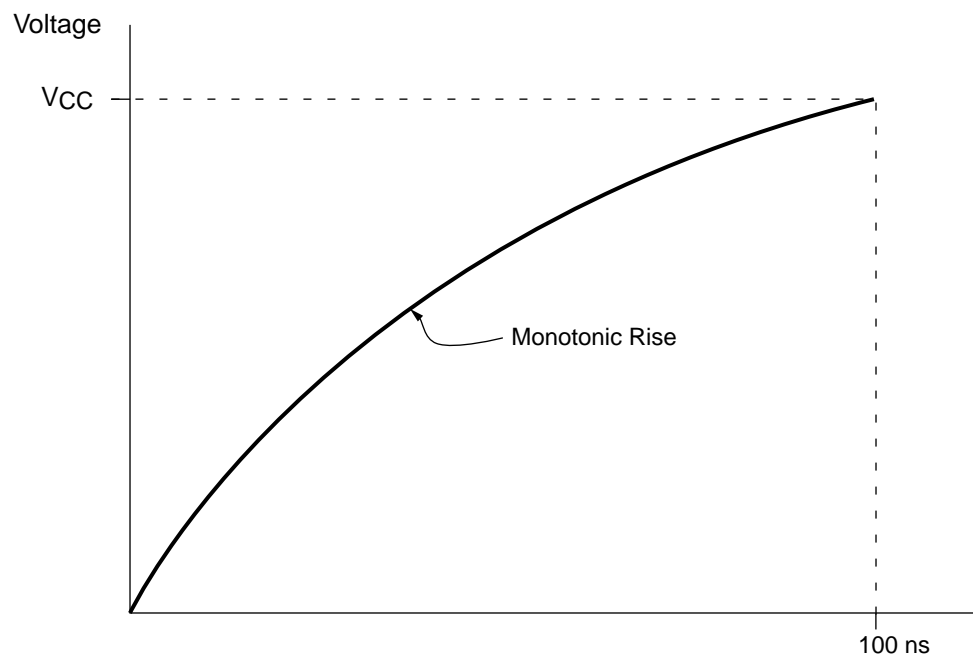


XAPP310 (v1.1) February 14, 2000

Power-up Reset Characteristics of CoolRunner CPLDs

Introduction

Depending upon where and how CoolRunner™ CPLDs are used, the power up characteristics may be of interest. **Figure 1** describes an "ideal" system power voltage ramp for Xilinx CoolRunner CPLDs. As one can see, the voltage must be monotonic during V_{CC} ramp. Also notice that the voltage must not reach valid V_{CC} in less than 100 nanoseconds. This will not present a problem because a system power bus would have to have an impedance of less than 0.5 Ohms and a total capacitance of less than 0.1 microfarads in order to produce a voltage ramp below this minimum. Even if one were to power a CoolRunner CPLD from the output of another device, (something that can be accomplished since they are such LOW power consumers) it would still be difficult to ramp up before the minimum ramp specification.



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Figure 1: "Ideal" Voltage Ramp

Figure 1 is the "Ideal" voltage ramp, and does not exist in nature. A more realistic example of a power voltage ramp appears in [Figure 2](#).

Many times a "glitch" will appear in the system power voltage ramp due to the instantaneous current demand produced by many active devices "turning on" at the same time. This flattening out of the voltage curve is acceptable as far as CoolRunner CPLDs are concerned, as long as it does not go in a negative direction.

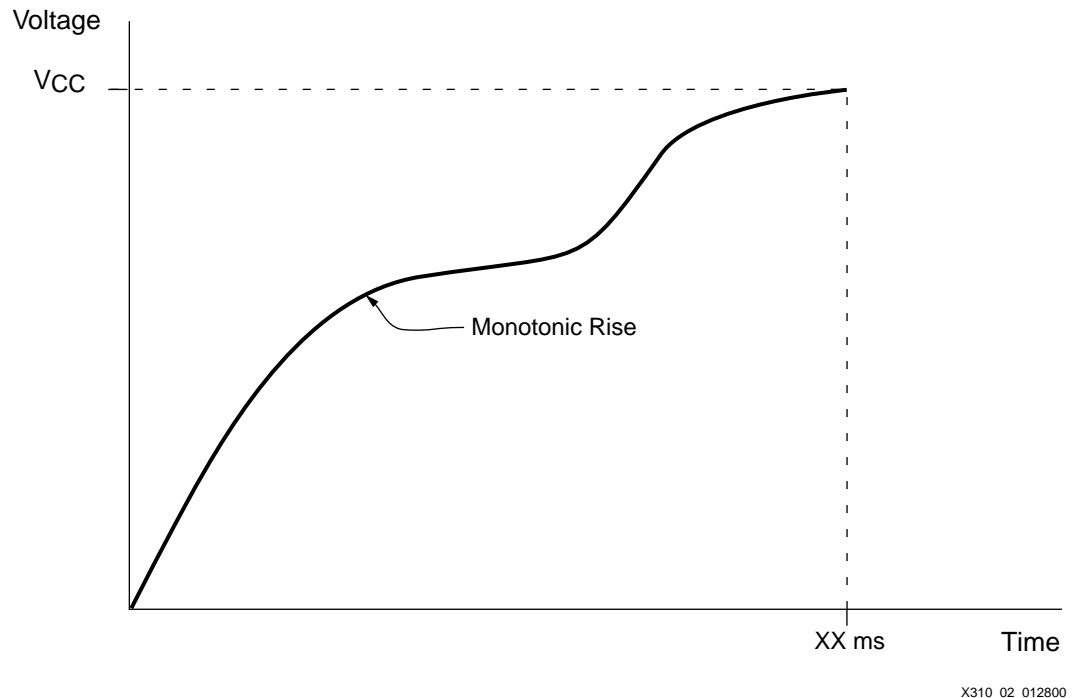


Figure 2: Realistic Voltage Ramp

During the time that the power voltage ramp is below a valid High level, the I/O pins on the CoolRunner devices will be in a high-impedance state. Once a valid High is reached the following will occur:

1. Output pins controlled by combinatorial logic will immediately go to the proper level determined by the result of the logic equations.
2. Registered output pins will go low until the first valid clock edge is generated. This clock edge will then clock the value of the register's input to its output.

Figure 3 graphically describes this situation.

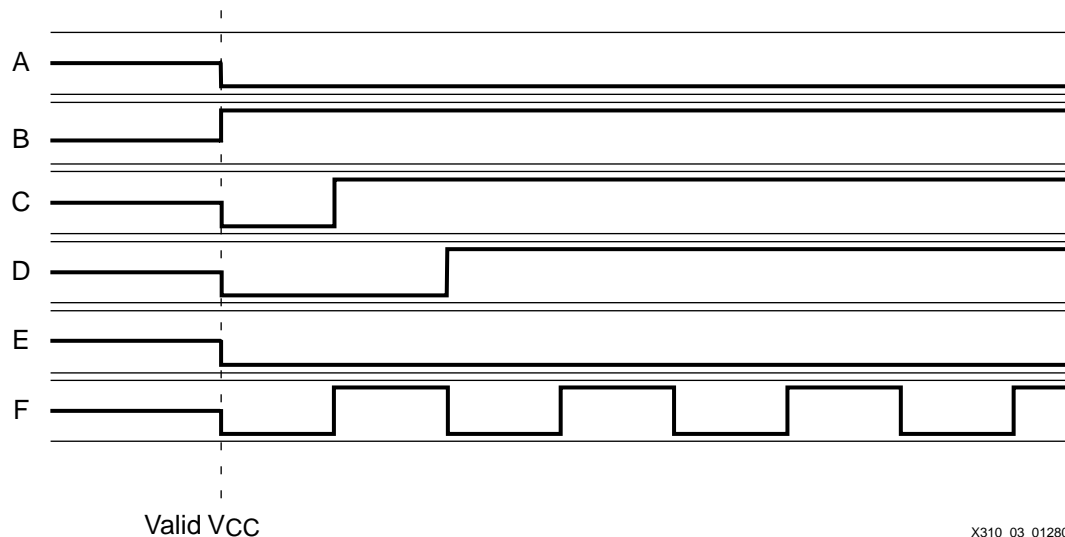


Figure 3: Power-up Graphic

The signals represented by the letters A through F are:

A combinatorial signal driving the output Low

B combinatorial signal driving the output High

C registered signal driving the output High on valid rising edge clock

D registered signal driving the output High on valid falling edge clock

E registered signal driving the output Low on valid rising/falling edge clock

F clock input

As can be seen in Figure 3, all I/Os are at high impedance until valid V_{CC} is reached. After the power voltage ramp reaches a valid level, a few milliamps of current will be drawn while the device configures. The time during which this current is drawn is approximately 50 microseconds. After configuration is complete the device will draw less than 100 microamps with no clock input. This is true of all the parts in the CoolRunner family.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/14/00	1.1	Converted to Xilinx format.