HDLC Controller Solutions Using Spartan-II FPGAs

HDLC Controller cores, ported to the Spartan-II family, highlight the concept of a programmable ASSP

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HDLC Controller cores (soft IP) have been available for Xilinx XC4000XL and Virtex FPGAs for some time. Now, this technology is also available for use with the new Spartan-II family, which is uniquely poised to penetrate the ASSP marketplace because of its advanced features, high performance, and low cost. A programmable HDLC Controller solution, with efficient partitioning of hardware and software functions, provides the necessary scalability and flexibility you need for any application, and allows you to easily adapt to new standards; you get all the benefits of an ASSP device, plus the many advantages offered by programmable logic.

HDLC stands for "High-Level Data Link Control," a bit-oriented synchronous data link layer protocol developed by the International Standards Organization (ISO). HDLC Controllers are devices which execute the HDLC protocol and their properties include:

- Transmitting and receiving the serial packet data.
- Providing data transparency through zero insertion and deletion.
- Generating and detecting flags that indicate HDLC status.
- Providing 16-/32-bit CRC on data packets using the CCITT defined polynomial.
- Recognizing the single byte address in the received frame.

HDLC Controller Applications

HDLC Controllers are used in various data networking operations. Some of the key applications are:

- Frame relay switches - high density access, FRADs.
- ISDN - basic-rate or primary-rate interfaces, D-channel.
- X.25 and V.35 protocols.
- Internet/edge routers, bridges, and switches for high bandwidth WAN links.
- Cellular base station switch controllers.
- Error-correction in modems.
- T1/E1, T3/E3 - channelized, clear channel (unchannelized).
- xDSL - each port can support up to 10Mbps.
- Dual HSSI.
- SONET termination.
- Digital sets, PBXs, and private packet networks.
- C-channel controller to Digital Network Interface Circuits.
- Data link controllers and protocol generators.

- Inter-processor communication.
- Logic consolidation.
- CSU/DSU.
- Protocol converters.
- Packet data switches.
- Distributed packet-based communications systems.
- Multiplexer/Concentrators - remote access, multi-service access.

Xilinx AllianceCORE Partners

Currently, there are two Xilinx AllianceCORE partners supplying HDLC cores for Spartan-II FPGAs: Memec Design Services, and CoreEL MicroSystems.

Memec Design Services (MDS)

The Single Channel XF-HDLC Controller core conforms to the ISO/IEC 3309 specification, and provides the entire functionality of the HDLC Controller. The core:

- Provides 16-/32-bit CCITT-CRC generation and checking.
- Performs flag and zero insertion and detection.
- Allows full duplex operation.
- Operates at a DC to 53 Mbps (STS-1) data rate.
- Provides full synchronous operation.
- Provides an interface that can be customized for user FIFO and DMA requirements.
- Allows 16-/32-bit FCS generation and verification.
- Provides an MTU and compression enable signal.
- Provides a scramble and de-scramble enable signal.
- Detects the Address field, Control field, escape sequence, and FCS packet errors.
- Provides statistics for Address field, Control field, Protocol field, FCS field, and escape sequence packet errors.
- Provides statistics such as the number of packets, runt packets, valid packets, and excess length packets.
- Detects error conditions like Transmission Break on transmit side.
- Discards packets received with Address, Control, or Protocol field errors.
- Optionally compresses Address, Control, and Protocol fields.
- Generates a discard packet signal for any

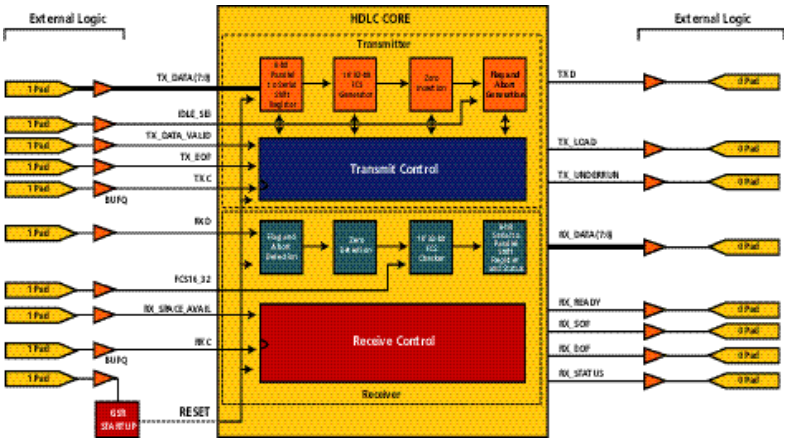

Figure 1 - HDLC Controller block diagram.
(courtesy: Memec Design Services)

CoreEL MicroSystems

The PPP8 HDLC core (CC318f) conforms to RFC1619 PPP over SONET specification. The core:

- Supports programmable Address, Control and Protocol fields.
- Supports an 8-bit Packet and PHY framer interface.

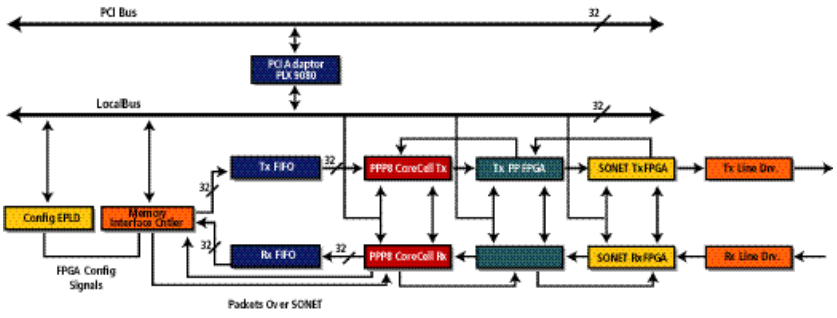

Figure 2 - Application of HDLC cores.
(courtesy: CoreEL MicroSystems)

packet with an FCS or invalid packet on packet interface error.

A typical HDLC Controller Block Diagram is shown in Figure 1. A typical application is shown in Figure 2.

Comparing the Spartan-II HDLC Solution with Stand-alone ASSPs

Using an HDLC IP core in conjunction with a Spartan-II FPGA, offers significant advantages over a fixed-logic (non-programmable) ASSP. By using the Spartan-II family, you can implement the feature sets required and these can be customized to meet the exact design requirements.

You can also integrate other parts of your design within the same FPGA, for increased performance and reduced cost. For example, an HDLC Controller supplied by a stand-alone ASSP vendor may include a 32-bit, 33-MHz PCI Controller. However, your design may require something different, such as a 32-bit, 66-MHz or a 64-bit, 33-MHz PCI Controller. By using the Spartan-II FPGA family in conjunction with the appropriate cores, you can create the optimal HDLC to PCI solution for your specific requirements. Because of the inherent low cost of the Spartan-II family, this flexibility comes at a significantly lower cost than the fixed ASSP solution. Figure 3 shows the value comparison.

Programmability is Key

Conflicting specifications and lack of a clear direction create the need for programmableASSP solutions. The Spartan-II family accommodates specification changes and can easily be used in volume production. For example, the currently available non-programmable HDLC Controller solutions are based on X.25 (CCITT) level-2 or OSI Layer-2, ISO3309 specifications only. However, the solutions provided through Spartan-II FPGAs allow you to use X.25 (CCITT) level-2, OSI Layer-2, ISO3309, RFC1619 PPP over SONET, and ITU recommendation (Q.921) specification standards. It would be nearly impossible, and cost-prohibitive, for an ASSP vendor to meet all of these specifications.

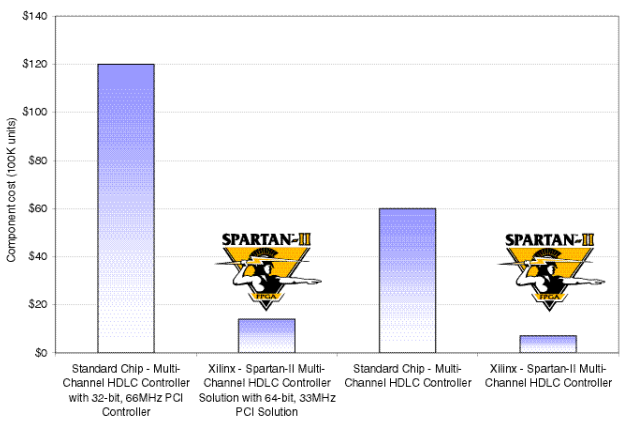

Figure 3 - Value comparison.

Xilinx Online for Field Updates

Through the Xilinx On-line program, the Spartan-II family allows you to remotely update your design, over any network. With new features, enhancements, and bug fixes, the life of the HDLC controller within any networking system increases. This also allows your equipment to adapt to changing standards. Designing systems that allow remote upgrades can provide new revenue opportunities as well, because you can continue to sell new features, after your equipment is installed. You cannot easily offer these unique features if your hardware design is not programmable.

Conclusion

The Spartan-II family is unaffected by the hurdles that an ASSP vendor must overcome; its inherent advantages extend the reach of the Spartan family to new levels and creates new opportunities for PLDs in the ASSP market.

The cost difference between a stand-alone ASSP and an equivalent programmable Spartan-II solution is considerable. Thus, the Spartan-II family is a clear winner in not only the HDLC Controller market, but also other ASSP niche areas.

For more information on the MDS core, see:
www.xilinx.com/products/logicore/alliance/memec/memec.htm.
For more information on the CoreEL MicroSystems core, see:
www.xilinx.com/products/logicore/alliance/coreel/coreel.htm.