Low Power Benefits of the Spartan-XL Family

A look at Spartan-XL power-down modes, small form factor packages, package power dissipation, and device reliability

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The Spartan™-XL family is built with an advanced 3.3V process, a segmented low power architecture, and a power-down feature that significantly reduces the FPGA's quiescent current requirements (from 3mA to 100µA typical). This opens up a whole new market for Spartan-XL FPGAs because these devices can now be used in power-sensitive applications such as laptop computers, cellular phones, PDAs, camcorders, and so on.

Power-down Modes

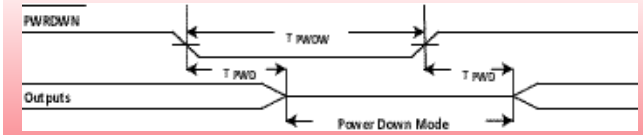
There are two kinds of power-down modes: manual and automatic. Both provide low quiescent (standby) current while retaining the bit map (configuration data with which the device had been configured).

Manual Mode

In the manual mode, the device is fully inactive, the register data is lost, and the activation and de-activation are controlled by the PWRDWN pin. The following events occur in sequence to conserve the power:

- All inputs (including M0, M1, DONE, CCLK, and TDO) except PWRDWN are disconnected from their sources. Internal to the device, the input signals are tied to GND.
- All pull-up and pull-down resistors on all I/Os (except PWRDWN) are disabled.
- The Global Set-Reset (GSR) is activated, clearing all the registers in the device. This reset state is held as long as the device is in power-down mode.
- The Global 3-state (GTS) is activated, putting the device outputs in high-impedance state.

The device stays in DC state, drawing minimal power, until PWRDWN goes High, at which point it returns to full operation over a period of 50 ns (max), as shown in Figure 1. The manual power-down mode is described in detail in application note XAPP124 on the Xilinx website at: http://www.xilinx.com/xapp/ xapp124.pdf.



Description	Symbol	Min	Max
Power-down Time	T_{PWD}	-	50ns
Power-down Pulse Width	T_{PWDW}	50ns	-

Figure 1: Power-down timing.

Automatic Power-down Mode

In the automatic mode the device is active, the register data can be retained if required, and the power-down is initiated without using the PWRDWN pin. You can selectively control the features of a design, which may consume a relatively large amount of power, to obtain quiescent (standby) current down to 100µA typical. Some of these controllable features are:

- Pull up and pull down resistors on the IO pins.
- 5V I/O tolerance.
- Clocks that need to run intermittently.
- The redundant use of high-frequency clocks.

The critical register data can be left operating, while disabling the remaining parts of the design, to obtain the low quiescent power. Unlike the manual power-down mode, this mode does not have any power-down recovery time when switching back to normal operation. The automatic power-down mode is described in detail in the application note XAPP125 on the Xilinx website at: http://www.xilinx.com/xapp/xapp125.pdf.

Superior Benefits

The low power requirements of the Spartan-XL family makes it possible to use small form factor packages to save board space and reduce design costs, making it an ideal choice for most portable and low power equipment.

Package Power Dissipation Limit

Power consumption plays an important role in selecting the device package. For the device to operate reliably, the power consumed by the device must be less than the maximum power its package can dissipate. Use the following equation to determine the maximum power dissipation P_d for a particular package:

$$P_d = (T_J - T_A)/\theta_{JA}$$

where T_J is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is thermal resistance of the package.

Lower power means lower heat dissipation requirements, thus making it possible to use smaller footprint packages. This in turn would provide cost savings because the package does not need to have an extra heat sink, and it occupies less board space. As an illustration of this power-performance limit, the graph shown in Figure 2 plots dynamic power with respect to performance for two devices of comparable logic density: the Xilinx XCS30XL in 144-pin Chip Scale package and the Altera 10K30A in 144-pin TQFP package.

Figure 2 shows that the Chip Scale package in the Spartan-XL family can be used up to 100 MHz without any problem with power dissipation. However, the TQ package used for the Altera 10K30A device cannot be used above 77 MHz. The device is just not reliable beyond this performance. To use it reliably beyond 77 MHz performance, you would need to either add a heat sink or force air into the package using a

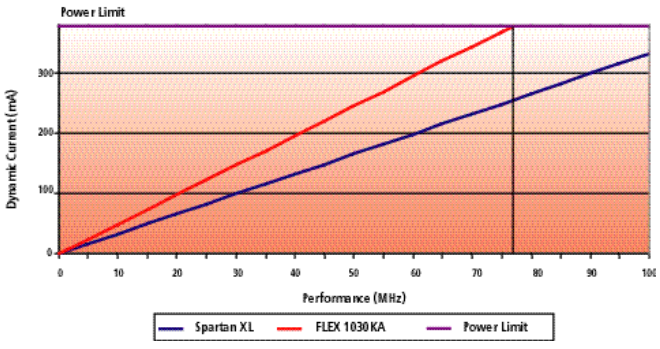


Figure 2: Dynamic power comparison of Spartan-XL device with 10K30A.

fan, which means extra hardware, additional cost, and more board space.

Small Form Factor Advantage

The Chip Scale package (CSP) dramatically reduces board space and increases I/O count; it is smaller than any competitive offering in the industry. The package is available in 144 and 280 ball counts with 0.8 mm pitch, and is ideal for low-power, light-weight, and small form factor designs. Xilinx is the first programmable logic supplier to offer the CSP package for an FPGA that meets the JEDEC Level 3 moisture sensitivity level requirements. This level of reliability enables you to reduce standard manufacturing cycle times and further minimize overall system cost.

As seen in Figure 3, the CS144 package offers 70% board area savings when compared with the TQ144 package. Similarly, the CS280 package offers 83% board area savings when compared with the popular PQ240 package.

Higher Reliability

Xilinx is known for quality and reliability. Reliability is measured in terms of Failure-In-Time rates (FIT); failures in 10^9 device hours. Lower power provides lower FIT rates and higher device reliability, thus reducing product test rework and field failures. Overall device reliability decreases exponentially as junction temperature increases. The industry standard limit for the maximum junction temperature is 125°C for the plastic package and 150°C for the ceramic package. Table 1 compares FIT rates of Xilinx to that of the nearest competitor.

T_J (°C)	50	60	70	80	90	100
Altera	7	20	50	118	267	578
Xilinx	1.5	4	10	23	53	115

Table 1 - FIT rate comparison.

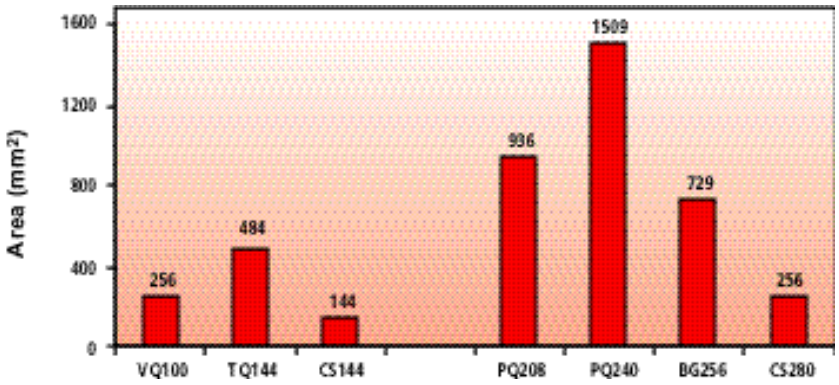


Figure 3: Package area comparison.

Conclusion

The low power requirements of the Spartan-XL family makes it possible to use small form factor packages to save board space and reduce design costs, making it an ideal choice for most portable and low power equipment.