THE NEW Spartan-II FPGA Family

KISS YOUR ASIC GOOD-BYE

Spartan FPGAs are experiencing tremendous growth due to their inherent advantages over ASICs.

Device	XC2S15	XC2S30	XC2S50	XC2S100	XC2S150
System Gates	15K	30K	50K	100K	150K
Logic Cells	432	972	1728	2700	3888
Block RAM Bits	16,384	24,576	32,768	40,960	49,152
Block RAM Blocks	4	6	8	10	12
DLLs	4	4	4	4	4
I/O Standards Supported	17	17	17	17	17
Max I/O	86	132	176	196	260
Packages	VQ100	VQ100			
	TQ144	TQ144	TQ144	TQ144	
	CS144	CS144			
		PQ208	PQ208	PQ208	PQ208
			FG256	FG256	FG256
				FG456	FG456

Table 1 - Integrated features.

The Spartan Series FPGAs, introduced by Xilinx in January 1998, offer a very attractive alternative to ASICs for your high volume, low cost applications. The Spartan families are designed to penetrate markets that were once dominated by ASICs. These include digital modems, printers, faxes, portable audio players (such as MP3), set-top boxes, and POS terminals. The Spartan Series is the first FPGA family to provide a complete and compelling mix of advanced features, low prices, high performance, and powerful development tools; the key ingredients required by ASIC designers. Now, the new Spartan-II FPGA family sets a new standard for low cost, and high performance.

The Spartan-II Family

Fabricated on a leading 0.18 µm, six-layer metal process, the Spartan-II family uses the most advanced process technologies available today. The family's core voltage operation is 2.5V, yet it incorporates unique I/O technology that allows both 3.3V and 5V I/O operation.

The Spartan-II family includes new system-level features such as delay locked loops (DLLs), block RAM, distributed RAM, multiple I/O standards, ultra-high performance, and arithmetic logic. All of the features found in ASICs and ASSP devices are now available in the Spartan-II family at very attractive prices. Spartan-II FPGAs also provide an impressive array of highly complex cores (intellectual property) enabling you to further leverage the time-to-market benefits offered by programmable logic.

Memory

On-chip memory is vital to most designs, from buffering data between two dissimilar buses to

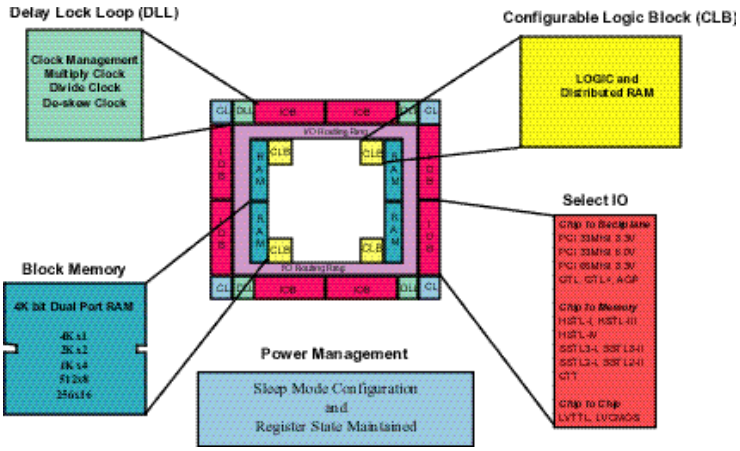


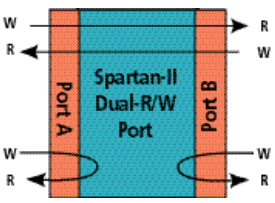
Figure 1 - Spartan-II family architecture.

providing storage locations of constants for high performance DSP functions. The Spartan-II family provides you with maximum memory flexibility.

Xilinx pioneered the capability of distributed memory (also found on Spartan and Spartan-XL families), which efficiently implements wide/shallow FIFOs or scratch pad memories. The family also incorporates block RAM (in blocks of 4Kbits) which efficiently implement memory for deep FIFOs, single port RAM, and True Dual Port RAMs as shown in Figure 2. Unlike competing two-port architectures, Xilinx provides true dual port RAM operation, for high-speed read and write operation.

Delay Locked Loops

DLLs perform the same tasks as traditional phase lock loops (PLLs) but are more robust and



Data Flow	Spartan II	Two-Port
A to B	Yes	Yes
B to A	Yes	No
A to A	Yes	No
B to B	Yes	No

Figure 2 - Spartan-II family dual port memory.

are less susceptible to noise interference, a common problem with PLLs. The Spartan-II DLLs allow you to multiply or divide the incoming clock on chip, as well as drive multiple clocks on the board. The DLL feature also allows you to de-skew the clock on chip, ensuring all nodes on the device are synchronized while providing minimum set-up and hold times.

With four DLLs per device, the Spartan-II family provides a sufficient number of DLLs with which you can perform multiple functions. For example, one DLL may be used to de-skew the clock on chip, one for multiplying the clock for accelerated performance on chip, two DLLs to drive clocks to various devices on the board—all at the same time. A single crystal oscillator and a Spartan-II device may provide all the clock management you need for your board design.

SelectI/O™

The Spartan-II family supports most of the popular and demanding I/O standards, including those that are optimized for high-speed memory interfaces. The new input/output standards that are supported, include SSTL, HSTL, AGP, GTL, GTL+, and PCI. The integration of these standards into the Spartan-II family now allow the elimination of costly bus transceivers that take up valuable board space.

The I/Os for the Spartan-II family are 5V and 3.3V tolerant for interfacing with older generation technology on the board. This is a significant advantage for the family because competing architectures are unable to support 5V operation.

Support for high-speed interfaces significantly increases performance over the Spartan (80 MHz) and Spartan-XL (100 MHz) families, to a blazing 200 MHz.

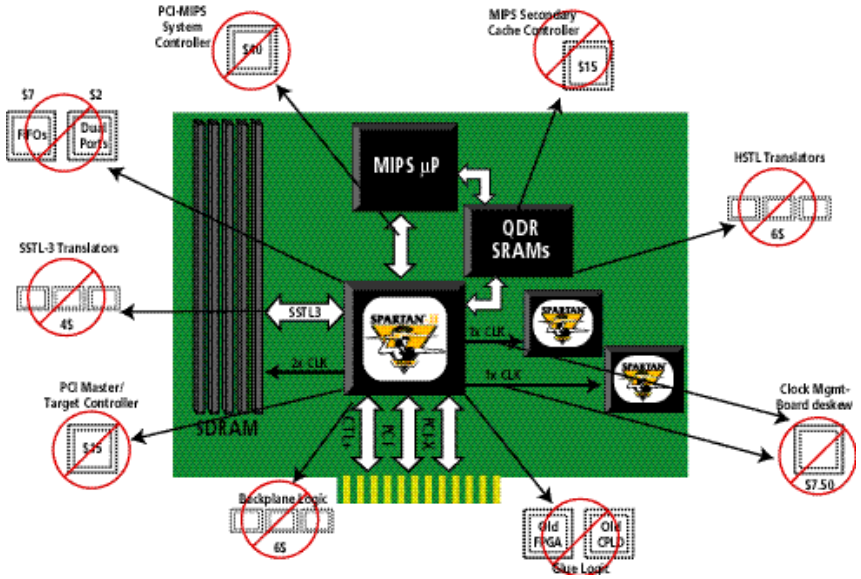


Figure 3 - Spartan-II value.

An Example of Spartan-II Value

The board diagram in Figure 3 illustrates how you can integrate many different functions into a Spartan-II FPGA to achieve significant cost savings. This example design includes a PCI master/target controller, some HSTL translators, a cache controller, SSTL-3 translators for SDRAM, a backplane interface, some glue logic, and the clock management device. All of these functions can be integrated into the XC2S100 Spartan-II device which costs just $10.00, almost two-thirds less than the discrete solution, with room to spare for more logic. The Spartan-II solution also uses less board real estate, requires less power, and provides higher reliability.

Pricing

The Spartan-II family has been created from the ground-up, in keeping with the Spartan Series philosophy, to provide industry-leading features, density, and performance at price points that match or beat ASICs and ASSP devices. The family has been able to achieve a milestone, long sought after and promised by the programmable logic industry but now only realized by the Spartan-II family: 100,000 gates for $10.00USD.

Below is a complete listing of high volume prices for the Spartan-II family at introduction.

Xilinx	Spartan II
Product	High Volume Price*
XC2S15	$ 3.95
XC2S30	$ 4.95
XC2S50	$ 7.95
XC2S100	$ 9.95
XC2S150	$ 12.95

* 250K units, a resale price, slowest speed/cheapest package

Table 2 - Spartan-II family pricing.

Conclusion

The Spartan-II family offers you the most cost-effective and flexible solution, enabling the fastest time-to-market with the lowest possible risk.

For more information regarding how the Spartan-II family addresses traditional ASIC and ASSP designs, please see www.xilinx.com