

Success Story

Spring Tide Uses Xilinx FPGAs for a New

Internet Protocol SERVICE

SWITCH

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The phenomenal success of the Internet and the universal adoption of the Internet Protocol (IP) are driving profound changes in the telecommunications industry. Spring Tide Network's IP Service Switch 5000 creates a new service layer for the public Internet Protocol network, and they chose eleven Xilinx FPGAs, including SpartanXL and Virtex devices, based upon the strong set of development tools and design flexibility.

"We began working with Xilinx as soon as we assembled our team. As a start-up, time to market was our overriding concern. Working with Xilinx was a very simple decision for us because Xilinx offered tremendous gate density and speed," said Steve Akers, co-founder and chief technology officer. "As a result, we were able to leverage their product to achieve our design objectives while avoiding the risk associated with an ambitious ASIC project."

"For our company, it was critical that we get to market in a timely fashion. Embarking on an ambitious ASIC program would have introduced too much risk to our plan," said Bob Sullebarger, vice president of marketing for Spring Tide. "We've seen several companies make the big bet

on ASIC science projects only to come up empty and disappoint their investors."

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About Spring Tide

Spring Tide switches are designed to create dedicated, secure tunnels between users, on demand, automatically setting up and tearing down point-to-point connections as needed. They are the only carrier-class, "any-to-any" data services tunnel switches capable of full service delivery at line speed. In addition, Spring Tide's hardware and software-

About Spring Tide

Spring Tide was founded by Stephen Collins, former vice president of marketing at StarBurst Communications, and Steve Akers, former CTO and vice president of advanced technology development at Shiva Corporation. Led by President and CEO Allan Wallack, the company has assembled a highly experienced product development team with engineering talent drawn from many of the leading networking and computer companies in the Boston area. For more information, visit the Spring Tide website at www.springtidenet.com.

based intelligence gives each flow the service it requires, such as filtering, tagging, classification, queuing, and address translation.

The Spring Tide switch's architecture features dedicated processors for handling the functions of flow classification and queuing; packet forwarding, routing and session management, encryption and compression, and key generation. A fully configured IP Service Switch 5000 contains more than one hundred special and general-purpose processors, as well as hundreds of megabytes of memory for context and state information.

The 5000 processes as many as 100,000 simultaneous secure customer sessions in a service provider's point of presence, without sacrificing Quality of Service or performance goals. Competing switches can process and track only a small fraction of that number. The 5000 switches all flows at line speed, regardless of any value-added processing (such as encryption), with less than 50 microseconds latency.

The IP Service Switch 5000 contains eleven Xilinx devices; 500k Virtex devices are installed in two locations: as a front-end packet scheduler to feed streams to the dual PowerPC processors on the tunnel card, and as a scheduler for the security subsystem. "We went with Xilinx for several reasons. First, Xilinx offered the strongest set of development tools available. Second, Xilinx had the highest device speed, which helps us from a performance perspective. In addition, Xilinx products offered us a great

deal of design flexibility as we architected our product," said Akers.

Xilinx Technology

The Virtex technology is the combination of leading-edge process technology, a system-level feature set, and breakthrough software technology. To build a multi-million-gate

FPGA, specific design optimization of the technology was necessary. The Virtex architecture represents aggressive use of an advanced 0.22-micron process to pack millions of gates with full utilization of five metal layers for an abundance of high performance routing tracks. The architecture is also easily scalable from 50,000 to one million system gates to offer the robust feature set across a wide range of densities in nine devices.

"The Xilinx parts allowed us to optimize the performance of our system by allowing us to run at 66 MHz," said Akers. "The overall design is very flexible and only Xilinx could give us a device capability supporting between 500,000 and 3.2 million gates."

"The Virtex devices are already proving to our customers the time-saving advantages that these FPGAs bring to their design cycle. The density and performance levels, combined with the popular system-level features and industry-leading FPGA price points make Virtex-E FPGAs an even more compelling alternative to ASICs," said Wim Roelandts, Xilinx president and CEO. ❧