Software Solutions

Version 3 Development Systems Quick Reference Guide

Xilinx development systems give you the speed you need. With the initial release of our version 3 solutions, Xilinx place and route times are as fast as two minutes for our 200,000 gate, XC2S200 Spartan™-II device, and 30 minutes for our one million gate, system-level XCV1000E Virtex™-E device. That makes Xilinx developmen systems the fastest in the industry.

And with the push of a button, our timing-driven tools are creating designs that support I/O speeds in excess of 800 Mbps, and internal clock frequencies in excess of 300 MHz. With each quarterly release, we are further accelerating your design process.

Xilinx desktop design solutions combine powerful technology with an easy to use interface to help you achieve the best possible designs within your project schedule, regardless of your experience level. For more information on any Xilinx products, visit www.xilinx.com

Alliance Series Solutions:
The Alliance Series Solutions contain powerful open systems implementation tools that are engineered to plug and play your existing design flow. This combination of advanced features delivers high performance results on the toughest designs.

Foundation Series ISE Solutions:
Foundation Integrated Synthesis Environment (ISE) is Xilinx next generation design environment, optimized to deliver the benefits of an HDL methodology. Foundation ISE is packed with technologies that help you bring your product to market faster.

Foundation Series Solutions:
The Foundation Series solutions are complete, ready-to-use design environments for programmable logic design based on industry-standard schematic, HDL, and pushbutton design flows.

Xilinx Web-based Design Solutions provide designers the ability to engage in digital design activities, on-line, using Xilinx application servers, or download design and implementation software modules for use in their own design environment. These applications include:

WebFITTER:
The WebFITTER is a free Web-based design tool that allows system designers to evaluate their designs using Xilinx XC9500 Series CPLDs.

WebPACK:
The WebPACK is a collection of four free downloadable software modules including ABEL v7.1, VHDL and Verilog synthesis, design implementation tools, and device programming software.

WebPACK now includes support of the entire Spartan-II FPGA family as well as the 300,000 system gate Virtex XCV300EFPGA.

Base and Base Express Configurations
The Base and Base Express configurations provide push button design flows and support a broad array of FPGA and CPLD devices targeted for low density and high volume applications.

Standard and Express Configurations
The Standard and Express configurations combine push button flows with powerful auto-interactive tools. These tools give designers more influence and control over implementation while maintaining the benefits of design automation.

Elite Configurations
The Elite configurations are designed to support powerful design flows that deliver high-performance designs for even the highest density, multi-million gate FPGA devices from Xilinx.

WebFITTER URL:
Go to the Xilinx website http://www.xilinx.com and jump to "WebFITTER"

WebPACK URL:
Go to the Xilinx website http://www.xilinx.com and jump to "WebPACK"

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Feature Comparison Guide

Design Entry	Alliance	Foundation	Foundation ISE	WebPACK
Schematic		●	●	●
VHDL, Veriolog HDL, ABEL, HDL		●	●	●
State Diagram Editor		●	●(1)	●(1)
Floorplanner	●	●	●	●
CORE Generator	●	●	●	●
Timing Constraint	●	●	●	●
Modular Design	(Optional)		(Optional)	
Design Synthesis	**Alliance**	**Foundation**	**Foundation ISE**	**WebPACK**
Xilinx Synthesis Technology (XST)			●	●
FPGA Express / Incremental Synthesis		●(5)	●	
Design Verification	**Alliance**	**Foundation**	**Foundation ISE**	**WebPACK**
Timing Simulation	●	●	●	●
Gate Level Simulator		●	●(2)	●
HDL Simulator	●(1)	●(1)	●(1)	●(1)
HDL Testbench Generator			●(1)	●(1)
Integrated Logic Analysis (ChipScope ILA)	(Optional)	(Optional)	(Optional)	
Static Timing Analysis	●	●	●	●
Design Implementation	**Alliance**	**Foundation**	**Foundation ISE**	**WebPACK**
Constraints Editor	●	●	●	●
CPLD ChipViewer	●	●	●	●
FPGA Editor	●	●	●	●
Error Navigation to Xilinx Web			●	●
Command Line Operation	●		●	●
HTML Timing Reports	●	●	●	●
Data Book I/O Timing	●	●	●	●
Timing-Driven Place and Route	●	●	●	●
Multi-pass Place and Route	●	●	●	
Project Archiving	●	●	●	●
System Interfaces	**Alliance**	**Foundation**	**Foundation ISE**	**WebPACK**
EDIF In	●	●		CPLD Only
PROM File Generator	●	●	●	●
JTAG Download Software	●	●	●	●
IBIS	●	●	●	●
STAMP	●	●	●	●
VHDL, Verilog Out	●	●	●	●
HDL Simulation Libraries	●	●	●	●
Environment	**Alliance**	**Foundation**	**Foundation ISE**	**WebPACK**
Operating System	PC / UNIX	PC	PC	PC

Device Comparison Guide

Elite	Standard/Express	Base/Base Express	WebPACK ISE
All Virtex-II Family	Virtex-II Family up to XC2V1000	Virtex-II Family up to XC2V80	Virtex XCV300E only
All Virtex-E Family	Virtex-E Family up to XCV1000E	Virtex-E XCV50E only	All Spartan-II Family
All Virtex Family	All Virtex Family	Virtex XCV50 only	All CoolRunner Series(4)
All Spartan Series	All Spartan Series	All Spartan Series	All XC9500 Series
All XC9500 Series	All XC9500 Series	All XC9500 Series	
All XC4000E/L/EX	All XC4000E/L	All XC4000E/L	
All XC4000XL/XLA	All XC4000XL/XLA/EX/XV(3)	XC4000XL/XLA up to XC4020	
All XC3000(3)	All XC3000(3)	All XC30003	
All XC5200(3)	All XC5200(3)	All XC52003	

1. Evaluation functionality available through the Xilinx ALLSTAR program. For more information on the ALLSTAR program, go to www.xilinx.com.
2. Functional and timing simulation is performed using a HDL simulator in the ISE product.
3. XC3000, XC5200, and XC4000XV devices are not supported in the Foundation Series ISE configurations.
4. CoolRunner series is only available in WebFITTER and WebPACK at this time.
5. Foundation Base does not include a license for FPGA Express.