

Points missed: _____ Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 2 for Spring Semester, 2005

Section 001

Read this before starting!

- The total possible score for this test is 100 points.
- This test is closed book and closed notes.
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- **Calculators are not allowed.** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

“Fine print”

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

Short answers – 2 points each

- True or False: The expression $A \cdot \bar{B} \cdot C + \bar{B} \cdot \bar{C} + \bar{A}$ is in proper Sum-of-Products format.
- True or False: Every truth table can be realized with both a Sum-of-Products expression and a Product-of-Sums expression.
- True or False? There exists exactly one pattern of rectangles for every pattern of 1's and 0's in a Karnaugh map.
All it takes is finding one case where this isn't true. The following is one of those cases. (Note the red rectangle.)

	<i>CD</i>			
<i>AB</i>	00	01	11	10
00	0	1	1	0
01	0	0	1	0
11	0	0	1	1
10	0	0	0	0

	<i>CD</i>			
<i>AB</i>	00	01	11	10
00	0	1	1	0
01	0	0	1	0
11	0	0	1	1
10	0	0	0	0

- How many cells does a 4 input Karnaugh map have?
a.) 4 b.) 6 c.) 8 d.) 16 e.) 24 f.) 32

With four inputs, there are $2^4 = 16$ possible combinations of ones and zeros. This means that the truth table has 16 rows and consequently the Karnaugh map has 16 cells.

- What is the largest number of input variables a Karnaugh map can have and remain 2-dimensional?
a.) 3 b.) 4 c.) 5 d.) 6 e.) 7 f.) 8

The most input variables for which a sequence can be made where only one bit changes from row to row or column to column is two. With two inputs for the rows and two inputs for the columns, we get four inputs. Adding another input will put us into the third dimension.

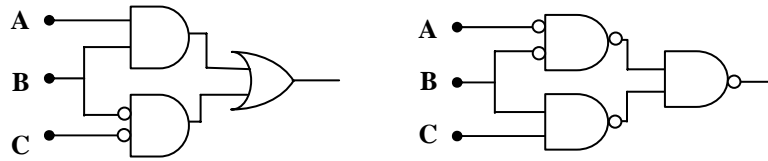
- In a 4-variable Karnaugh map, how many input variables (A, B, C, or D) does a product have if its rectangle of 1's contains 4 cells?
a.) 1 b.) 2 c.) 3 d.) 4 e.) Cannot be determined

One cell uses all input variables. Doubling that to two cells requires one fewer input variables, i.e., three variables. Doubling two cells to four cells requires one fewer input variables again, i.e., two variables.

- An active-low transparent latch copies data from the D input to the Q output when the clock is:
 a.) a logic 0 c.) changing from a 1 to a 0 b.) a logic 1 d.) changing from a 0 to a 1
- The invalid state of the active-low S-R latch occurs when the inputs are:
 a.) $\bar{S} = 0, \bar{R} = 0$ b.) $\bar{S} = 0, \bar{R} = 1$ c.) $\bar{S} = 1, \bar{R} = 0$ d.) $\bar{S} = 1, \bar{R} = 1$

Remember that the active low signals \bar{S} and \bar{R} represent set and reset respectively. Since they are active low, i.e., they cause stuff to happen when they go to zero, and they cannot both be active at the same time, then they both cannot be zero at the same time.

9. True or **False** The two circuits below are equal.



DeMorgan's theorem shows us that an OR gate can be replaced with a NAND gate with inverted inputs. The circuit above replaces the OR gate with a NAND gate with inverted inputs, but it also inverts all of the inputs to the AND gates. This is where the situation becomes false.

10. **True** or False: The result of the application of a Karnaugh map is a *minimum* SOP expression.

11. **True** or False: In a 3-input Karnaugh map, the maximum number of rectangles to cover all of the ones of any pattern of ones is 4. (Hint: try to find an example that requires more rectangles.)

The Karnaugh map to the right is the worst possible map. You cannot add or take away a one without resulting in either the same or fewer rectangles. Therefore, the answer is true.

		C	
		0	1
AB	00	1	0
	01	0	1
	11	1	0
	10	0	1

12. **True** or False: The \bar{S} and \bar{R} inputs to a D-latch have priority over the D and clock inputs.

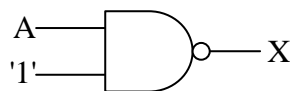
13. Which of the following products produces the truth table to the right?

- a.) $A \cdot B \cdot \bar{C}$ b.) $\bar{A} \cdot \bar{B} \cdot C$ c.) $A \cdot \bar{B} \cdot C$
 c.) $A \cdot B \cdot C$ **d.) $\bar{A} \cdot B \cdot \bar{C}$** d.) None of the above

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

The truth table to the right equals 1 only when $A = 0$ and $B = 1$ and $C = 0$, i.e., when $\bar{A} = 1$ and $B = 1$ and $\bar{C} = 1$. Therefore, the answer is d.

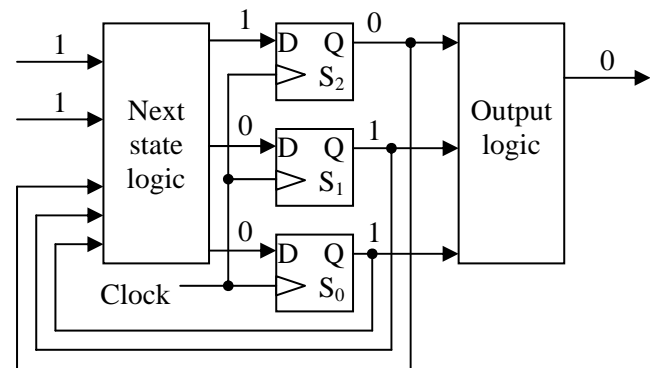
14. Fill in the truth table for the NAND circuit shown below.



A	X
0	1
1	0

The truth table for a NAND gate shows that the only time a zero is output is if all of the inputs equal 1. Therefore, when $A=0$, the output X must equal 1. When $A=1$, then both of the inputs to the NAND gate equal 1, and a 0 is output. This gives us the truth table above which looks just like that of an inverter.

The next four problems use the state machine diagram to the right. Assume that the states are numbered so that bit S_2 is the MSB and bit S_0 is the LSB.



15. How many rows does the next state truth table have for this system?

With three inputs from the current state and two external inputs, we have a total of five inputs for the next state logic. This gives us $2^5 = 32$ possible combinations of ones and zeros, each identifying a unique row in the truth table.

16. How many rows does the output truth table for this system have?

The output logic depends only on the current state which is represented with three binary variables. Therefore, the output logic truth table has $2^3 = 8$ possible combinations of ones and zeros identifying each row of the truth table.

17. What is the current state of this system? Keep your answer in binary.

The current state is represented with the state variables S_2 , S_1 , and S_0 which are output from the three latches at the center of the circuit. (S_2 being the most significant bit.) Therefore, the current state is **011₂**.

18. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

The next state is represented with the inputs to the latches for the state variables S_2 , S_1 , and S_0 . (S_2 being the most significant bit.) Therefore, the current state is **100₂**.

19. True or **False**: Renumbering the states of a state machine has no effect on the "next state" logic for the digital hardware implementation.

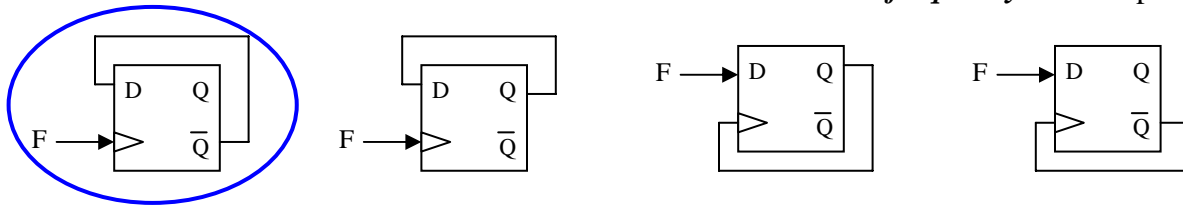
The numbering of the states directly affects the next state truth table, and therefore changes the logic that is derived from it. Therefore, the answer is **False**.

20. How many latches will a state machine with 16 states require?

- a.) 1 b.) 2 c.) 3 **d.) 4** e.) 5 f.) 6 g.) 7

Sixteen states will be numbered 0, 1, 2, 3, ..., 14, and 15. Since $15_{10} = 1111_2$, we will need 4 bits to represent the state. **Therefore, the answer is d.** Another way of looking at it is to see how many states it is possible to represent with n bits, and to figure out what value of 2^n is greater than or equal to 16. 2^4 fits that bill.

21. Place a circle around the circuit below that can be used to divide the *frequency* of the input F by 2.



22. In a truth table, the symbol ↓ represents an input that is:

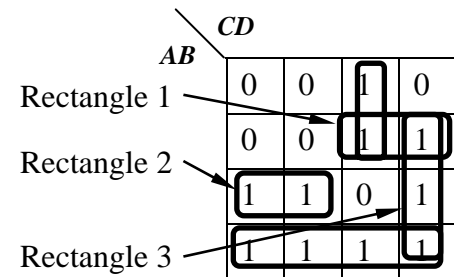
- a.) a logic 0 **c.) changing from a 1 to a 0** e.) this is an output symbol, not an input
 b.) a logic 1 d.) changing from a 0 to a 1 f.) a "don't care"

23. For the Karnaugh map to the right, identify the problems with each of the three rectangles shown. (2 points each)

Rectangle 1: This rectangle does not have a unique cell in it. All of its cells are covered with other rectangles.

Rectangle 2: This rectangle could have been twice as large by including the two cells of ones directly beneath it.

Rectangle 3: This rectangle contains a non-power of two number of cells. The best solution would be to drop the bottom cell so that it contained two cells, then deleting rectangle 1.



A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Medium answers – 4 points each

24. Complete the truth table to the right with the values for the following Sum-of-Products expression:

$$X = (\bar{A} \cdot \bar{B} \cdot C) + (\bar{A} \cdot B) + (A \cdot \bar{B} \cdot \bar{C})$$

$(\bar{A} \cdot \bar{B} \cdot C)$ This term equals one when A=0, B=0, and C=1.

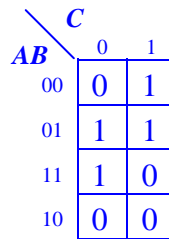
$(\bar{A} \cdot B)$ This term equals one when A=0, B=1, and C=1 or 0.

$(A \cdot \bar{B} \cdot \bar{C})$ This term equals one when A=1, B=0, and C=0.

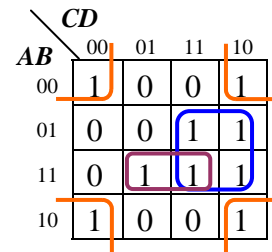
All of the other rows should contain zeros.

25. Create a Karnaugh map from the truth table below. *Do not worry about making the rectangles.*

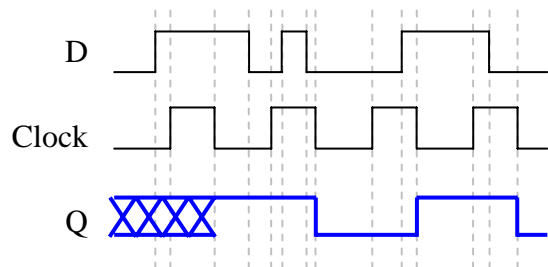
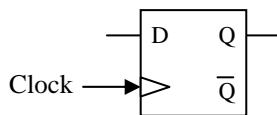
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0



26. In the Karnaugh map to the right, draw the best pattern of rectangles you can. *Do not derive the SOP expression.*



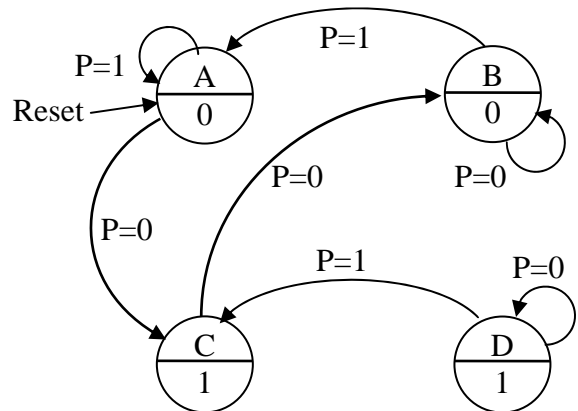
27. Show the D latch output waveform Q based on the inputs D , \bar{S} , \bar{R} , and clock indicated in the graph to the right. Assume the latch captures on the falling edge. (The figure below is just for a reference.)



28. Identify the *two* errors in the state diagram shown to the right.

First of all, there is no transition out of state C for when P equals 1. Remember that there must be a transition for EVERY possible input, even if it is an arrow going back into the same state to indicate we're not going anywhere.

The second error is for state D. There is no way to get to it. Even if there is a reset, the machine cannot get to state D.

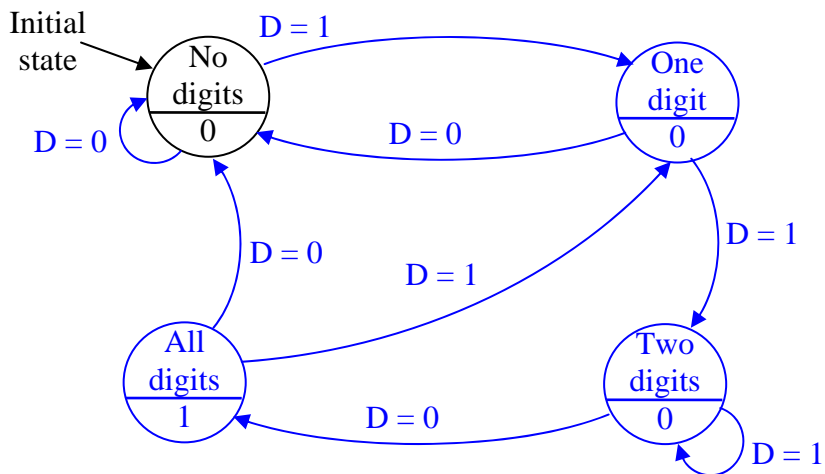


Longer answers – Points vary per problem

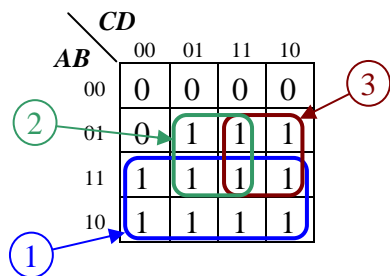
29. Make the state diagram that will output a '1' when the sequence '110' is detected in a serial stream of bits. For example, if the following binary stream is received:

1 1 1 0 0 1 1 1 1 1 0 0 1 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0

then 1's will be output here. Otherwise, the system will output zeros. Label the input D. (8 points)



30. Derive the minimum SOP expression from the Karnaugh map below. (6 points)



Rectangle 1

A	B	C	D
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	0	0
1	0	0	1
1	0	1	1
1	0	1	0

Rectangle 2

A	B	C	D
0	1	0	1
0	1	1	1
1	1	0	1
1	1	1	1

A and C drop out.
Neither B nor D equal 0, so neither term is inverted.

Rectangle 3

A	B	C	D
0	1	1	1
0	1	1	0
1	1	1	1
1	1	1	0

A and D drop out.
Neither B nor C equal 0, so neither is inverted.

B, C, and D drop out. Since A is equal to 1 for all cells, it is not inverted.

$B \cdot D$

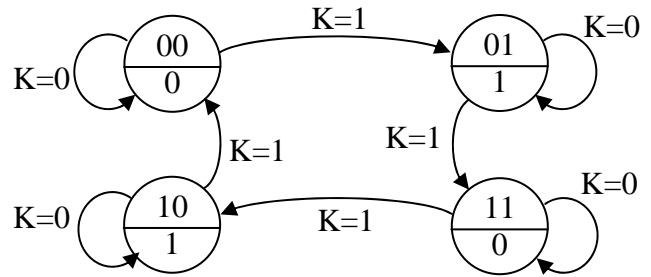
$B \cdot C$

A

The final answer is:

$A + B \cdot D + B \cdot C$

31. Create the next state truth table and the output truth table for the state diagram to the right. Use the variable names S_1 and S_0 to represent the most significant and least significant bits respectively of the binary number identifying the state. (8 points)



Next State T.T.

S_1	S_0	K	S_1'	S_0'
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

Output T.T.

S_1	S_0	X
0	0	0
0	1	1
1	0	1
1	1	0

32. The three Boolean expressions below represent the *next state bits* (S_0' and S_1') and the *output bit* X based on the *current state* (S_0 and S_1). Draw the logic circuit for the state machine including the latches and output circuitry. Be sure to label the latch inputs and other signals. (8 points)

$$S_0' = \bar{S}_1$$

$$S_1' = \bar{S}_0$$

$$X = S_1 \cdot S_0$$

