

CS/EE 6710

CMOS Processing

N-type Transistor

Drain
N+
Gate
Poly Gate
Gate Oxide
Diffusion
Source
N+
P-doped substrate

D
G
S
+Vgs
Vds
i
electrons

N-type from the top

Poly Gate
Diffusion
Drain
Gate
Source
P-doped substrate

► Top view shows patterns that make up the transistor

Diffusion Mask

Drain
Diffusion
Source
P-doped substrate

► Mask for just the diffused regions

Polysilicon Mask

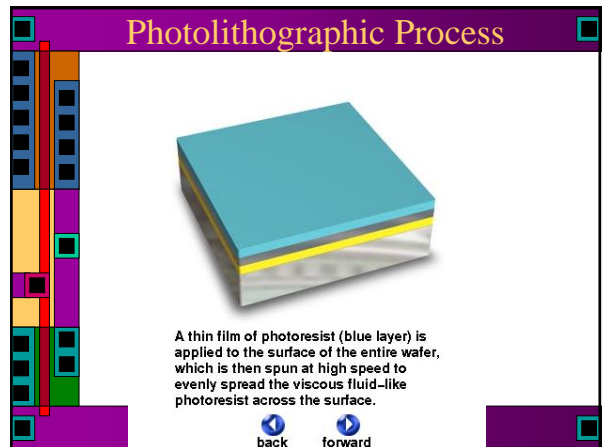
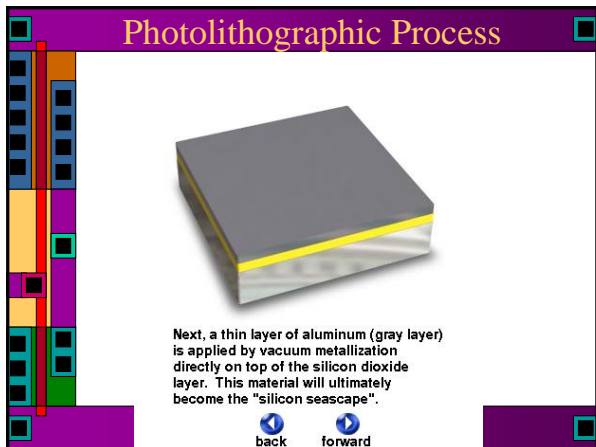
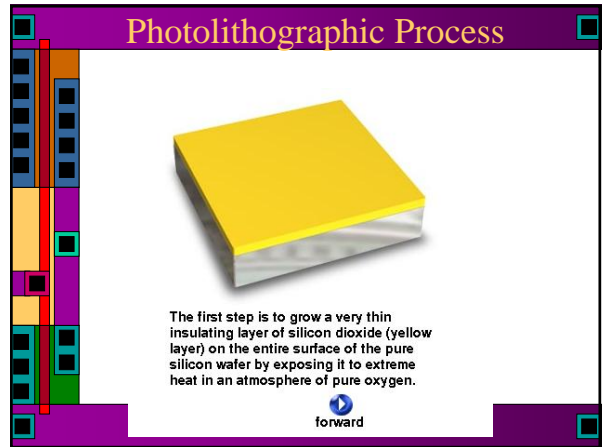
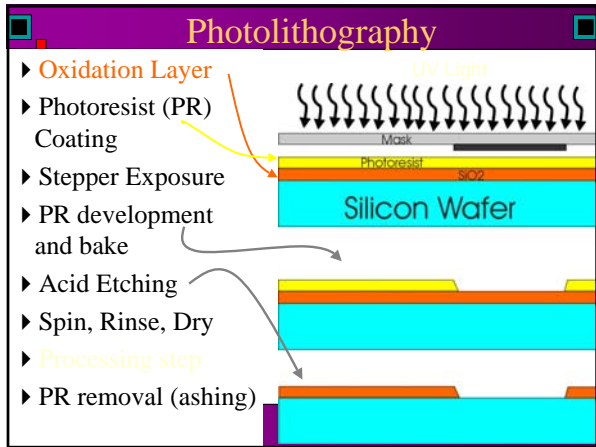
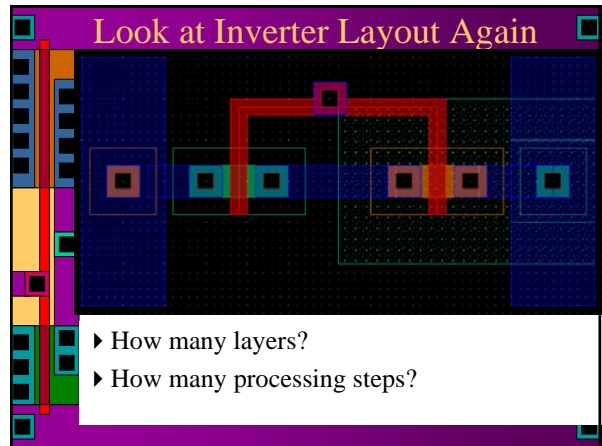
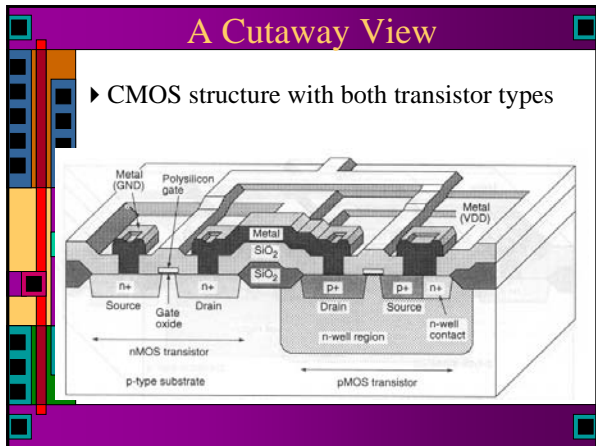
Gate
P-doped substrate

► Mask for just the polysilicon areas

Combine the two masks

Drain
N+
Gate
Poly Gate
Gate Oxide
Diffusion
Source
N+
P-doped substrate

► You get an N-type transistor
► There are other steps in the process...



Photolithographic Process

A mask containing the pattern of the sailboat, the sun, and a seagull is then placed over the wafer and ultraviolet light is then passed through the pattern exposing the soft photoresist beneath.

back forward

Photolithographic Process

The soft unexposed photoresist is removed with an organic solvent leaving only those areas that were hardened by exposure to the ultraviolet light. An outline of the seascape is now in place.

back forward

Photolithographic Process

The exposed areas of aluminum metal are now removed by "etching" the surface of the wafer in a process called ion beam milling that removes the unprotected aluminum.

back forward

Photolithographic Process

The hardened photoresist is then removed by washing with acid and the seascape is finished. We can now photograph it through a microscope and add it to the gallery in the Silicon Zoo.

back

Growing the Silicon Crystal

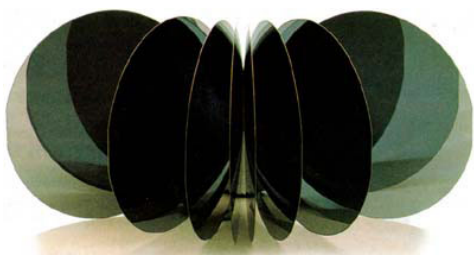
Single Crystal Silicon Ingot

- ▶ Need single crystal structure
- ▶ Single crystal vs. Polycrystalline silicon (Poly)

Czochralski Method

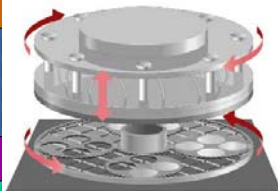
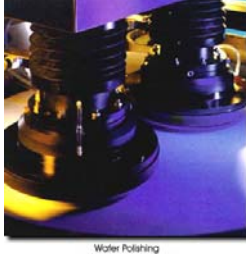

- ▶ Need single-crystal silicon to accept impurities correctly
 - ▶ Donor elements provide electrons
 - ▶ Acceptor elements provide holes
- ▶ Pull a single crystal of silicon from a puddle of molten polycrystalline silicon

Slice Crystal into Wafers

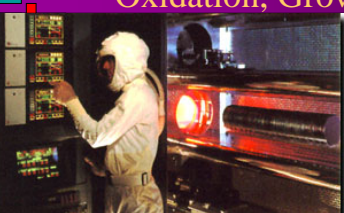
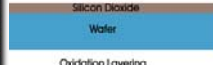


▶ Slice into thin wafers (.25mm - 1.0mm), and polish to remove all scratches

Lapping and Polishing

Oxidation, Growing SiO₂

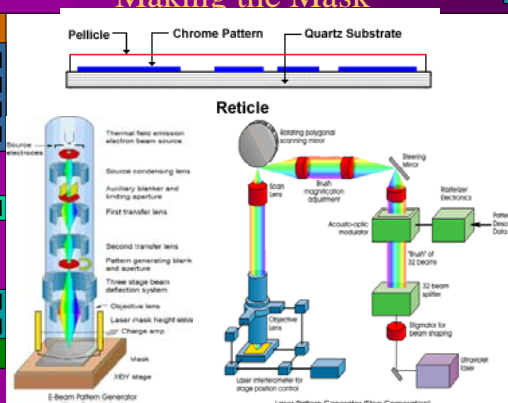



Oxidation Furnace
(Silicon Valley Group - Thermco Systems)

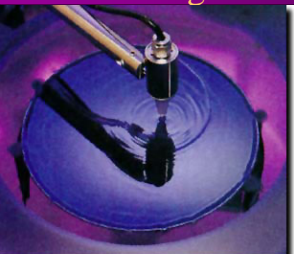
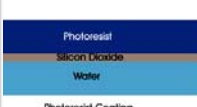
▶ Essential property of silicon is a nice, easily grown, insulating layer of SiO₂

- ▶ Use for insulating gates ("thin oxide")
- ▶ Also for "field oxide" to isolate devices

Making the Mask



Adding Photoresist


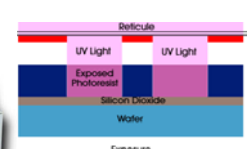



Photoresist Application
(Oritrak)

▶ Photoresist can be positive or negative

- ▶ Does the exposed part turn hard, or the unexposed part?

"Steppers" Expose the Mask





Stepper
(ASM Lithography)


▶ Use very short wavelength UV light

- ▶ Single frequency, 436 - 248 nm
- ▶ Expensive! ~\$5,000,000/machine...

Develop and Bake Photoresist




Oxidation Furnace
(Silicon Valley Group - Thermco Systems)



Photoresist Develop & Strip

- ▶ Developed photoresist is soft, unexposed is hardened
- ▶ So you can etch away the soft (exposed) part

Now Etch the SiO₂



Automated Acid Etch
(SEZ)



Oxide Etch




SRD (Spin, Rinse, Dry)
(SEZ)

- ▶ Etch the SiO₂ to expose the wafer for processing
- ▶ Then Spin Rinse, and Dry

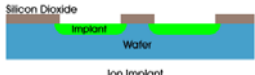
Add a Processing Step

- ▶ Now that we've got a pattern etched to the right level, we can process the silicon
- ▶ Could be:
 - ▶ Ion Implantation (I.e. diffusion)
 - ▶ Chemical Vapor Deposition (silicide, Poly, insulating layers, etc.)
 - ▶ Metal deposition (evaporation or sputtering)
 - ▶ Copper deposition (very tricky)


Ion Implantation



Ion Implanter
(Varian Associates)



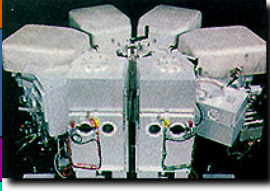
Ion Implant




Ion Implanter Steering Magnets
(Varian Associates)

- ▶ Implant ions into the silicon
- ▶ Donor or Acceptor

Chemical Vapor Deposition

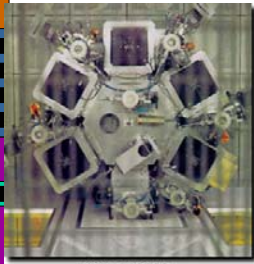


CVD Tool
(Applied Materials)

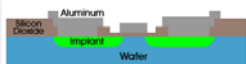


CVD Tool
(Applied Materials)

Metal Deposition

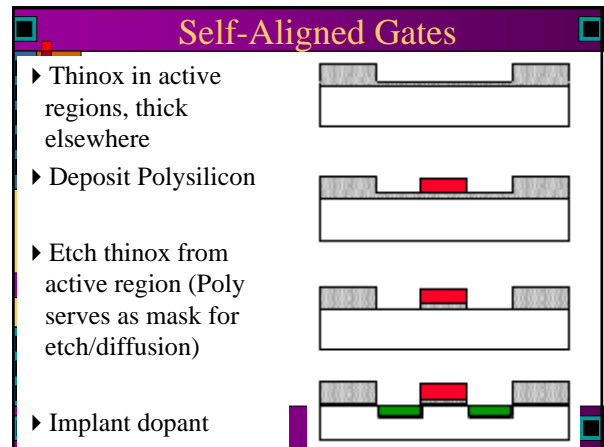
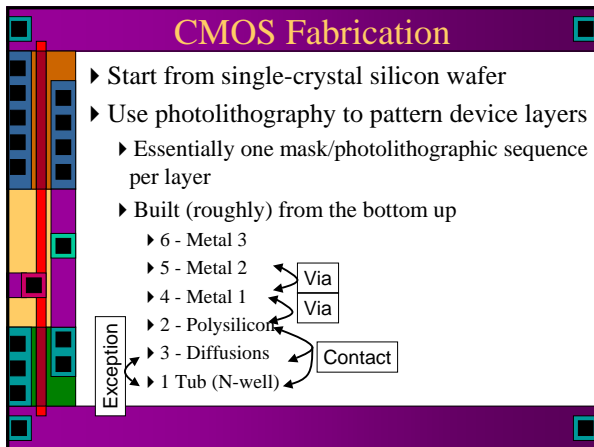
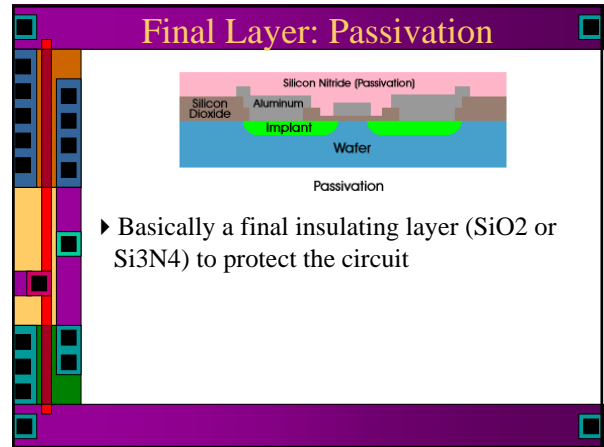
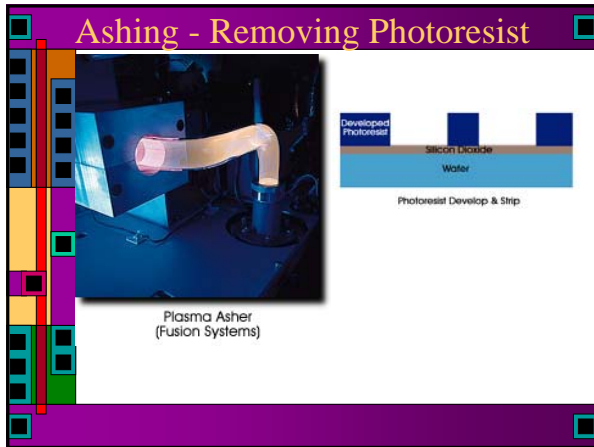
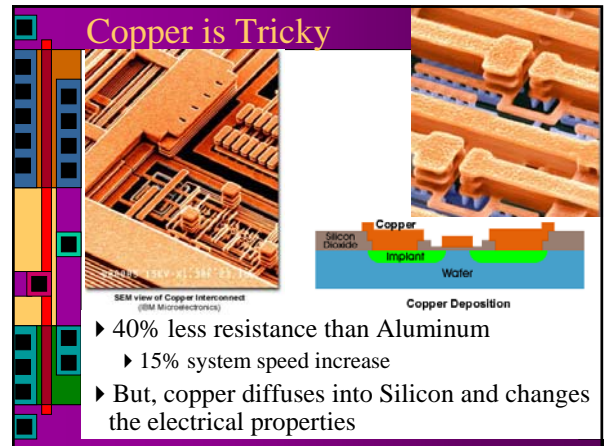


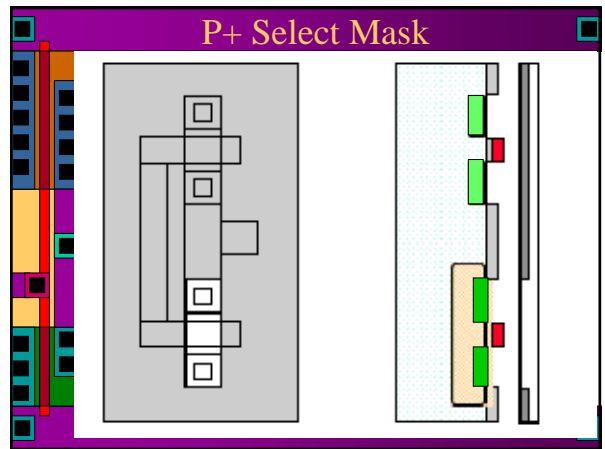
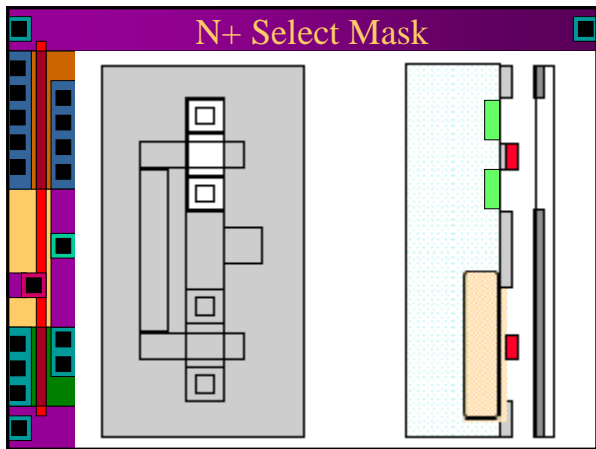
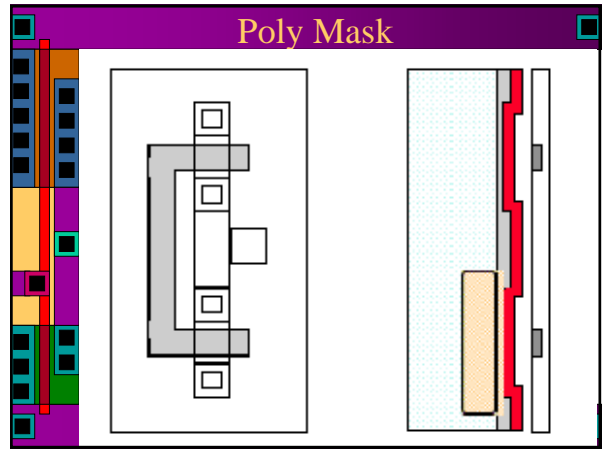
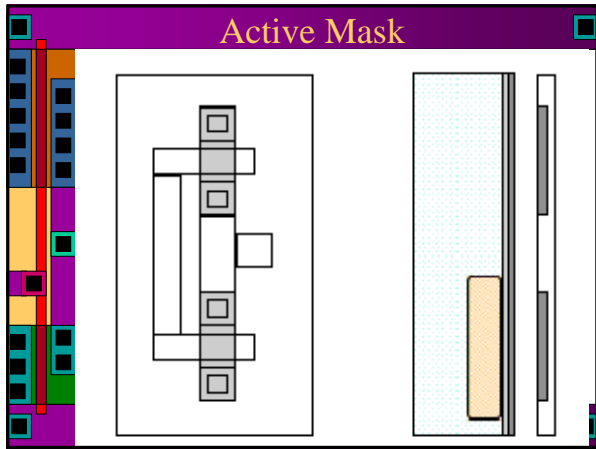
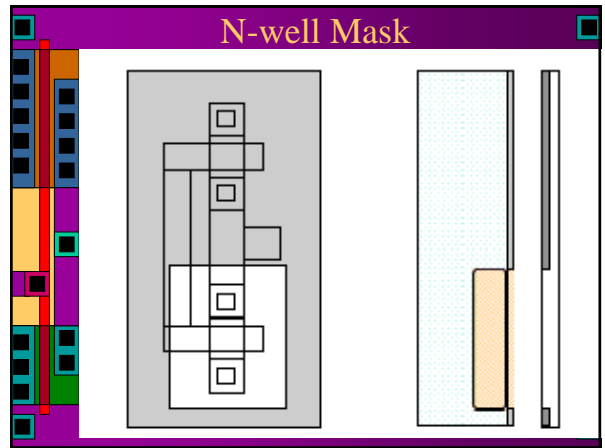
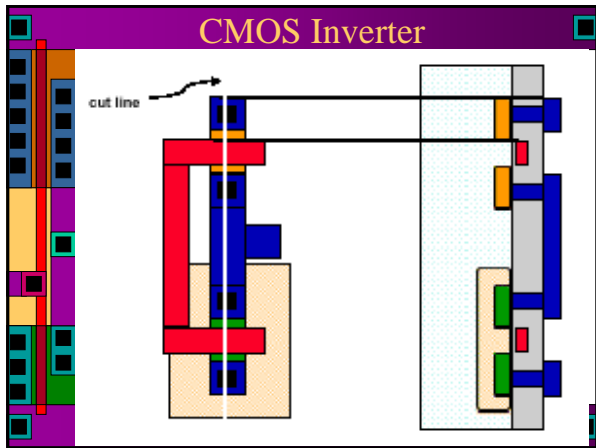
PVD Sputtering tool
(Sputtered Films Corporation)

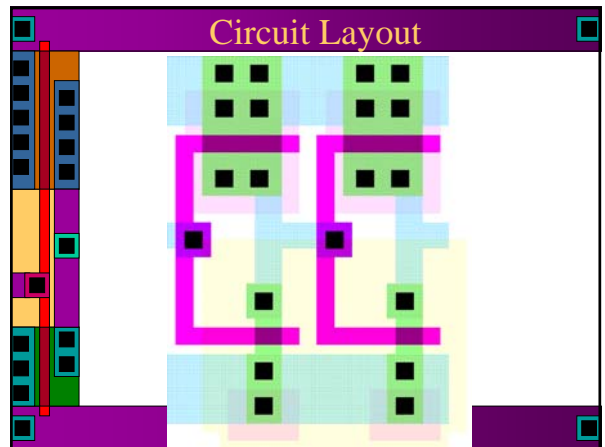
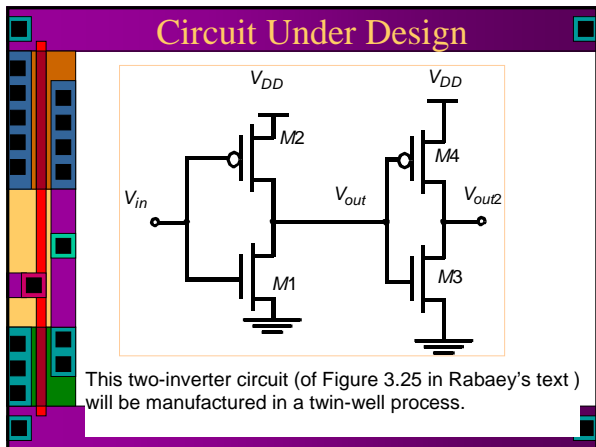
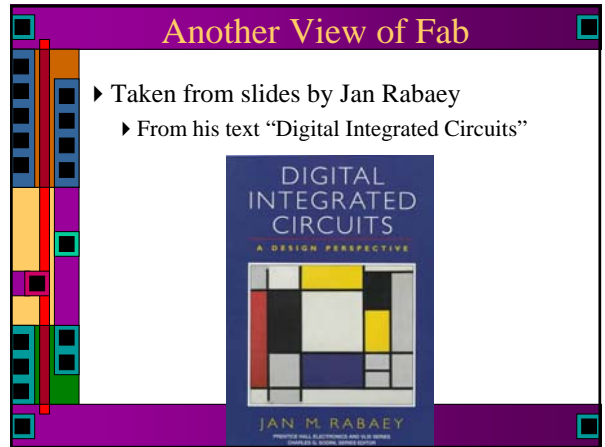
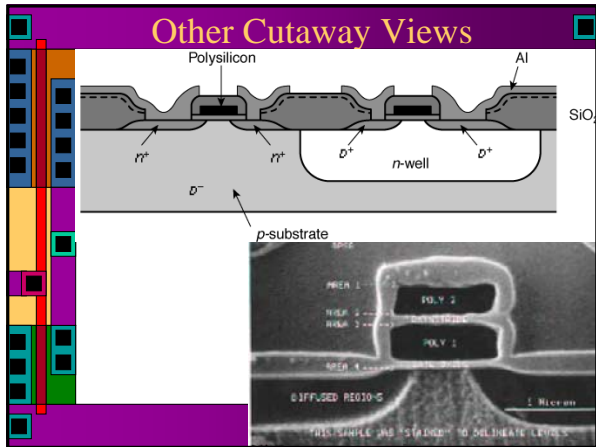
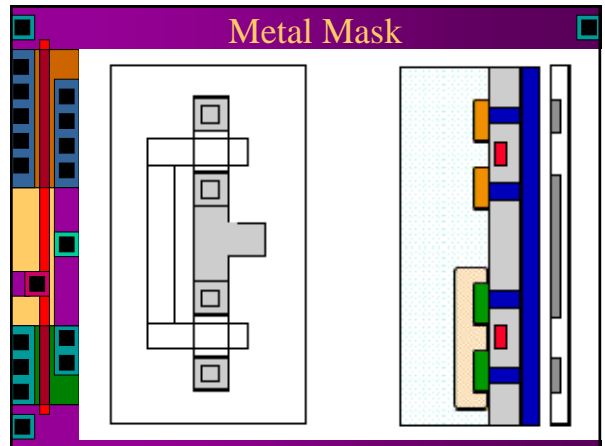
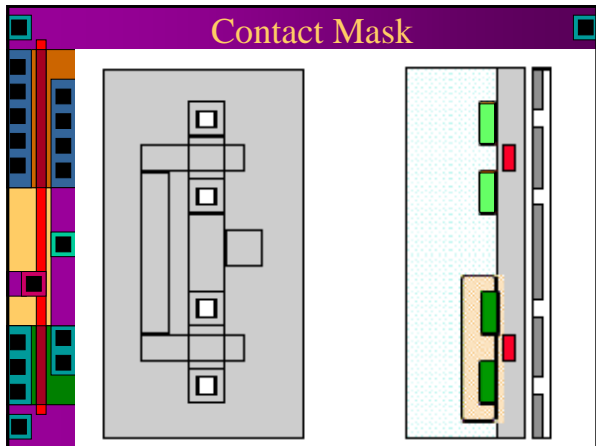


Metal Deposition

- ▶ Typically aluminum, gold, tungsten, or alloys







Start Material

Starting wafer: n-type with doping level = $10^{19}/\text{cm}^3$

* Cross-sections will be shown along vertical line A-A'

N-well Construction

- (1) Oxidize wafer
- (2) Deposit silicon nitride
- (3) Deposit photoresist

N-well Construction

- (4) Expose resist using n-well mask

N-well Construction

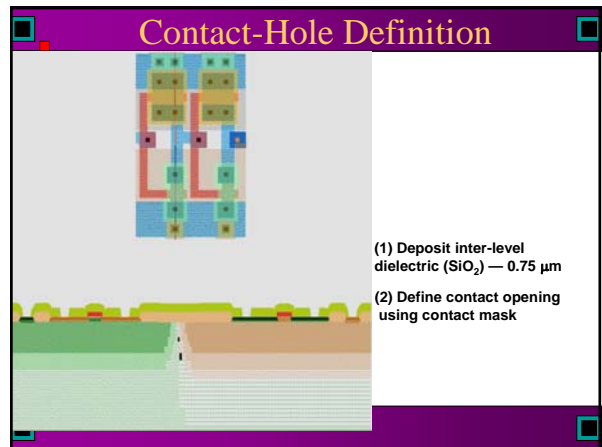
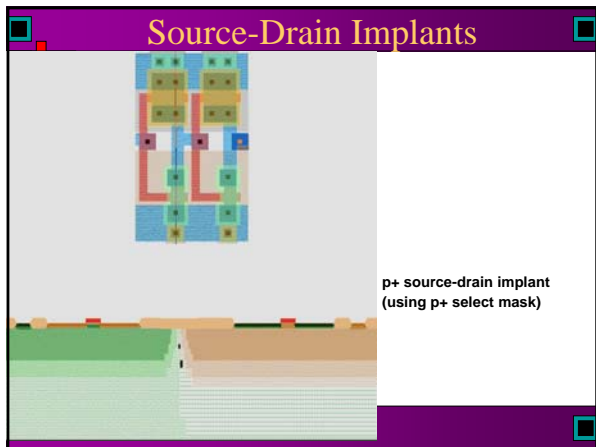
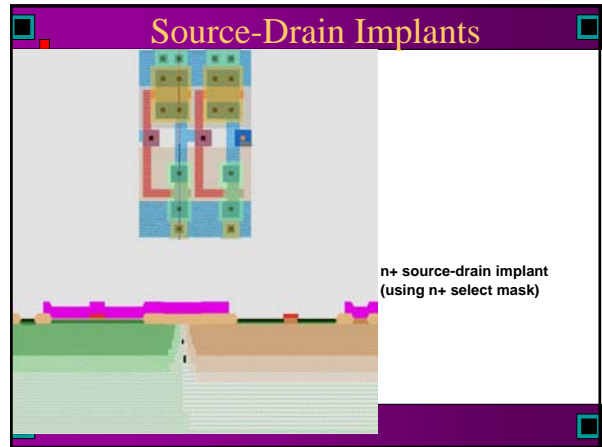
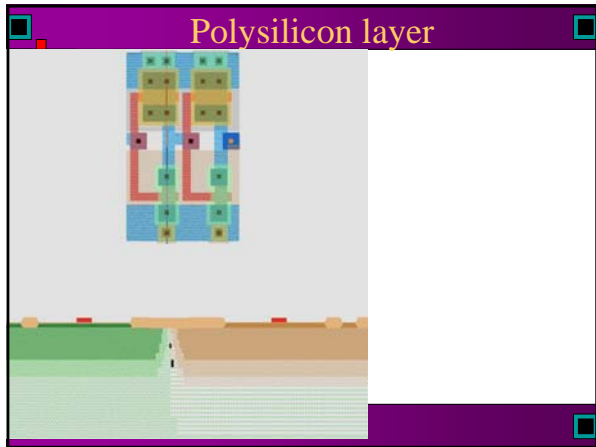
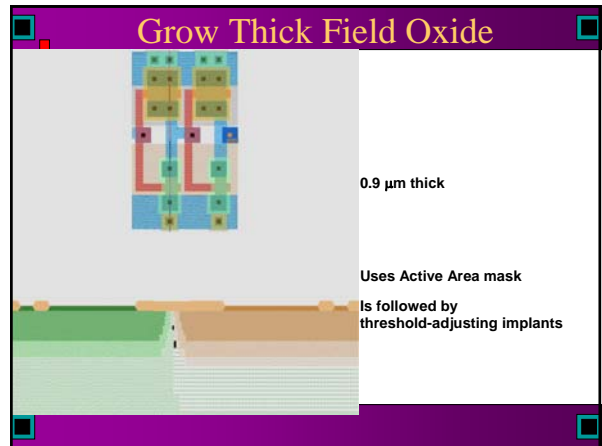
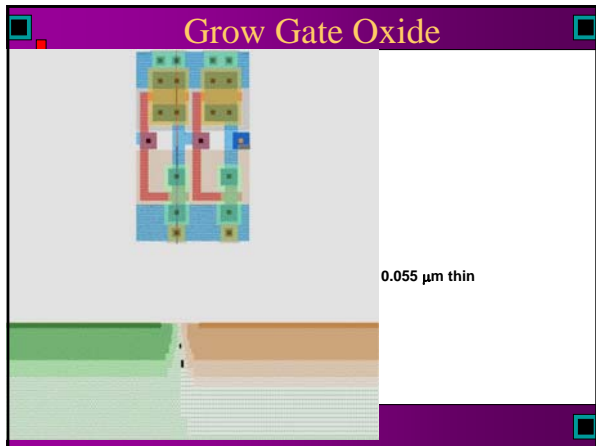
- (5) Develop resist
- (6) Etch nitride and
- (7) Grow thick oxide

N-well Construction

- (8) Implant n-dopants (phosphorus) (up to 1.5 μm deep)

P-well Construction

Repeat previous steps



Aluminum-1 Layer

