**Design Project: Pulse-Width Modulation (PWM) signal generator**



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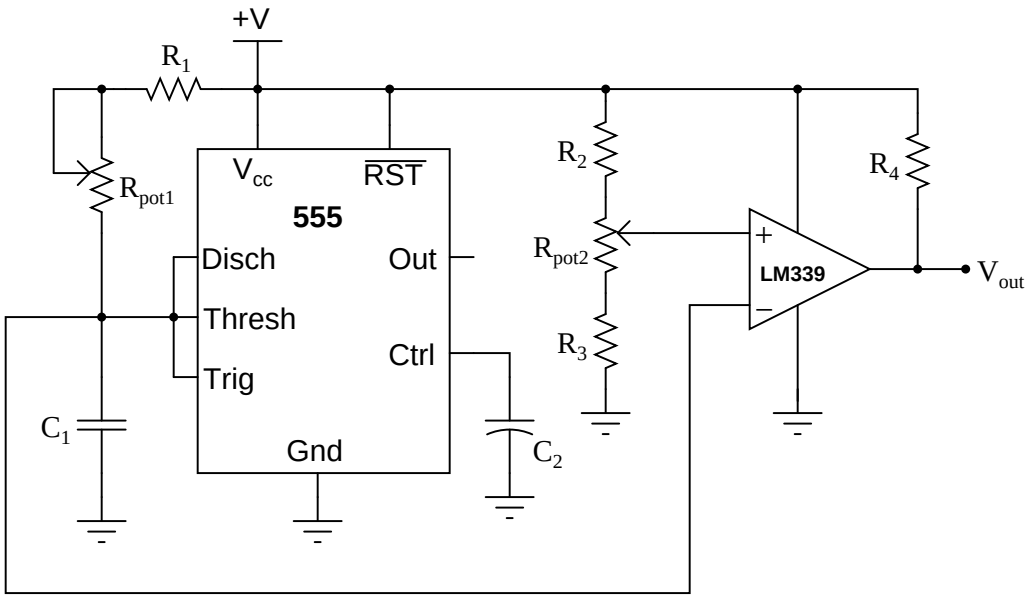
Your project is to build a specialized signal generator that produces variable frequency, variable duty cycle square waves suitable for driving power transistors to control load power by pulse width modulation. The following schematic diagram is recommended:




$R_1$, $R_{pot1}$, and $C_1$ set the oscillation frequency. $R_{pot2}$ sets the duty cycle.

Deadlines (set by instructor):

- Project design completed:
- Components purchased:
- Working prototype:
- Finished system:
- Full documentation:

**Questions**

Question 1

What shape of voltage waveform would you expect to measure (using an oscilloscope) across capacitor $C_1$? How does this waveform interact with the DC reference voltage at the wiper of $R_{pot2}$ to produce a pulse-width modulated square wave output?

file 03195

Question 2

Which direction would you have to move the wiper on potentiometer $R_{pot2}$ to *increase* the duty cycle of the output waveform? Explain your answer.

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Question 3

The design recommendation for this circuit is to make resistors $R_2$ and $R_3$ both equal to the resistance of the potentiometer $R_{pot2}$. This way, the full mechanical range of the potentiometer will be useful for adjusting duty cycle: fully turning it one way will just produce a 0% duty cycle, while fully turning it the other way will just produce a 100% duty cycle.

Explain why those resistor values need to be equal to achieve this optimum usage of pot range. Hint: it has something to do with the internal workings of the 555 timer IC.

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Question 4

It is important to not make resistor $R_1$ too small in value. Explain why, and what might happen if it were.

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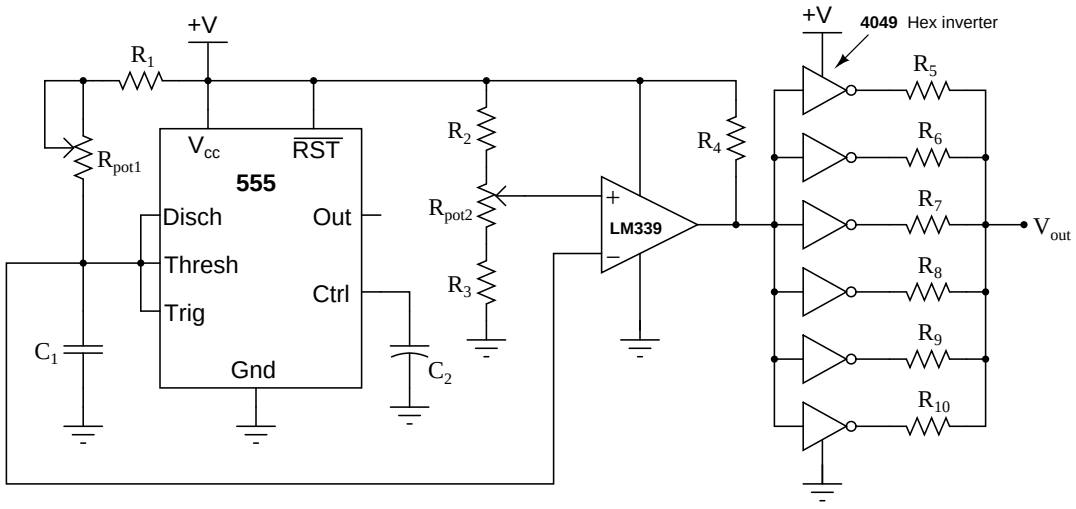
Question 5

For those of you who are used to working with regular opamps, the presence of resistor $R_4$ may be a mystery. It is necessary because of a special limitation of the type LM339 comparator IC. Research and explain what this limitation is.

file 03197

Question 6

The following modification may be made to the circuit to provide it with additional output current capability:




Here, six CMOS inverters (IC part number 4049) are ganged together in parallel to supply significantly more sourcing and sinking current capability than the LM339-with-pullup-resistor could on its own. Since CMOS logic gates are inherently on-or-off devices, they have no trouble handling the square wave output of the LM339.

Two questions here: first, why all the resistors at the outputs of the inverter gates? Why not just connect all the inverter outputs directly in parallel? Secondly, what value of resistor would you suggest at the output of each gate ($R_5$ through $R_{10}$)?

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**Answers**

Answer 1

The waveform will be a "sawtooth" shape. When compared against the DC reference voltage at $R_{pot2}$'s wiper by the LM339 comparator IC, the result is a square wave of varying duty cycle.

Answer 2

Moving the wiper *up* (as drawn in the schematic) produces greater duty cycles.

Answer 3

The sawtooth signal seen at capacitor $C_1$ (with reference to ground) oscillates between $\frac{1}{3}$ and $\frac{2}{3}$ supply voltage.

Answer 4

In the 555's discharge cycle, resistor $R_1$ will drop (almost) the full power supply voltage when $R_{pot1}$ is set for minimum resistance. Not only could this overheat $R_1$, but it could also damage the discharge transistor within the 555 timer.

Answer 5

The LM339 comparator is only able to *sink* current at its output. Therefore, $R_4$ acts as a *pullup* resistor.

Follow-up question: is this (overall) circuit capable of sourcing current to a load? Explain why or why not.

Answer 6

The resistors prevent the (unlikely) occurrence of a short-circuit between two or more inverter gates, if one gate happens to fail high or low, or if some gates are significantly slower than others (and thus will "fight" with the faster gates during each transition).

Challenge question: adding inverter gates to the output of this circuit has an interesting effect on the duty cycle control. The potentiometer will now act backward from the way it was before (decreasing duty cycle when it formerly increased duty cycle, and visa-versa). Explain why.

## Notes

Notes 1

Many students will initially be puzzled by the operating principle of this circuit. The best way I have found to answer their questions, I have found, is with a multi-trace oscilloscope (preferably one that can show three traces simultaneously). Connect one channel to the top of $C_1$, the next channel to $R_{pot2}$'s wiper, and the third to the comparator's output terminal. A picture, as they say, is worth a thousand words.

Notes 2

Notice that I did not even hint at *why* this is. Ask your students to fully explain their answers!

Notes 3

This question forces students to explore what the 555 is really doing, and to recognize the comparator's function in generating PWM square waves.

Notes 4

In order to really understand *why* insufficient resistance at $R_1$ would be a bad thing, students must understand the astable operating cycle of the 555 timer. This question provides a very practical context in which to explore and/or review it!

Notes 5

This characteristic of the LM339 caused problems for me the first few times I tried to use it in my designs. Despite this limitation, though, the LM339 is very aptly suited for this application with its fast response and very wide power supply voltage limits.

Notes 6

This question may or may not be suitable for your students, depending on whether or not they have studied logic gates yet. If they have not yet studied digital circuits, it may be wise to skip this question!

Note that I did not answer the question of resistor sizes. Discuss this with your students, and let them determine how these resistors should be sized. Let them have access to datasheets for the 4049 inverter IC, and ask them what parameter(s) would be the most important in this decision.

If no one notices, point out how the power supply wires are drawn for the six-gate (hex) inverter. This is a common way to show power wiring for multiple gates (or opamps, or any other sort of IC where complex elements are duplicated).