IEEE 1149.1 (JTAG) Boundary-Scan Testing

in Altera Devices

September 2000, ver. 4.05 Application Note 39

Introduction

As printed circuit boards (PCBs) become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods—e.g., external test probes and "bed-of-nails" test fixtures—harder to implement. As a result, cost savings from PCB space reductions are sometimes offset by cost increases in traditional testing methods.

In the 1980s, the Joint Test Action Group (JTAG) developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing.

This BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. Figure 1 illustrates the concept of boundary-scan testing.

Figure 1. IEEE Std. 1149.1 Boundary-Scan Testing

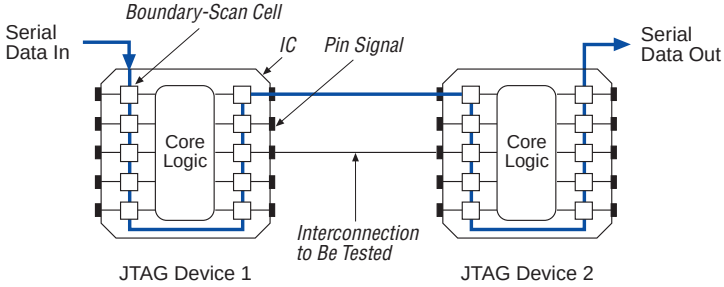


Table 1 summarizes the Altera® devices that comply with the IEEE Std. 1149.1 specification by providing BST capability for input, output, and dedicated configuration pins.

Table 1. Altera Devices with BST Capability

Family	Devices Supporting BST
APEX® 20K, APEX 20KE	All devices
ACEX® 1K	All devices
FLEX® 10K, FLEX 10KE	All devices
FLEX 8000	EPF8282A, EPF8282AV, EPF8636A, EPF8820A, EPF81500A
FLEX 6000	All devices
MAX® 9000 (including MAX 9000A)	All devices
MAX 7000S *(1)*	EPM7128S, EPM7160S, EPM7192S, EPM7256S
MAX 7000A	All devices
MAX 7000B	All devices
MAX 3000A	All devices

Note:
(1) The EPM7032S, EPM7064S, and EPM7096S devices contain an IEEE Std. 1149.1 controller for in-system programming. However, these devices do not support BST.

This application note discusses how to use the IEEE Std. 1149.1 BST circuitry in Altera devices. The topics are as follows:

- IEEE Std. 1149.1 BST architecture
- IEEE Std. 1149.1 boundary-scan register
- IEEE Std. 1149.1 BST operation control
- Enabling IEEE Std. 1149.1 BST circuitry
- Guidelines for IEEE Std. 1149.1 boundary-scan testing
- Boundary-Scan Description Language (BSDL) support
- References

In addition to BST, you can use the IEEE Std. 1149.1 controller for in-system programming in MAX 9000 (including MAX 9000A), MAX 7000S, MAX 7000A, MAX 7000B, and MAX 3000A devices and for in-circuit reconfiguration in APEX 20K, ACEX 1K, and FLEX 10K devices. This application note only discusses the BST feature of the IEEE Std. 1149.1 circuitry.

For more information on using IEEE Std. 1149.1 circuitry for in-system programming and in-circuit reconfiguration, go to the following documents:

- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*
- *Application Note 95 (In-System Programmability in MAX Devices)*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)*

IEEE Std. 1149.1 BST Architecture

A device operating in IEEE Std. 1149.1 BST mode uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. Table 2 summarizes the functions of each of these pins.

Table 2. IEEE Std. 1149.1 Pin Descriptions

Pin	Description	Function
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.
TRST	Test reset input (optional)	Active-low input to asynchronously reset the boundary-scan circuit. This pin is only available in certain APEX 20K, ACEX 1K, FLEX 10K, and FLEX 8000 devices (TRST is optional according to IEEE Std. 1149.1).

APEX 20K, ACEX 1K, FLEX 10K and MAX 9000 devices have pins dedicated for IEEE Std. 1149.1 operation. For EPF8820A, EPF8636A, EPF8282A, EPF8282AV, FLEX 6000, MAX 7000S, MAX 7000A, MAX 7000B, and MAX 3000A devices, you can use the four JTAG pins as I/O pins by turning off the JTAG option with the MAX+PLUS II software (see "Enabling IEEE Std. 1149.1 BST Circuitry" on page 24 of this application note). Certain APEX 20K, ACEX 1K, FLEX 10K, and FLEX 8000 JTAG devices have the optional TRST pin.

Go to the appropriate device family data sheet for specific information on device and package combinations.

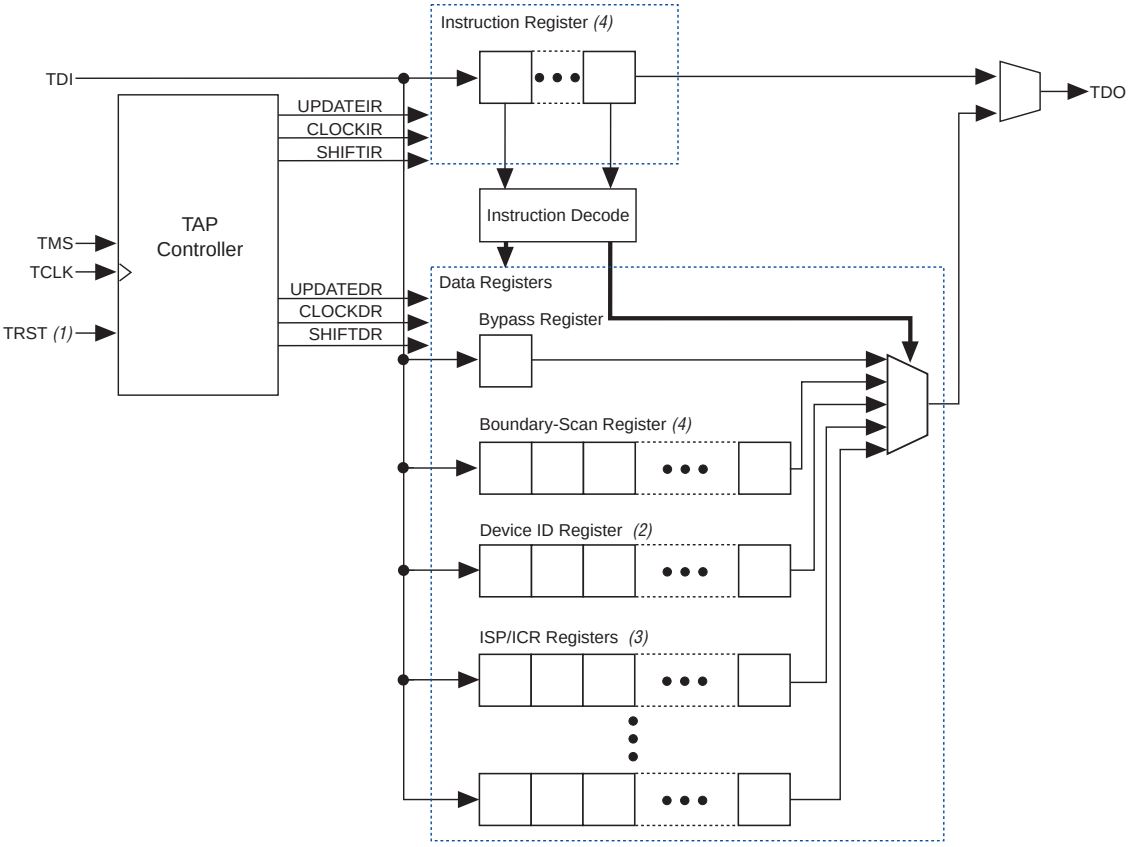
The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register which is used to determine the action to be performed and the data register to be accessed.

- The bypass register which is a 1-bit-long data register used to provide a minimum-length serial path between TDI and TDO.
- The boundary-scan register which is a shift register composed of all the boundary-scan cells of the device.

Figure 2 shows a functional model of the IEEE Std. 1149.1 circuitry.

Figure 2. IEEE Std. 1149.1 Circuitry



Notes:

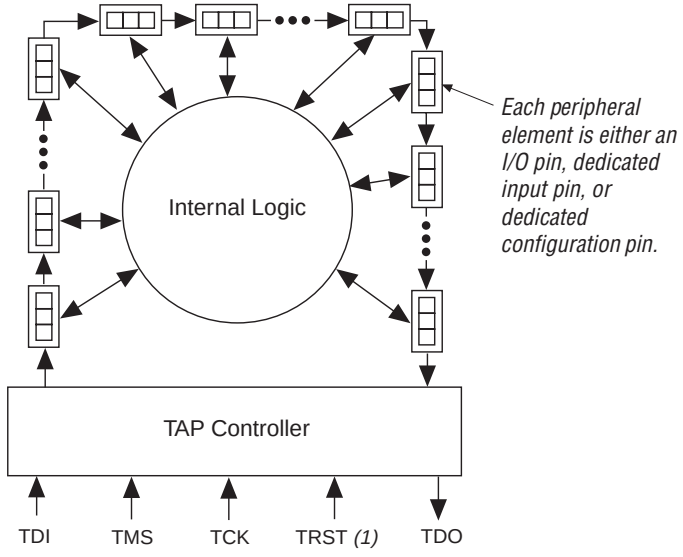
(1) The TRST pin is available in APEX 20K, ACEX 1K, and some FLEX devices.
(2) The device ID register is available in all JTAG-compliant families except EPM9320 and EPM9560 devices.
(3) The private registers are used for in-system programmability (ISP) in MAX 9000 (including MAX 9000A), MAX 7000A, MAX 7000B, MAX 7000S, and MAX 3000A devices and for in-circuit reconfigurability (ICR) in APEX 20K, ACEX 1K, and FLEX 10K devices.
(4) Refer to the appropriate device family data sheet for register lengths.

IEEE Std. 1149.1 boundary-scan testing is controlled by a Test Access Port (TAP) Controller, which is described in "IEEE Std. 1149.1 Std. Operation Control" on page 15 of this application note. The TMS, TRST, and TCK pins operate the TAP controller, and the TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are either I/O pins (all devices), dedicated inputs (all devices), or dedicated configuration pins (APEX, ACEX, and FLEX devices). You can use the boundary-scan register to test external pin connections or to capture internal data. Figure 3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 3. Boundary-Scan Register



Note:
(1) The TRST pin is available in APEX 20K, ACEX 1K, and some FLEX devices.

I/O Pin

The 3-bit boundary-scan cell (BSC) consists of a set of capture registers and a set of update registers for each I/O pin. The capture registers connect to internal device data via the OUTJ, OEJ, and I/O pin signals, while the update registers connect to external data through the tri-state data input, tri-state control, and INJ signals. The control signals for the IEEE Std. 1149.1 BST registers (e.g., SHIFT, CLOCK, and UPDATE) are generated internally by the TAP controller; the MODE signal is generated by a decode of the instruction registers. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device. Figure 4 shows the BSCs associated with each I/O pin in APEX 20K, ACEX 1K, FLEX 10K, and FLEX 8000 devices.

Figure 4. APEX 20K, ACEX 1K, FLEX 10K & FLEX 8000 I/O Pins with IEEE Std. 1149.1 BST Circuitry

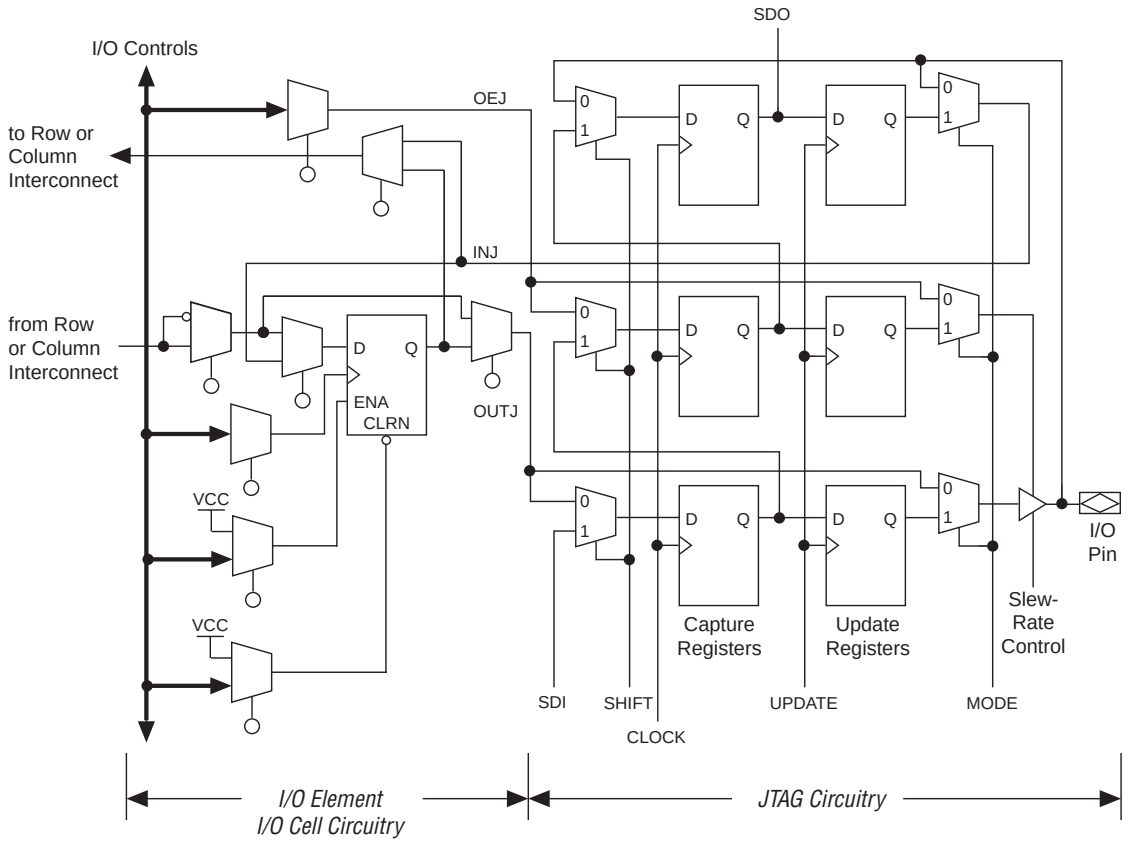


Figure 5 shows the BSCs associated with each I/O pin in MAX 9000 devices.

Figure 5. MAX 9000 I/O Pins with IEEE Std. 1149.1 BST Circuitry

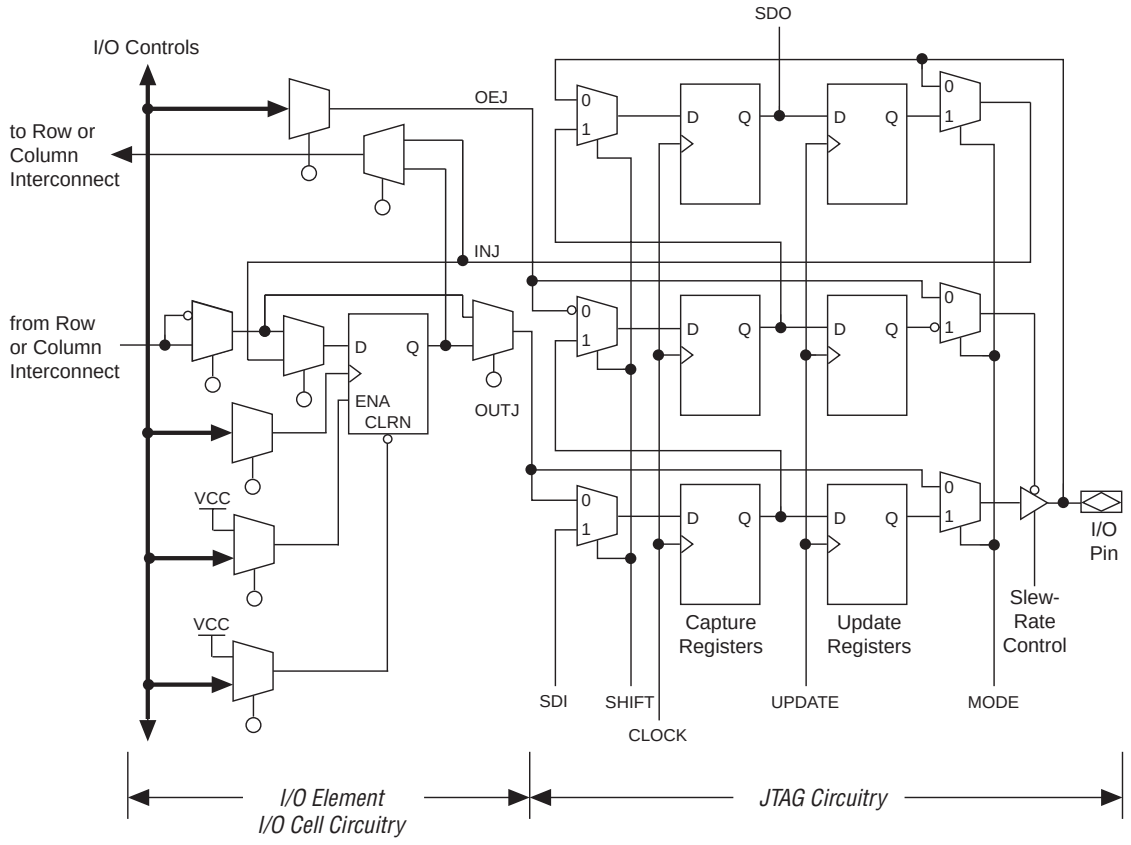


Figure 6 shows the BSCs that are associated with each I/O pin in FLEX 6000 devices.

Figure 6. FLEX 6000 I/O Pins with IEEE Std. 1149.1 BST Circuitry

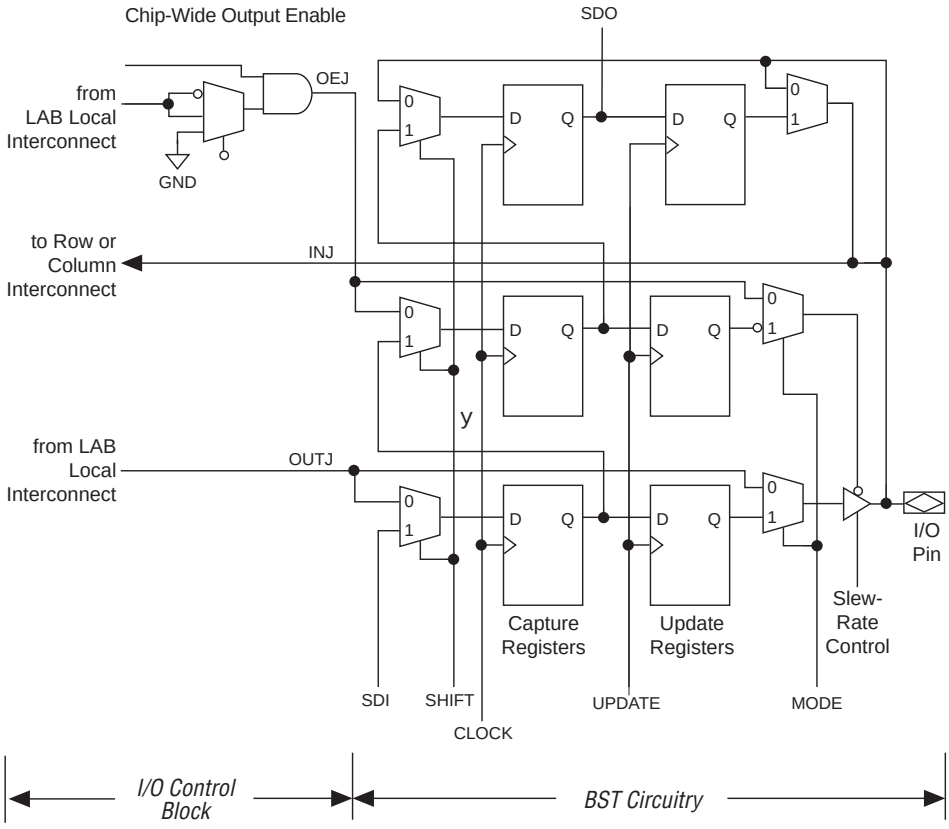
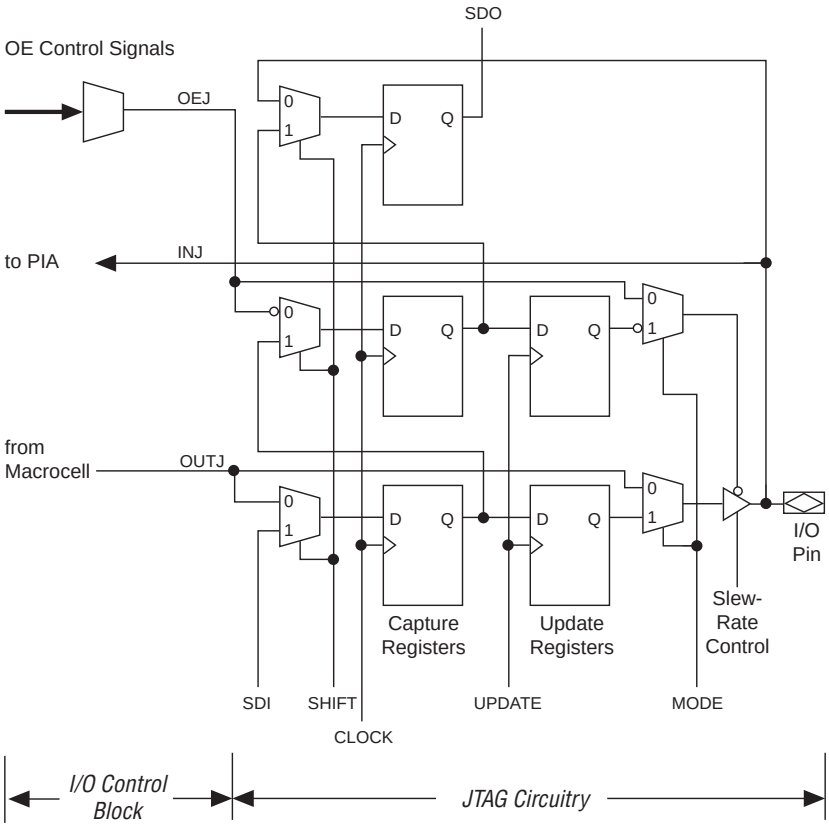


Figure 7 shows the BSCs that are associated with each I/O pin in MAX 7000S, MAX 7000A, MAX 7000B, and MAX 3000A devices. The BSCs in Figure 7 are similar to BSCs in other device families, except the input portion does not contain an update register.

Figure 7. MAX 7000S, MAX 7000A, MAX 7000B & MAX 3000A I/O Pins with IEEE Std. 1149.1 BST Circuitry



Dedicated Input

The boundary-scan register also includes dedicated input pins. Because these pins have special functions, some bits of the boundary-scan register are internally connected to V_{CC} or ground, or are used only for device configuration; these bits are either forced to a static high (1) or low (0) state, or used internally for configuration.

Figure 8 shows the BSCs for the dedicated input pins in APEX, ACEX, and FLEX devices. The register normally associated with an output signal, `OUTJ`, is tied to ground, and the tri-state control, `OEJ`, is connected to V_{CC}. The signal data from the dedicated input is the only register that contains test data. The data shifts out of `SDO` in the order `D`, `1`, and `0`, where `D` is the data associated with the dedicated input. Because only the `D` bit has valid data, a scan test pattern must either ignore or expect the `1` and `0` that follow the `D` bit.

Figure 8. APEX, ACEX & FLEX Dedicated Input Pins with IEEE Std. 1149.1 BST Circuitry

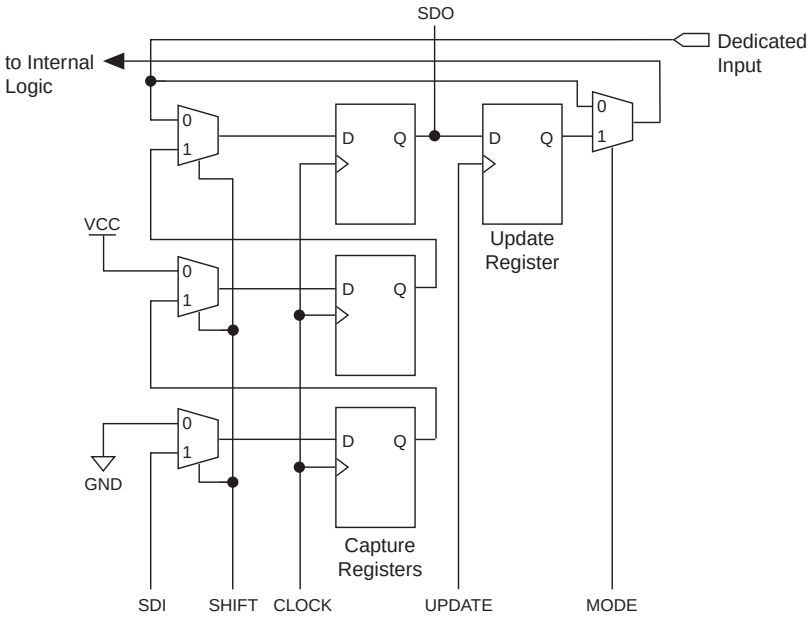
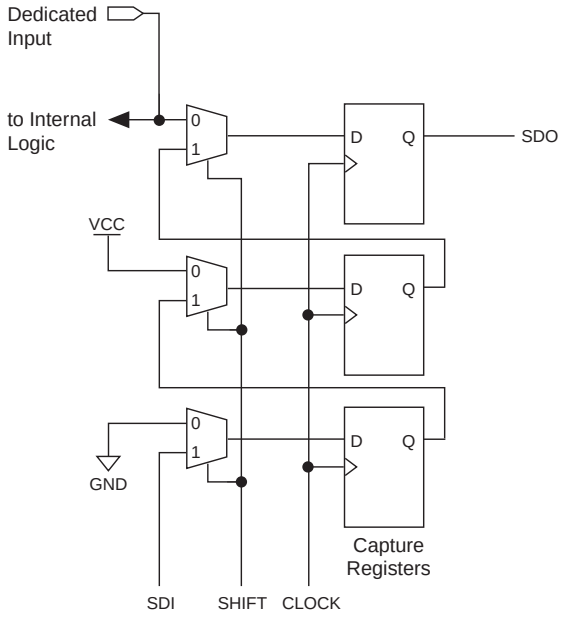


Figure 9 shows the BSCs for the dedicated input pin in MAX devices. All of the update registers in the BSCs are disabled, and the registers normally associated with the output signals `OUTJ` and `OEJ` are connected to ground and V_{CC}, respectively. When shifting data in and out of the BSCs, `OUTJ` and `OEJ` should be ignored.

Figure 9. MAX Dedicated Input Pins with IEEE Std. 1149.1 BST Circuitry

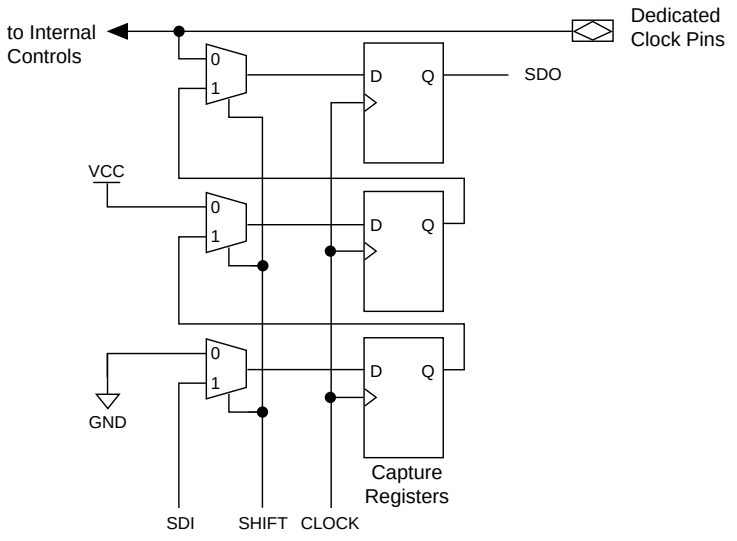


Dedicated Clock Pins (APEX 20K, ACEX 1K & FLEX 10K)

The boundary-scan register also includes dedicated clock pins. Because these pins have special functions, some bits of the boundary-scan register are internally connected to V_{CC} or ground before configuration; these bits are thus forced to a static high (1) or low (0) state.

Figure 10 shows the BSCs for the dedicated clock pins in APEX 20K, ACEX 1K, and FLEX 10K devices. These pins continue to clock internal user registers, but the capture register associated with the pin can be used for external pin connectivity tests. The pin can receive data but cannot force data onto external connections. The data values associated with the other two capture registers should be ignored.

Figure 10. APEX, ACEX & FLEX Dedicated Clock Pins with IEEE Std. 1149.1 BST Circuitry

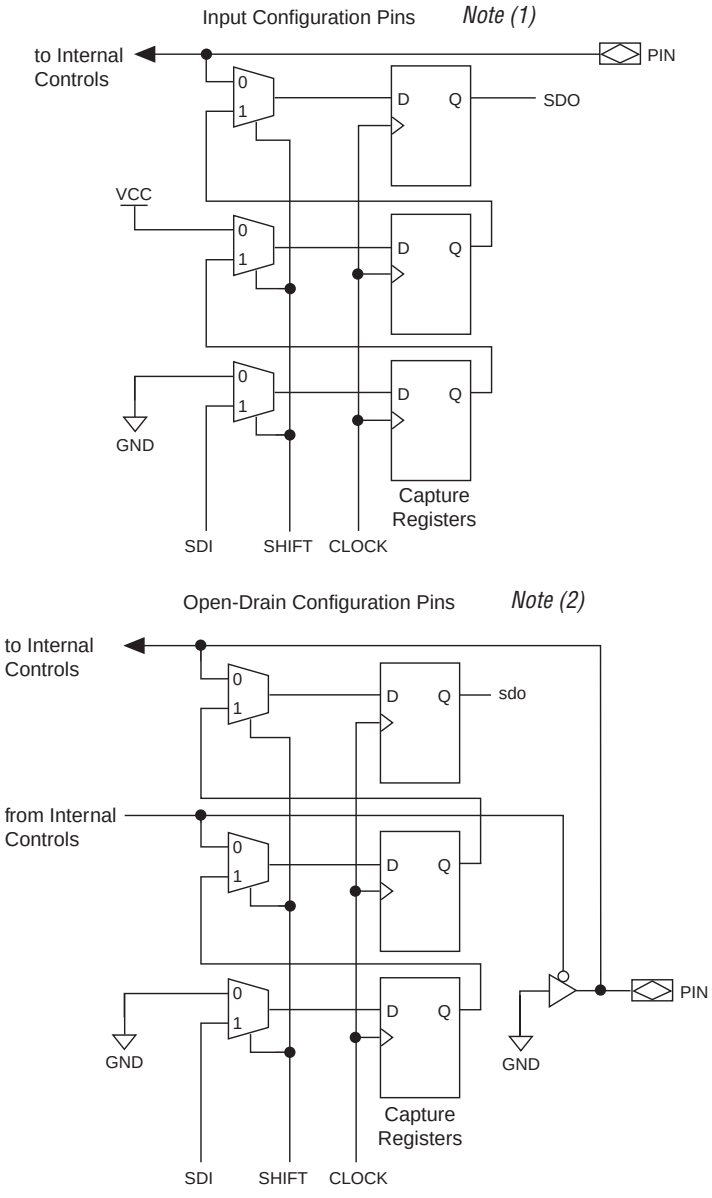


Dedicated Configuration (All APEX, ACEX & FLEX Devices)

The APEX 20K, ACEX 1K, and FLEX boundary-scan register includes dedicated configuration pins. Because these pins have special functions, some bits of the boundary-scan register are internally connected to V_{CC} or ground, or are used only for device configuration; these bits are either forced to a static high (1) or low (0) state, or used internally for configuration.

Figure 11 shows the peripheral elements associated with the APEX, ACEX, and FLEX dedicated configuration pins (i.e., `nCONFIG`, `MSEL0`, `MSEL1`, `nSP`, `CONF_DONE`, `nSTATUS`, and `DCLK`). These pins are used only during device configuration, but the capture register associated with the pin can be used for external pin connectivity tests. The pin can receive data but cannot force data onto external connections. The data values associated with the other two capture registers should be ignored.

Figure 11. APEX, ACEX & FLEX Dedicated Configuration Pins with IEEE Std. 1149.1 BST Circuitry (Part 1 of 2)

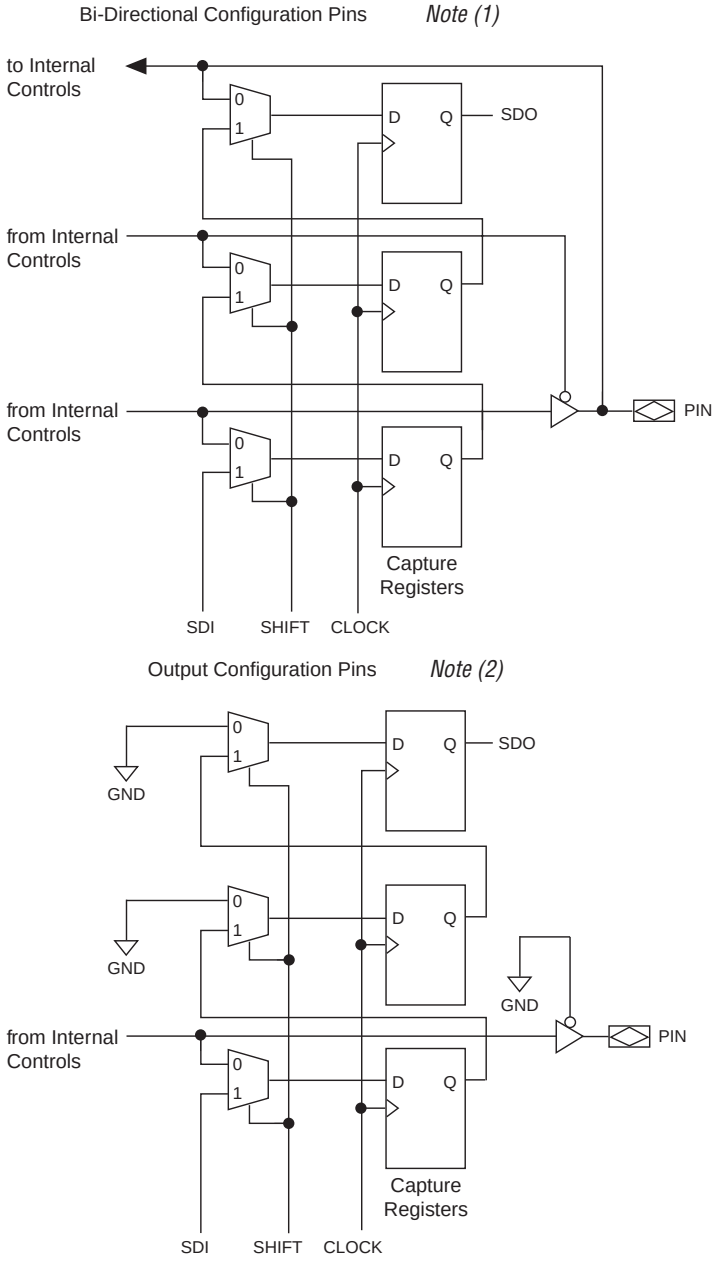


Notes:

(1) For APEX, ACEX, and FLEX 10K devices, these pins include `nCONFIG`, `MSEL0`, `MSEL1`, `nCE`, and `DCLK`; for FLEX 8000 devices, these pins include `nCONFIG`, `nSP`, `MSEL0`, and `MSEL1`, and for FLEX 6000 devices, these pins include `nCONFIG`, `MSEL`, `nCE`, and `DCLK`.

(2) These pins include `CONF_DONE` and `nSTATUS`.

Figure 11. APEX, ACEX & FLEX Dedicated Configuration Pins with IEEE Std. 1149.1 BST Circuitry (Part 2 of 2)



Notes:

(1) For FLEX 8000 devices, these pins include DCLK and DATA.

(2) For APEX 20K, ACEX 1K, FLEX 10K, and FLEX 6000 devices, these pins include nCEO.

IEEE Std. 1149.1 Std. Operation Control

Altera IEEE Std. 1149.1 devices implement the following BST instructions: SAMPLE/PRELOAD, EXTEST, BYPASS, USERCODE, and IDCODE. Table 3 summarizes the BST instructions, which are described in detail later in this application note.

Table 3. Boundary-Scan Instructions

Mode	Instruction Code				Description
	FLEX 10K APEX 20K ACEX 1K	FLEX 8000 FLEX 6000	MAX 9000 MAX 9000A	MAX 7000S MAX 7000A MAX 7000B MAX 3000A	
SAMPLE/ PRELOAD	0001010101	101	0001010101	0001010101 *(1)*	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	0000000000	000	0000000000	000000000 *(1)*	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	1111111111	111	1111111111	1111111111 *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.
IDCODE	0000000110	–	0001011001 *(3)*	0001011001	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
USERCODE	0000000111	–	–	0000000111 *(2)*	Selects the USERCODE register and places it between TDI and TDO, allowing the USERCODE to be serially shifted out of TDO.

Notes to table:

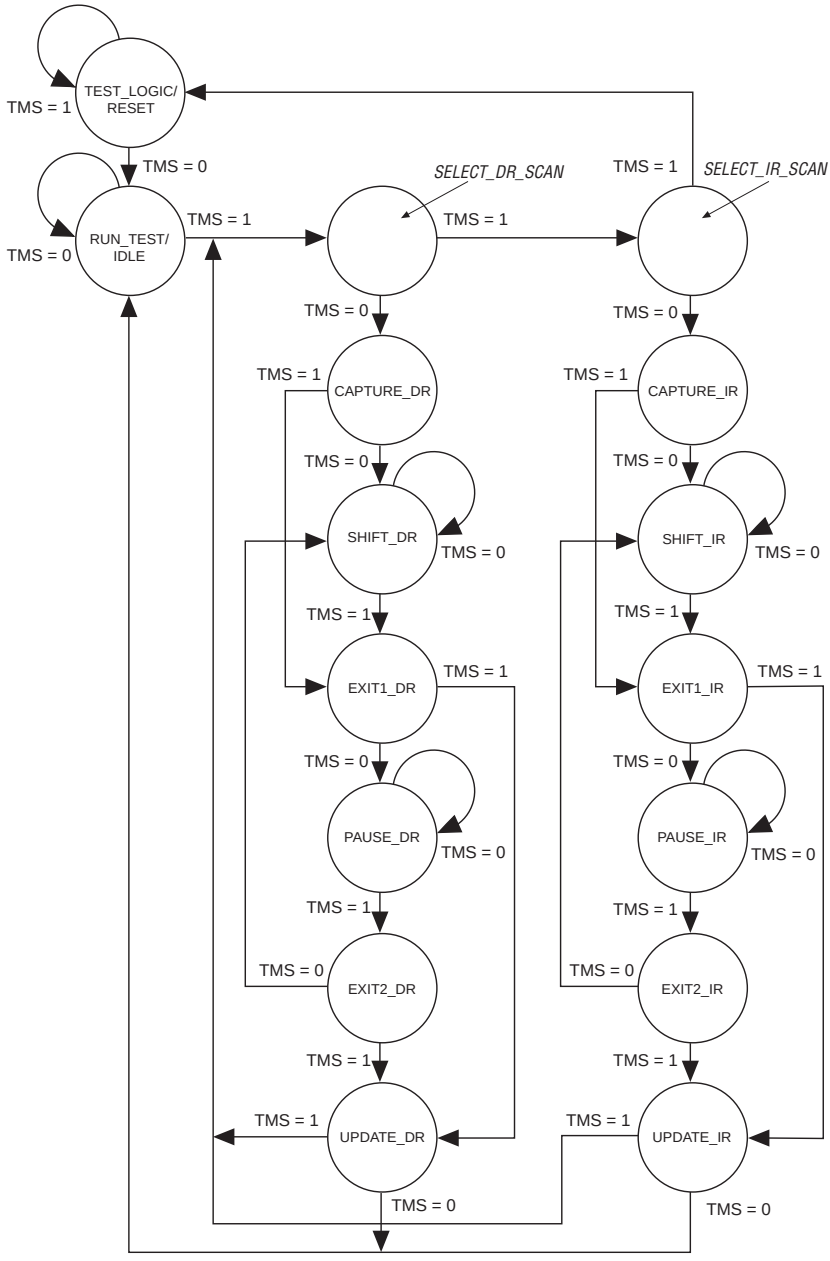
(1) EPM7032S, EPM7064S, and EPM7096S devices do not support IEEE Std. 1149.1 BST. However, these devices have a BYPASS mode that allows them to pass IEEE Std. 1149.1 information to other devices in the scan chain that supports IEEE Std. 1149.1 BST.

(2) MAX 7000S devices do not support the optional USERCODE instruction. However, the MAX 7000S devices offer a 16-bit UESCODE register that serves the same purpose.

(3) IDCODE is available in all MAX 9000 (including MAX 9000A) devices except in early versions of the EPM9320 and EPM9560 devices.

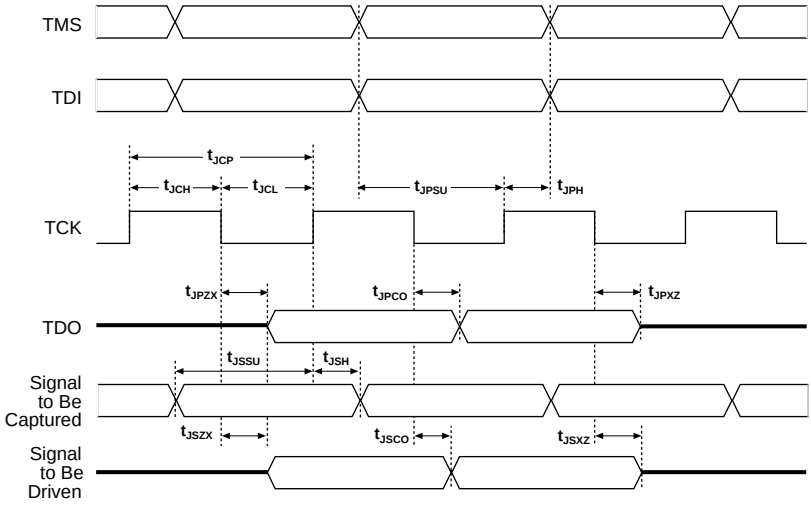
The IEEE Std. 1149.1 test access port (TAP) controller, a 16-state state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE Std. 1149.1 operation in the device. Figure 12 shows the TAP controller state machine.

Figure 12. IEEE Std. 1149.1 TAP Controller State Machine



When the TAP controller is in the TEST_LOGIC/RESET state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized. If the device supports IDCODE, this initial instruction is IDCODE; otherwise, it is BYPASS. At device power-up, the TAP controller starts in this TEST_LOGIC/RESET state. In addition, the TAP controller may be forced to the TEST_LOGIC/RESET state by holding TMS high for five TCK clock cycles or by holding the TRST pin low (if the optional TRST pin is supported.) Once in the TEST_LOGIC/RESET state, the TAP controller remains in this state as long as TMS continues to be held high while TCK is clocked or TRST continues to be held low. Figure 13 shows the timing requirements for the IEEE Std. 1149.1 signals.

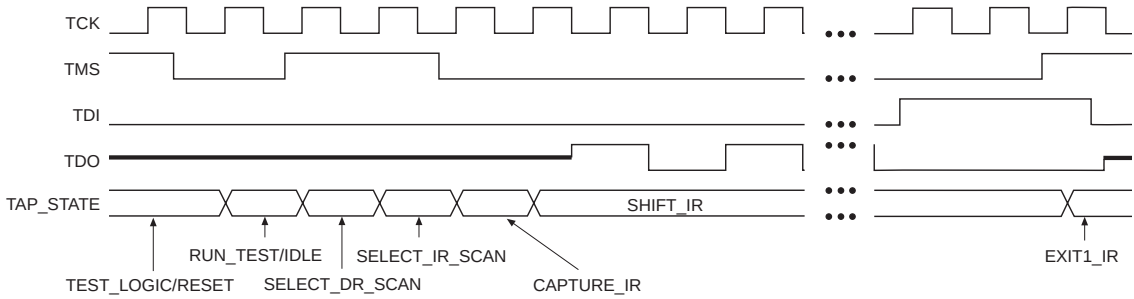
Figure 13. IEEE Std. 1149.1 Timing Waveforms



The timing values for each Altera device are provided in the appropriate device family data sheet.

To start IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (SHIFT_IR) state and shift in the appropriate instruction code on the TDI pin. The waveform diagram in Figure 14 represents the entry of the instruction code into the instruction register. It shows the values of TCK, TMS, TDI, and TDO and the states of the TAP controller. From the RESET state, TMS is clocked with the pattern 01100 to advance the TAP controller to SHIFT_IR.

Figure 14. Selecting the Instruction Mode



The TDO pin is tri-stated in all states except in the SHIFT_IR and SHIFT_DR states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

When the SHIFT_IR state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the SHIFT_IR state is active. The TAP controller remains in the SHIFT_IR state as long as TMS remains low.

During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the opcode must be clocked at the same time that the next state, EXIT1_IR, is activated; EXIT1_IR is entered by clocking a logic high on TMS. Once in the EXIT1_IR state, TDO becomes tri-stated again. TDO is always tri-stated except in the SHIFT_IR and SHIFT_DR states. After an instruction code is entered correctly, the TAP controller advances to perform the serial shifting of test data in one of three modes—SAMPLE/PRELOAD, EXTEST, or BYPASS—that are described below.

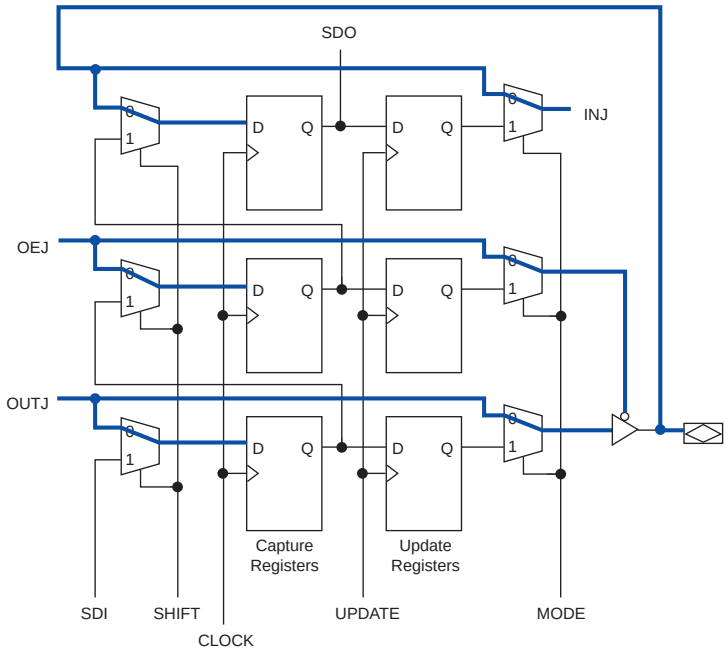
SAMPLE/PRELOAD Instruction Mode

The SAMPLE/PRELOAD instruction mode allows you to take a snapshot of device data without interrupting normal device operation. Figure 15 shows the capture, shift, and update phases of the SAMPLE/PRELOAD mode.

Figure 15. IEEE Std. 1149.1 BST SAMPLE/PRELOAD Mode

Capture Phase

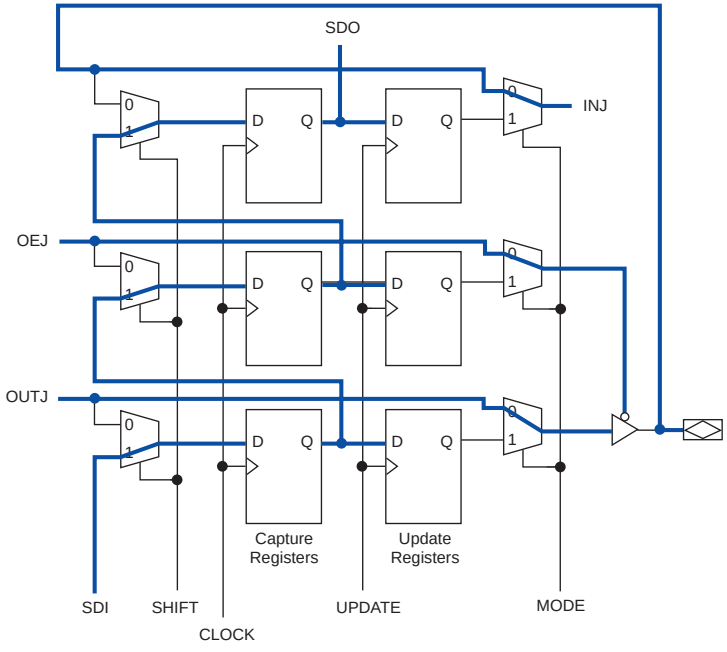
In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The register CLOCK signal is supplied by the TAP Controller's CLOCKDR output. The data retained in these registers consists of signals from normal device operation.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

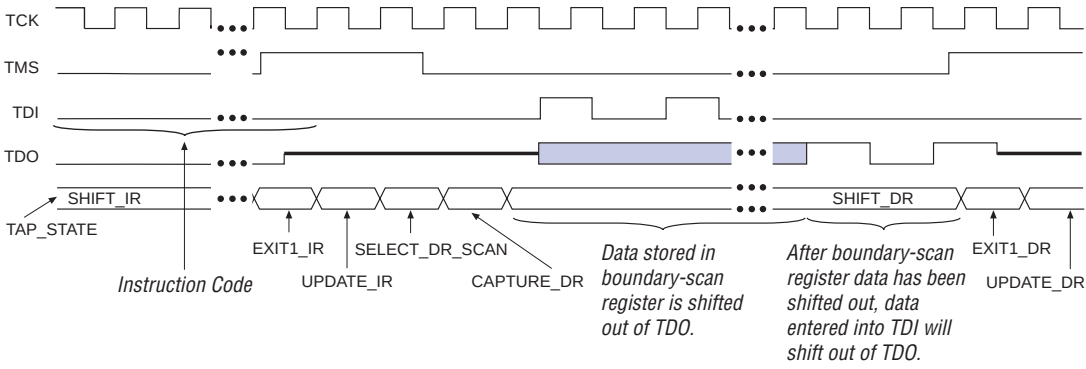
In the update phase, data is transferred from the capture registers to the UPDATE registers using the UPDATE Clock. The data stored in the UPDATE registers can be used for the EXTEST instruction.



During the capture phase, multiplexers preceding the capture registers select the active device data signals; this data is then clocked into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device. During the shift phase, the boundary-scan shift register is formed by clocking data through capture registers around the device periphery and then out of the TDO pin. New test data can simultaneously be shifted into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers. This data can then be used in the EXTEST instruction mode. Refer to "EXTEST Instruction Mode" on page 21 for more information.

Figure 16 shows the SAMPLE/PRELOAD waveforms. The SAMPLE/PRELOAD instruction code is shifted in through the TDI pin. The TAP controller advances to the CAPTURE_DR state and then to the SHIFT_DR state, where it remains if TMS is held low. The data shifted out of the TDO pin consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register. Figure 16 shows that the instruction code at TDI does not appear at the TDO pin until after the capture register data is shifted out. If TMS is held high on two consecutive TCK clock cycles, the TAP controller advances to the UPDATE_DR state for the update phase.

Figure 16. SAMPLE/PRELOAD Shift Data Register Waveforms



EXTEST Instruction Mode

The EXTEST instruction mode is used primarily to check external pin connections between devices. Unlike the SAMPLE/PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, opens and shorts can be detected at pins of any device in the scan chain.

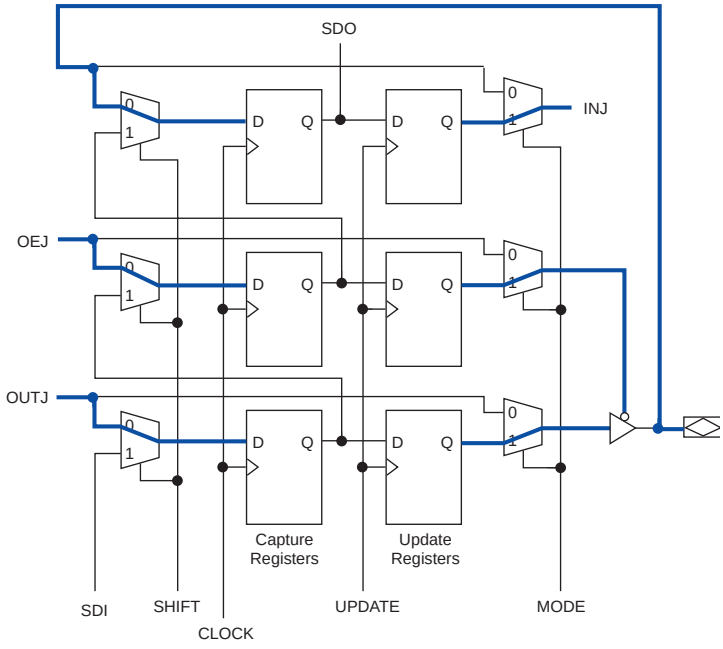
Figure 17 shows the capture, shift, and update phases of the EXTEST mode.

Figure 17. IEEE Std. 1149.1 BST EXTEST Mode

Capture Phase

In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The register CLOCK signal is supplied by the TAP Controller's CLOCKDR output. Previously retained data in the update registers drives the IOC input, INJ, and allows the I/O pin to tri-state or drive a signal out.

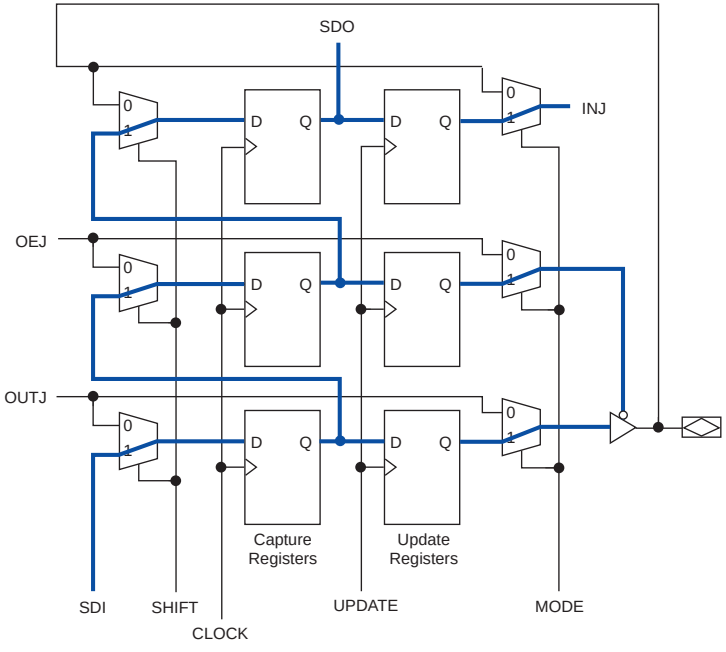
A "1" in the OEJ update register tri-states the output buffer.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

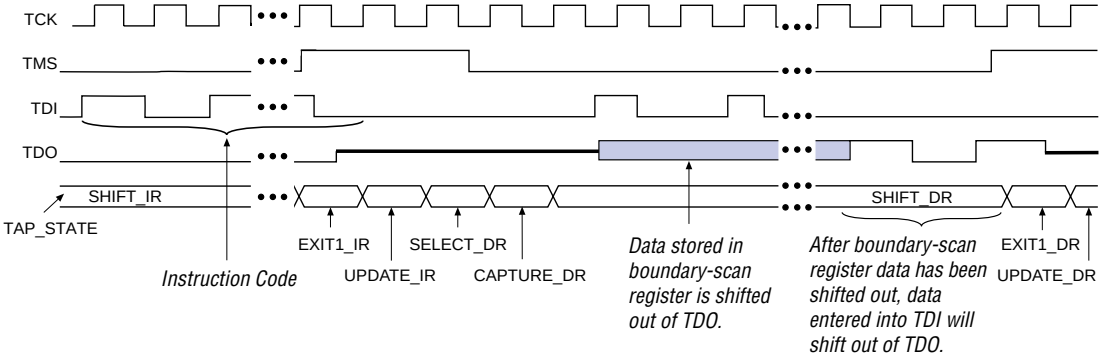
In the update phase, data is transferred from the capture registers to the update registers using the UPDATE Clock. The update registers then drive the IOC input, INJ, and allow the I/O pin to tri-state or drive a signal out.



EXTEST selects data differently than SAMPLE/PRELOAD. EXTEST chooses data from the update registers as the source of the INJ, output, and output enable signals. Once the EXTEST instruction code is entered, the multiplexers select the update register data; thus, data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers and then shifted out of TDO during the shift phase. New test data can then be stored in the update registers during the update phase.

The waveform diagram in Figure 18 resembles the SAMPLE/PRELOAD waveform diagram, except that the instruction code for EXTEST uses all zeros. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

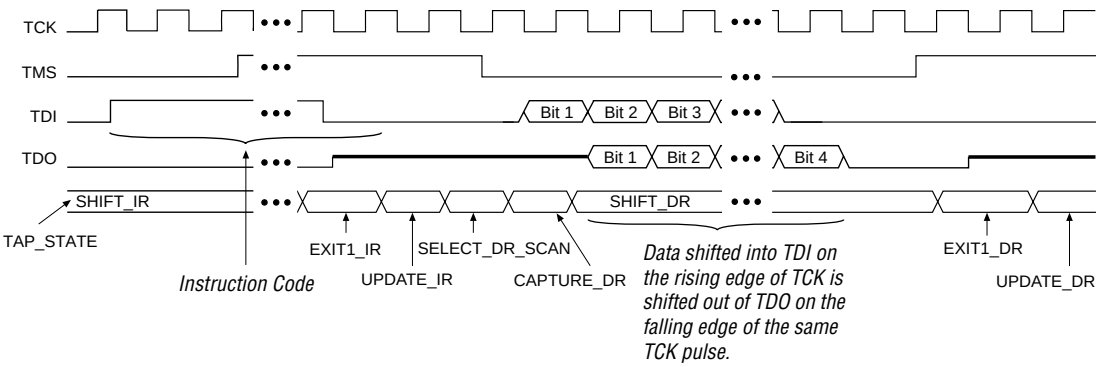
Figure 18. EXTEST Shift Data Register Waveforms



BYPASS Instruction Mode

The BYPASS instruction mode is activated with an instruction code made up of only ones. The waveforms in Figure 19 show how scan data passes through a device once the TAP controller is in the SHIFT_DR state. In this state, data signals are clocked into the bypass register from TDI on the rising edge of TCK and out of TDO on the falling edge of the same clock pulse.

Figure 19. BYPASS Shift Data Register Waveforms



IDCODE Instruction Mode

The IDCODE instruction mode is used to identify the devices in an IEEE Std. 1149.1 chain. When IDCODE is selected, the device identification register is loaded with the 32-bit vendor-defined identification code and connected between the TDI and TDO ports. The 32-bit vendor-defined identification register for Altera devices is listed in the appropriate device family data sheet.

USERCODE Instruction Mode

The USERCODE instruction mode is used to examine the user electronic signature (UES) within the devices along an IEEE Std. 1149.1 chain. When this instruction is selected, the device identification register is connected between the TDI and TDO ports and the user-defined UES is shifted out through the device ID register.

MAX 7000S devices offer an alternative method of providing the ability to read out user-defined 16-bit UES.

Enabling IEEE Std. 1149.1 BST Circuitry

The IEEE Std. 1149.1 BST circuitry for Altera devices is enabled upon device power-up. Because this circuitry may be used for BST, ISP, or ICR (depending in the device), this circuitry must be enabled only at specific times. This section describes how to enable the IEEE Std. 1149.1 circuitry when needed and to ensure that the circuitry is not inadvertently enabled when it is not needed.

APEX 20K, ACEX 1K, FLEX 10K & MAX 9000 Devices

The IEEE Std. 1149.1 BST circuitry for Altera devices is enabled upon device power-up. You can use the IEEE Std. 1149.1 BST circuitry both before and after device programming or configuration. However, in APEX 20K, ACEX 1K, and FLEX 10K devices, the nCONFIG pin must be held low when you perform JTAG boundary-scan testing before configuration.

Because these devices have dedicated IEEE Std. 1149.1 pins, their BST circuitry is always enabled. To disable the JTAG circuitry in these devices, tie these pins to the values shown in Table 4.

Table 4. Disabling IEEE Std. 1149.1 Circuitry

Devices	Compiler Option	JTAG Pins *(1)*				
		TMS	TCK	TDI	TDO	TRST
APEX 20K, APEX 20KE	–	VCC	GND *(2)*	VCC	Leave open	GND
ACEX 1K	–	VCC	GND *(2)*	VCC	Leave open	GND
FLEX 10K, FLEX 10KE	–	VCC	GND *(2)*	VCC	Leave open	GND
FLEX 8000	JTAG Disabled	User I/O *(3)*	User I/O *(3)*	User I/O *(3)*	User I/O	GND *(3)*
	JTAG Enabled	VCC	GND *(2)*	VCC	Leave open	GND
FLEX 6000	JTAG Disabled	User I/O	User I/O	User I/O	User I/O	–
	JTAG Enabled	VCC	GND *(2)*	VCC	Leave open	–
MAX 9000	–	VCC	GND *(2)*	VCC	Leave open	–
MAX 7000S, MAX 7000A, MAX 7000B, MAX 3000A	JTAG Disabled	User I/O	User I/O	User I/O	User I/O	–
	JTAG Enabled	VCC	GND *(2)*	VCC	Leave open	–

Notes:

(1) If the design has been compiled with IEEE Std. 1149.1 circuitry enabled, tying the IEEE Std. 1149.1 pins to the appropriate state will deactivate the IEEE Std. 1149.1 circuitry.

(2) The TCK signal may also be tied high. If TCK is tied high, power-up conditions must ensure that TMS is pulled high before TCK. Pulling TCK low avoids this power-up condition.

(3) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, TMS, TCK, TDI, and TRST should be tied to GND.

FLEX 8000 & FLEX 6000 Devices

The IEEE Std. 1149.1 BST circuitry for Altera devices is enabled upon device power-up. You can use the IEEE Std. 1149.1 BST circuitry both before and after device programming or configuration. In FLEX 8000 and FLEX 6000 devices, the `nCONFIG` pin must be held low when you perform boundary-scan testing before configuration.

Because these devices have four pins that can be used as either JTAG pins or user I/O pins, you must enable or disable the JTAG circuitry before compilation. For a design that has been compiled with JTAG pins enabled, the four pins operate as dedicated pins only. If these devices are not using the IEEE Std. 1149.1 circuitry, tying the pins to the appropriate state (shown in Table 4) disables the circuitry.

By choosing **Device Options** from the **Device** dialog box (Assign menu), you can enable or disable IEEE Std. 1149.1 support for applicable devices on a device-by-device basis with the *Enable JTAG Support* option. You can also enable JTAG support for all devices in a project by choosing **Global Project Device Options** (Assign menu) and selecting the *Enable JTAG Support* option.

MAX 7000S, MAX 7000A, MAX 7000B & MAX 3000A Devices

The IEEE Std. 1149.1 BST circuitry of MAX 7000S, MAX 7000A, MAX 7000B, and MAX 3000A devices is enabled by an IEEE Std. 1149.1 enable bit within the device. A blank device will always have the BST circuitry enabled. The state of this enable bit may be set only by programming in the Altera MPU or third-party programmer. The state of the JTAG enable bit may not be changed using ISP via the IEEE Std. 1149.1 port.

Because these devices have four pins that can be used as either JTAG pins or user I/O pins, you must enable or disable the JTAG circuitry before compilation. For a design that has been compiled with JTAG pins enabled, the four pins operate as dedicated pins only. If these devices are not using the IEEE Std. 1149.1 circuitry, tying the pins to the appropriate state (shown in Table 4) disables the circuitry.

By choosing **Device Options** from the **Device** dialog box (Assign menu), you can enable or disable IEEE Std. 1149.1 support for applicable devices on a device-by-device basis with the *Enable JTAG Support* option. You can also enable JTAG support for all devices in a project by choosing **Global Project Device Options** (Assign menu) and selecting the *Enable JTAG Support* option.

Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing

Use the following guidelines when performing boundary-scan testing with IEEE Std. 1149.1 devices:

- If the "10..." pattern does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the proper TAP controller state has not been reached. To solve this problem, try one of the following procedures:
  - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and clock the code 01100 on the TMS pin.
  - Check the connections to the VCC, GND, JTAG, and dedicated configuration pins on the device.
  - For all FLEX, MAX 7000S, MAX 7000A, MAX 7000B, and MAX 3000A devices, if the device is in user mode, make sure that you have turned on the *Enable JTAG Support* option in the MAX+PLUS II software.
- Perform a SAMPLE/PRELOAD test cycle prior to the first EXTEST test cycle to ensure that known data is present at the device pins when the EXTEST mode is entered. If the OEJ update register contains a 0, the data in the OUTJ update register will be driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST and SAMPLE/PRELOAD tests during ISP or ICR. These instructions are supported before and after ISP/ICR but not during ISP and ICR.
- In FLEX 8000 devices, do not execute a BYPASS shift cycle before an EXTEST test cycle that requires preloaded test data. The bypass and boundary-scan registers shift simultaneously when the TAP controller is in the SHIFT_DR state. Therefore, using the BYPASS mode will shift test data out of the capture registers.

If problems persist, contact Altera Applications at (800) 800-EPLD.

Boundary-Scan Description Language (BSDL) Support

The Boundary-Scan Description Language (BSDL)—a subset of VHDL—provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested. Test software development systems then use the BSDL files for test generation, analysis, failure diagnostics, and in-system programming. For more information, or to receive BSDL files for IEEE Std. 1149.1-compliant Altera devices, visit the Altera web site at **http://www.altera.com**.

Conclusion

The IEEE Std. 1149.1 BST circuitry available in Altera devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE Std. 1149.1-compliant devices can use the EXTEST, SAMPLE/PRELOAD, and BYPASS modes to create serial patterns that internally test the pin connections between devices and check device operation.

References

Bleeker, H., P. van den Eijnden, and F. de Jong. ***Boundary-Scan Test: A Practical Approach***. Eindhoven, The Netherlands: Kluwer Academic Publishers, 1993.

Institute of Electrical and Electronic Engineers, Inc. ***IEEE Standard Test Access Port and Boundary-Scan Architecture*** (IEEE Std 1149.1-1990). New York: Institute of Electrical and Electronic Engineers, Inc., 1990.

Maunder, C. M., and R. E. Tulloss. ***The Test Access Port and Boundary-Scan Architecture***. Los Alamitos: IEEE Computer Society Press, 1990.

Revision History

The information contained in *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* version 4.05 supersedes information published in previous versions.

Version 4.05 Changes

Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices) version 4.05 contains the following changes:

- Added APEX 20K, ACEX 1K, FLEX 10KE, MAX 7000B, and MAX 3000A information to document where relevant.
- Updated Table 1 on page 2.
- Updated Figure 2 on page 4.
- Updated *Note (2)* and *Note (3)* on page 4.
- Updated Figure 11 on page 13.
- Updated *Note (1)* and *Note (2)* on page 13.
- Updated Figure 11 on page 14.
- Updated *Note (2)* on page 14.
- Updated Table 3 on page 15.
- Updated *Note (2)* on page 16.
- Updated Table 4 on page 25.

Version 4.04 Changes

Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices) version 4.04 contains the following changes:

- Updated information on TCK and MAX 7000A devices in Table 4.

- Moved IDCODE values and information from the "Length of IEEE 1149.1 Registers" table to the device family data sheets.
- Added *Note (4)* to Figure 2.
- Made minor style changes.

Version 4.03 Changes

Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices) version 4.03 contained the following changes:

- Added *Note (3)* to Table 4 for JTAG BST in EPF81500A devices.
- Made minor style changes.

Version 4.02 Changes

Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices) version 4.02 contained the following changes:

- Corrected the boundary-scan register length for several devices in Table 3 on page 15.
- Corrected the signal polarity on I/O pins in Figures 4 and 5.
- Updated information on how to disable the JTAG circuitry in Table 4 on page 25.
- Made minor textual and style changes.

Version 4.01 Changes

Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices) version 4.01 contained the following changes:

- Corrected the boundary-scan register length for EPM7192S devices in Table 3 on page 15.
- Updated Figure 13 for accuracy.

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