Using Selectable I/O Standards

in Altera Devices

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Introduction

High-performance, low-voltage I/O standards have been introduced to keep pace with increasing clock speeds, higher data rates, and new low-voltage devices. These I/O standards are used to interface with memory, microprocessors, backplanes, and peripheral devices. Designers who want to use these new standards with programmable logic need flexible, high-performance, multi-standard I/O buffers. Altera's revolutionary APEX™ 20KE devices offer the highest density, highest performance programmable logic solution with the necessary I/O standards for the communication and computer industries.

Altera® MAX® 7000B devices are the product-term leader in I/O standard support: MAX 7000B devices are the only macrocell-based devices to support Gunning transceiver logic plus (GTL+), stub series terminated logic for 2.5 V (SSTL-2), and 3.3-V SSTL-3.

With the new programmable I/O standards supported by APEX 20KE and MAX 7000B devices, a single device can simultaneously support multiple I/O standards, as well as interface with high-speed, low-voltage memory buses and backplanes. These I/O standards include low-voltage differential signaling (LVDS), which supports data rates up to 622.08 million bits per second (Mbps). Programmable I/O standards simplify board design. Dedicated circuitry like LVDS is integrated into programmable logic devices (PLDs), saving board space, reducing pin usage, and improving performance.

This application note provides guidelines for designing with selectable I/O standards in Altera devices and covers the following topics:

- Overview of I/O Standards & Applications
- APEX 20KE & MAX 7000B I/O Standards
- Operating Conditions
- Using LVDS
- Board Termination Schemes

Overview of I/O Standards & Applications

The ability for PLDs to support industry I/O standards gives customers a quick time-to-market design solution. This section provides an overview of typical applications for the selectable I/O standards supported by Altera devices. The specifications for each I/O standard are listed in this section.

LVTTL

The low-voltage transistor-transistor logic (LVTTL) standard is a single-ended, general-purpose standard for 3.3-V applications. The LVTTL interface is defined by JEDEC Standard JESD 8-A, *Interface Standard for Nominal 3.0 V/3.3 V Supply Digital Integrated Circuits*. The maximum recommended input voltage for APEX and MAX 7000B devices is 4.1 V, which exceeds the 3.9-V requirement of this specification. The LVTTL output buffer is a push-pull driver. This standard requires the output buffer to drive to 2.4 V (minimum V_{OH} = 2.4 V). It does not require the use of input reference voltages or termination. APEX and MAX 7000B devices are compliant with this standard.

LVCMOS

The low-voltage CMOS (LVCMOS) standard is defined in JEDEC Standard JESD 8-A, *Interface Standard for Nominal 3.0 V/3.3 V Supply Digital Integrated Circuits*. LVCMOS is a single-ended general-purpose standard also used for 3.3-V applications. The input buffer requirements are the same as the LVTTL requirements, and the output buffer is required to drive to the rail (minimum $V_{OH} = V_{CCIO} - 0.2$ V). APEX and MAX 7000B devices are fully compliant with the LVCMOS standard. This standard requires a 3.3-V I/O supply voltage (V_{CCIO}), but not the use of input reference voltages or termination.

2.5 V

The 2.5-V I/O standard is documented by JEDEC Standard JESD 8-5, *2.5 V ±0.2 V (Normal Range) and 1.7 V to 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit*. This standard is similar to LVCMOS but is used for 2.5-V power supply levels. APEX and MAX 7000B devices are compliant with this standard, which requires a 2.5-V V_{CCIO}, but not the use of input reference voltages or termination.

1.8 V

The 1.8-V I/O standard is documented by JEDEC Standard JESD 8-7, *1.8 V ±0.15 V (Normal Range) and 1.2 V to 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit*. This standard is similar to LVCMOS but is used for 1.8-V power supply levels and reduced input and output thresholds. APEX and MAX 7000B devices are compliant with this standard, which requires a 1.8-V V_{CCIO}, but not the use of input reference voltages or termination.

3.3-V PCI

APEX devices are compliant with ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation. MAX 7000B devices are compliant with all aspects of this standard except that they do not offer clamps to V_{CCIO}. At 3.3 V, the PCI standard supports up to 64-bit bus width operation at 33 or 66 MHz. This standard uses LVTTL-type input and output buffers and requires a 3.3-V V_{CCIO}, but not the use of input reference voltages or termination.

LVDS

The LVDS I/O standard is used for very high-performance, low-power-consumption data transfer. Two key industry standards define LVDS: IEEE 1596.3 SCI-LVDS and ANSI/TIA/EIA-644. Both standards have similar key features, but the IEEE standard supports a maximum data transfer of 250 Mbps. APEX 20KE devices are designed to meet the ANSI/TIA/EIA-644 requirements at up to 622 Mbps. The LVDS standard requires a 3.3-V V_{CCIO} and a 100-Ω termination resistor between the two traces at the input buffer. No input reference voltage is required. For more information on LVDS, see "Using LVDS" on page 12 or the Altera web site (**http://www.altera.com**).

GTL+

The GTL+ standard is a high-speed bus standard first used by Intel Corporation for interfacing with the Pentium Pro processor. GTL+ is a voltage-referenced standard requiring a 1.0-V input reference voltage (V_{REF}) and board termination voltage (V_{TT}) of 1.5 V. Because GTL+ is an open-drain standard, it does not require a particular V_{CCIO} supply voltage. APEX 20KE and MAX 7000B devices are compliant with this standard. GTL+ is often used for processor interfacing or communication across a backplane.

SSTL-2 Class I & II

The SSTL-2 standard, specified by JEDEC Standard JESD 8-9, *Stub-Series Terminated Logic for 2.5 Volts (SSTL-2)*, is a voltage-referenced standard requiring a 1.125-V V_{REF}, a 2.5-V V_{CCIO}, and a 1.125-V V_{TT}. APEX 20KE and MAX 7000B devices are compliant with this standard. SSTL-2 is used for high-speed SDRAM interfaces.

SSTL-3 Class I & II

The SSTL-3 standard, specified by JEDEC Standard JESD 8-8, *Stub-Series Terminated Logic for 3.3 Volts (SSTL-3)*, is a voltage-referenced standard requiring a 1.5-V V_{REF}, a 3.3-V V_{CCIO}, and a 1.5-V V_{TT}. APEX 20KE and MAX 7000B devices are compliant with this standard. SSTL-3 is used for high-speed SDRAM interfaces.

AGP

The advanced graphics port (AGP) standard is specified by the *Advanced Graphics Port Interface Specification Revision 2.0* introduced by Intel Corporation for graphics applications. AGP is a voltage referenced standard requiring a 1.32-V V_{REF}, a 3.3-V V_{CCIO}, and does not require termination. APEX 20KE devices support the AGP interface.

CTT

The center-tap-terminated (CTT) standard is specified by JEDEC Standard JESD 8-4, *Center-Tap-Terminated (CTT) Low-Level, High-Speed Interface Standard for Digital Integrated Circuits*. CTT is a voltage referenced standard requiring a 1.5-V V_{REF}, a 3.3-V V_{CCIO}, and a 1.5-V V_{TT}. The CTT standard is a superset of LVTTL and LVCMOS. CTT receivers are compatible with LVCMOS and LVTTL standards. CTT drivers, when unterminated, are compatible with the AC and DC specifications for LVCMOS and LVTTL.

Software Support

Selectable I/O standards are programmable on a per I/O block basis for both APEX 20KE and MAX 7000B devices. APEX 20KE devices have a total of 10 I/O blocks including two LVDS blocks. The LVDS I/O blocks can also be used for any of the other I/O standards when not used for LVDS. MAX 7000B devices have two I/O blocks; I/O standards supported by MAX 7000B devices are shown in Table 1 on page 5. The Quartus™ and MAX+PLUS® II software tools define the I/O standard used for each I/O block.

Software support for the selectable I/O standards is provided in the Quartus and MAX+PLUS II software. The Quartus software versions 1999.10 and higher supports selectable I/O standards in APEX 20KE devices, and the MAX+PLUS II software versions 9.4 and higher supports the new I/O standards for MAX 7000B devices. For information on how the Quartus and MAX+PLUS II software tools will support these I/O standards, contact Altera Applications.

APEX 20KE & MAX 7000B I/O Standards

The APEX 20KE I/O blocks support 13 I/O standards and are the only PLDs in the industry with LVDS. The MAX 7000B family support for GTL+, SSTL-2, and SSTL-3 is unique among product-term-based PLDs.

The programmable input/output element (IOE) blocks in both APEX 20KE and MAX 7000B devices have individual power planes with separate I/O supply voltage (VCCIO) pins for each I/O block. The V_{CCIO} supply supports 3.3-V, 2.5-V, and 1.8-V levels.

APEX 20KE & MAX 7000B I/O Standards

The APEX 20KE and MAX 7000B I/O buffers meet the voltage, drive strength, and AC characteristics necessary to comply with the I/O standards listed in Table 1.

Table 1. APEX 20KE & MAX 7000B Supported I/O Standards

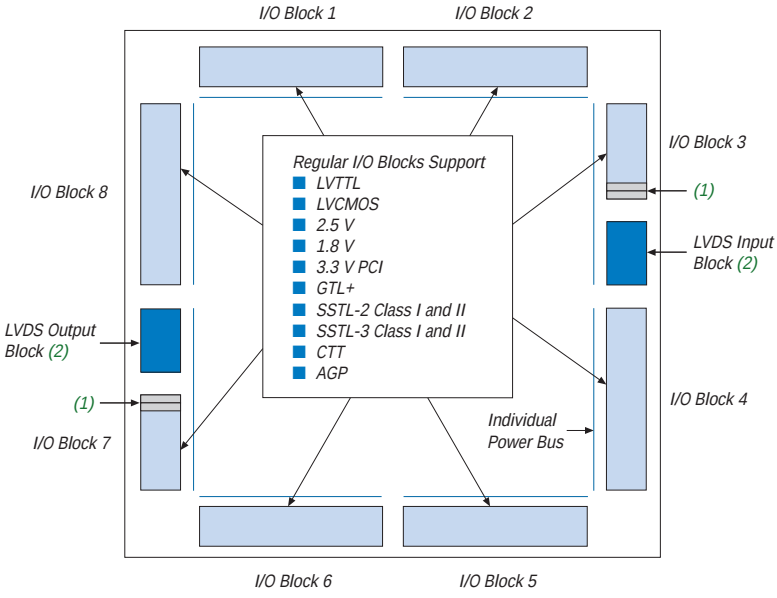
I/O Standard	Device		Type	Input Reference Voltage (V_{REF}) (V) *(1)*	Output Supply Voltage (V_{CCIO}) (V) *(1)*	Board Termination Voltage (V_{TT}) (V) *(1)*
	APEX 20KE	MAX 7000B				
LVTTL	✓	✓	Single-ended	N/A	3.3	N/A
LVCMOS	✓	✓	Single-ended	N/A	3.3	N/A
2.5 V	✓	✓	Single-ended	N/A	2.5	N/A
1.8 V	✓	✓	Single-ended	N/A	1.8	N/A
PCI	✓	✓ *(2)*	Single-ended	N/A	3.3	N/A
LVDS	✓		Differential	N/A	N/A	N/A
GTL+	✓	✓	Voltage referenced	1.0	N/A	1.5
SSTL-2 Class I and II	✓	✓	Voltage referenced	1.125	2.5	1.125
SSTL-3 Class I and II	✓	✓	Voltage referenced	1.5	3.3	1.5
AGP	✓		Voltage referenced	1.32	3.3	N/A
CTT	✓		Voltage referenced	1.5	3.3	1.5

Notes:
(1) The values shown for V_{REF}, V_{CCIO}, and V_{TT} are typical values.
(2) MAX 7000B devices do not have the PCI diode clamp to V_{CCIO}. These devices comply with all other 64-bit/66-MHz 3.3-V PCI specifications.

Each I/O standard has different V_{REF}, V_{TT}, and V_{CCIO} requirements. For more information, refer to "Board Termination Schemes" on page 16.

APEX 20KE devices in FineLine BGA™ packages have eight programmable I/O blocks and two LVDS I/O blocks. Figure 1 shows the representation of the I/O blocks. For APEX 20KE designs that do not use LVDS, the LVDS I/O blocks can be used for any other standard.

Figure 1. APEX 20KE I/O Blocks



Note:

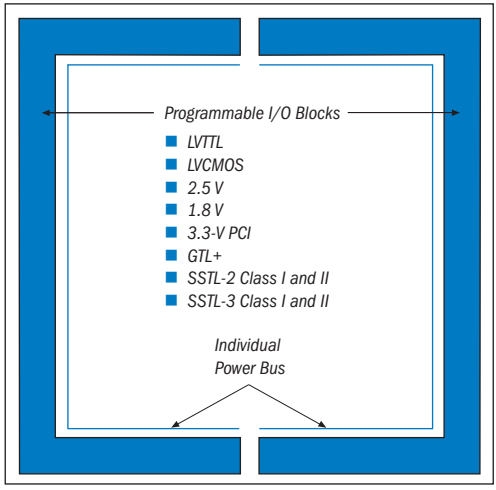
(1) The first two I/O pins that border the LVDS blocks can only be used for input to maintain an acceptable noise level on the V_{CCIO} plane.

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

MAX 7000B I/O Standards

Each MAX 7000B device has two programmable I/O blocks. Each I/O block can be configured independently to utilize any of the I/O standards supported by the MAX 7000B devices. Additionally, you can use I/O standards with common V_{CCIO} voltages simultaneously within a single block. Each programmable I/O block has its own power supply with separate `VCCIO` pins and support for 3.3-V, 2.5-V, and 1.8-V voltage levels. Figure 2 shows a representation of the MAX 7000B programmable I/O blocks.

Figure 2. MAX 7000B I/O Blocks *Notes (1), (2), (3)*



Notes:
(1) Any input pin can be referenced to one of the two available V_{REF} levels.
(2) MAX 7000B devices have two VREF pins that can be referenced by any I/O pin in both I/O blocks.
(3) The output drivers are dependent on V_{CCIO}. The VCCIO pins for each I/O block can be powered to a different voltage.

The I/O standards supported by MAX 7000B devices are listed in Figure 2.

Operating Conditions

Tables 2 through 14 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only. APEX 20KE and MAX 7000B devices may exceed these specifications. Consult individual device data sheets for details.

Table 2. LVTTL Input Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V		±5	µA
V_{OH}	High-level output voltage	I_{OH} = –4 mA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		0.4	V

Table 3. LVCMOS Input Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Power supply voltage range		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V		±10	µA
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA		0.2	V

Table 4. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V		±10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 mA	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OH} = 1 mA		0.4	V
		I_{OH} = 2 mA		0.7	V

Table 5. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.7	1.9	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage			0.35 × V_{CCIO}	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V		±10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 mA	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		0.45	V

Table 6. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		450	mV
Δ V_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
Δ V_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to APEX devices)		90	100	110	Ω

Table 7. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
I_I	Input pin leakage current	0 < V_{IN} < V_{CCIO}			±10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 8. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 34 mA			0.65	V

Table 9. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –7.6 mA	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 7.6 mA			V_{TT} – 0.57	V

Table 10. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA			V_{TT} – 0.76	V

Table 11. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{TT} – 0.6	V

Table 12. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA			V_{TT} – 0.8	V

Table 13. 3.3-V AGP Input Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage *(1)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(1)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$			±10	µA

Note:
(1) V_{REF} specifies center point of switching range.

Table 14. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF}	Termination and reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$			±10	µA
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high Z)	$GND \le V_{OUT} \le V_{CCIO}$			±10	µA

Using LVDS

The LVDS I/O standard is a high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. LVDS requires a differential input but does not need an input reference voltage. Typical uses for LVDS interfaces are high-bandwidth data transfer, backplane driver, and clock distribution applications.

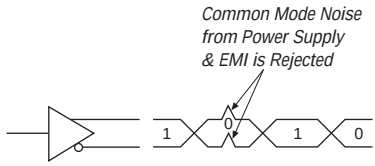
Efficiency

LVDS is a power-efficient standard. Because it contains a low-switching voltage (typically 350 mV) and a DC current of 3.5 mA per channel, the AC power dissipation per signal is small. The load power dissipation is 350 mV × 3.5 mA = 1.225 mW per channel (V × I = P).

Electromagnetic Interference

Due to the low-voltage swing of the LVDS standard, the electromagnetic interference (EMI) effects are much smaller than with CMOS, TTL, or even PECL. EMI is radiated noise created from the acceleration of electric charges within a device and across the transmission medium between devices. Device-generated EMI is dependent on frequency, output-voltage swing, and slew rate. Figure 3 shows that system and power-supply noise do not affect signal quality because they are coupled equally to both LVDS signals.

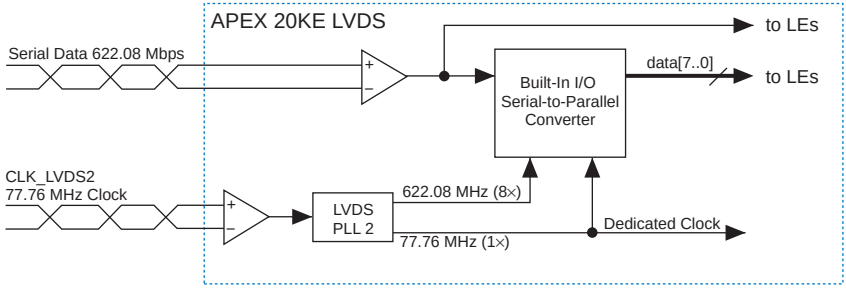
Figure 3. LVDS Rejects System-Level Noise



APEX 20KE LVDS Interface

APEX 20KE devices have dedicated circuitry in the LVDS I/O block to manage a 622.08-Mbps data transfer. For example, an LVDS phase-locked loop (PLL) is used to boost the LVDS input clock from 77.76 MHz to 622.08 MHz for SONET OC-12 applications. The PLL also phase-aligns the clock with incoming data. Figure 4 shows a block diagram of the LVDS circuitry.

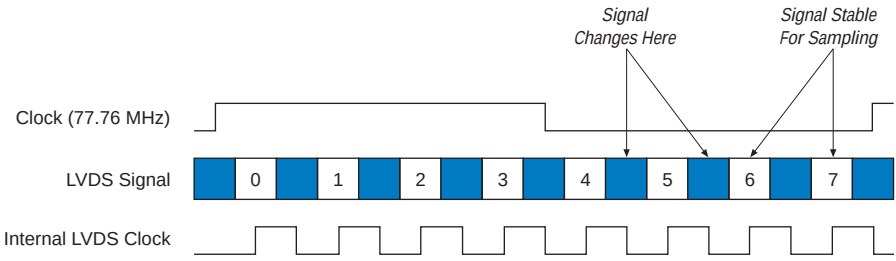
Figure 4. Dedicated LVDS Circuitry



The incoming serial LVDS channels can either use or bypass the serial-to-parallel converter. The serial-to-parallel converter is built into the dedicated silicon, and does not consume any LEs. The parallel converter can operate in different data-conversion modes: 8-to-1, 7-to-1, 4-to-1, and 1-to-1. The LVDS PLL is clocked at 8×, 7×, 4×, and 1× the input clock frequency for 8-to-1, 7-to-1, 4-to-1, and 1-to-1 data conversion, respectively. The 8-to-1 conversion mode is shown in Figure 4. The LVDS PLL can also clock internal logic within the device.

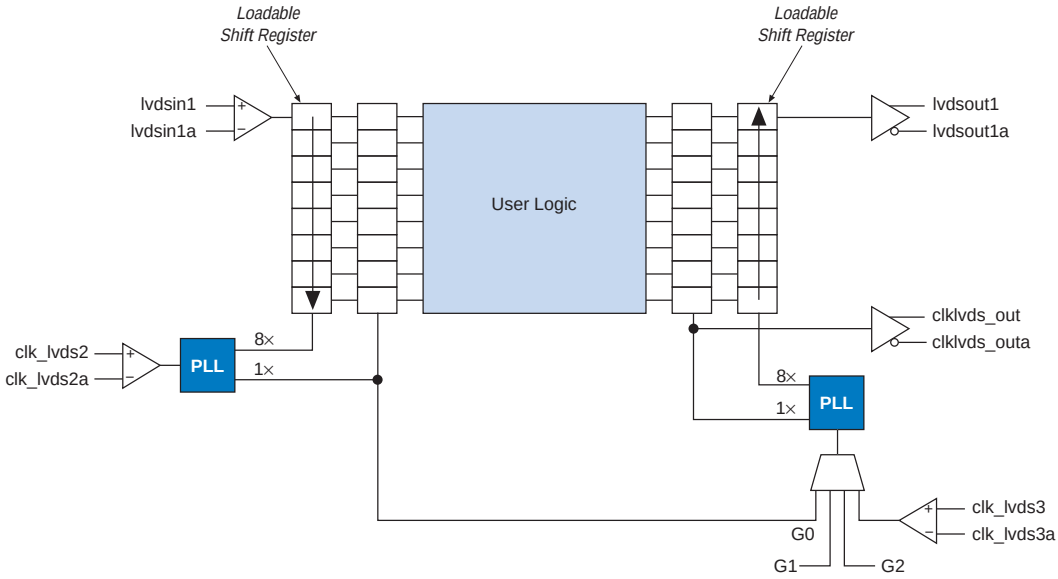
Data synchronization is necessary for the 8-to-1, 7-to-1, and 4-to-1 modes. For example, with an 8-to-1 data conversion at a 77.76-MHz clock frequency, the external clock is multiplied by 8 and phase-aligned with the data to ensure a successful data capture in the serial-to-parallel converter. Figure 5 shows the data synchronization timing diagram for the 8-to-1 data conversion mode.

Figure 5. Internal Data Synchronization



The 16 input LVDS channels in the input block, together with an LVDS PLL, clock the serial-to-parallel converter in the receiver. A parallel-to-serial converter clocked by a separate PLL drives 16 output LVDS channels in the transmitter. The LVDS transmitter converts a maximum of 128 CMOS data bits on-chip into 16 LVDS data streams using an 8-to-1 parallel-to-serial converter. Similarly, the LVDS receiver converts the 16 LVDS data streams back into 128 CMOS data bits. See Figure 6.

Figure 6. LVDS Receiver & Transmitter Interface



The internal PLL clocks have a maximum multiplication rate of 8×. The LVDS transmitter has the ability to drive the 1× locked PLL clock off-chip. The external clock transmits signals in phase with the LVDS data streams. Every cycle, the 16 LVDS I/O channels sample up to 128 bits of input and output data.

The LVDS input pins are row pins located on the right side of the device. Each LVDS input channel interfaces with dedicated shift registers and drives row lines. Similarly, the LVDS output pins are row pins located on the left side of the device. Each LVDS output channel interfaces with dedicated shift registers, driven by peripheral LEs.

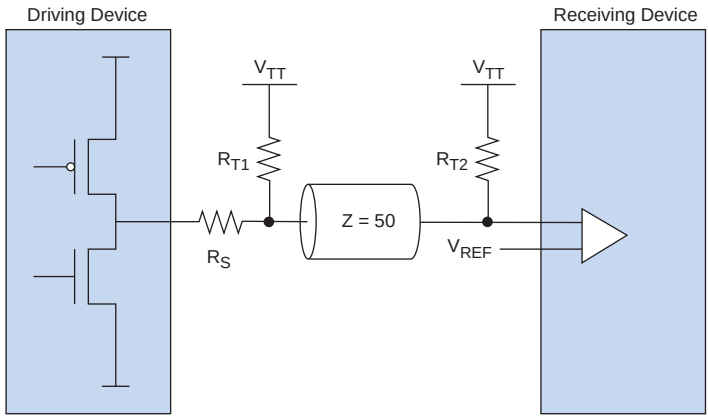
APEX 20KE LVDS Features

The LVDS I/O standard offers fast I/O pins and IOE registers for improved setup and clock-to-output times. The LVDS standard also supports hot-socketing operation; I/O pins can be driven before the device is powered up.

Board Termination Schemes

The various I/O standards supported by APEX 20KE and MAX 7000B devices require specific termination schemes to achieve their high speeds. Each I/O standard has an individual termination scheme. The diagram in Figure 7 shows the series and parallel termination resistors that are used with the I/O standards.

Figure 7. Board Termination Diagram



The LVDS I/O standard requires a termination resistor between the signals at the receiving device as shown in Figure 8. The termination resistor should match the differential load impedance of the bus ranging from 90 to 110 Ω, but typically 100 Ω.

Figure 8. LVDS Board Termination at the Receiver

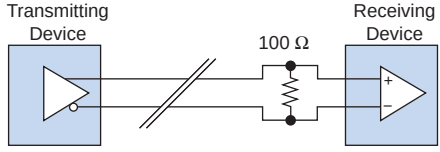


Table 15 shows the board termination values and reference voltages that each APEX 20KE I/O standard uses.

Table 15. Board Termination Values

I/O Standard	Output Driver	R_S (Ω)	R_{T1} (Ω)	R_{T2} (Ω)	V_{REF} (V)	V_{TT} (V)
GTL+	Open-drain	–	–	25	1.0	1.5
SSTL-2 Class I	Push-pull	25	–	50	1.1	1.125
SSTL-2 Class II	Push-pull	25	50	50	1.125	1.125
SSTL-3 Class I	Push-pull	25	–	50	1.5	1.5
SSTL-3 Class II	Push-pull	25	50	50	1.5	1.5
AGP	Push-pull	–	–	–	1.32	–
CTT	Push-pull	–	–	50	1.5	1.5

Conclusion

The new programmable I/O features and standards simplify board design by minimizing the number of devices used to interface with memory, microprocessors, and backplanes. APEX 20KE devices are 64-bit, 66-MHz PCI compliant and offer increased I/O performance with new standards and features like LVDS (622.08-Mbps data transfer), programmable delays, and fast APEX I/O.

References

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- *Stub-Series Terminated Logic for 2.5 Volts (SSTL-2)*, EIA/JESD8-9, Electronic Industries Association, September 1998.
- *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*, ANSI/TIA/EIA-644, American National Standards Institute/Telecommunication Industry Association/Electronic Industries Association.
- *2.5 V ±0.2 V (Normal Range) and 1.7 V to 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit*, EIA/JESD8-5, Electronic Industries Association, October 1995.
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