Implementing a W-CDMA System

with Altera Devices & IP Functions

September 2000, ver. 1.0 Application Note 129

Introduction

In the wireless world, the demand for advanced information services is growing. Voice and low-rate data services are insufficient in a world where high-speed Internet access is taken for granted. The trend is toward global information networks that offer flexible multimedia information services to users on demand, anywhere, anytime. The need to support bandwidth-intensive multimedia services places new and challenging demands on cellular systems and networks.

The International Telecommunications Union (ITU), under an initiative named IMT-2000, devised a number of standards that support these new requirements. However, third-generation wireless standards will continue to evolve in the future as new services and technologies are identified. Systems that implement these standards must be flexible enough to accommodate changes easily. Additionally, because the demand for third-generation products is still unknown, it is diffcult to justify high non-recurring engineering (NRE) costs.

ASICs—with their associated NRE costs and long turnaround times—are expensive to respin. For example, the lower-limit block level in the turbo specification changed four months after the specification was initially released. An ASIC design implementing a turbo function based on the initial specification would need to be reworked.

The advanced capacity enhancement techniques, which are contemplated in academic circles, require a high throughput platform. A programmable solution that provides flexibility, zero NRE costs, and the required throughput is the right solution for third-generation wireless applications.

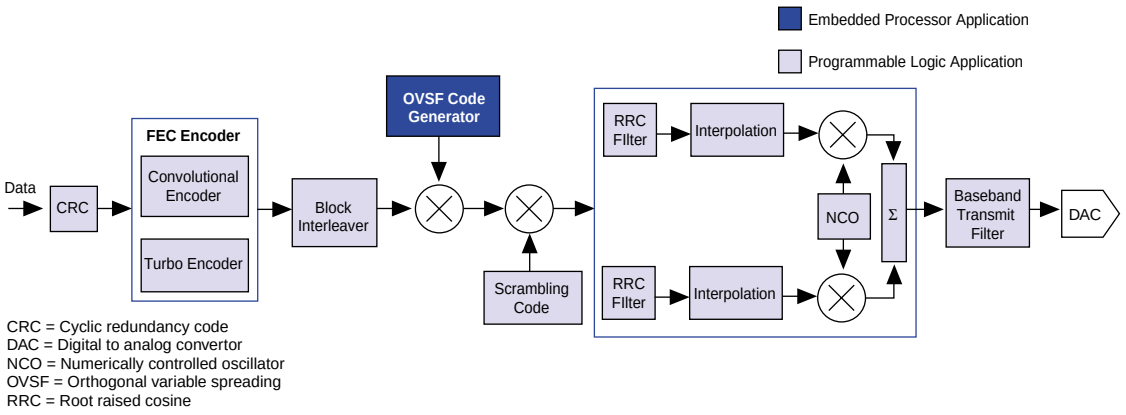
Altera® high-density, high-performance programmable logic devices (PLDs) combined with intellectual property (IP) functions and the Quartus™ development software provide a complete solution for the wireless communications market. For example, Altera's high-density APEX™ devices can implement thousands of multiply-accumulators (MACs), making it feasible to develop a very high throughput platform. This application note describes how to implement a wideband code division multiple access (W-CDMA) system that conforms to the IMT-2000 standard using Altera devices and IP functions.

For information about Altera devices, IP functions, and software tools refer to the Altera web site at **http://www.altera.com**.

W-CDMA Transmitter

This section describes the digital architecture of a downlink transmitter that supports the W-CDMA standard. Figure 1 shows a block diagram of the transmitter. Light shaded blocks can be implemented in an Altera PLD; dark shaded blocks can be implemented in software in the embedded processor of an Excalibur™ embedded processor PLD.

Figure 1. W-CDMA Transmitter Architecture



To conform to the W-CDMA standard, cyclic redundancy code (CRC) bits are added for error detection, and error correction bits are added for channel coding. The data is then spread with a user- or channel-specific code to produce a data stream at a given chip-rate. The spread data stream is scrambled with Gold code so that multipath signals can be uniquely identified and decoded by the receiver. To transmit a signal within the specified bandwidth, the data bits are shaped using a pulse shaping filter. Next, the signal goes through carrier modulation and up-conversion to radio frequency (RF), and is then sent to the antenna to be transmitted over the air. The various functions used in the transmitter are described in the following sections, including:

- CRC checker
- Forward error correction (FEC)
- Block interleaver
- Orthogonal variable spreading (OVSF) channelization codes
- Scrambling codes
- Quadrature phase shift keying (QPSK) modulator

CRC Checker

The standard specifies four different polynomials for CRC checking:

- $g_{CRC24}(D) = D^{24} + D^{23} + D^6 + D^5 + D + 1$
- $g_{CRC16}(D) = D^{16} + D^{12} + D^5 + 1$
- $g_{CRC12}(D) = D^{12} + D^{11} + D^3 + D^2 + D + 1$
- $g_{CRC8}(D) = D^8 + D^7 + D^4 + D^3 + D + 1$

Altera provides the CRC MegaCore® function, which can implement these polynomials and therefore meets the third-generation standard requirements. The CRC function is fully parameterized, including:

- Variable length generator polynomial
- Variable data width from 1 bit to the width of the polynomial
- Any initial value

Forward Error Correction

The standard defines two encoding schemes to support different quality of services. For voice and MPEG4 applications, the standard employs convolutional encoding, which gives a bit error rate (BER) of up to 10^{-3}. For data applications, the standard uses turbo encoding, which gives a BER of up to 10^{-6}.

Convolutional Encoder

The required specification for a convolutional encoder is given below:

- Basestation: K = 9 and rate = 1/2 and 1/3
- Mobile: K = 9 and rate = 1/3

A convolutional encoder uses delay elements and XORs. Altera provides building blocks optimized for Altera PLDs in the library of parameterized modules (LPM). You can use these functions, for example LPM_SHIFTREG and LPM_XOR, to implement a convolutional encoder.

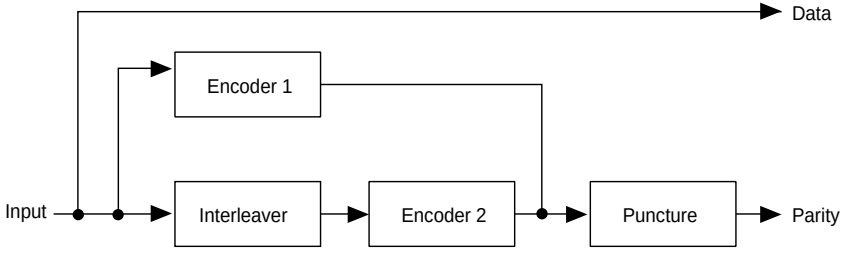
Turbo Encoder

Turbo encoding gives a relatively large encoding gain with a reasonable computational complexity. This encoding scheme is useful for data services that permit longer transmission delays. The W-CDMA specifications are:

- Parallel concatenated convolutional code (PCCC) with two 8-state constituent encoders and an interleaver
- Block size: 40 to 5,114 bits
- Puncturing: rate = 1/3 (no puncturing); rate = 1/2 (puncturing)

Altera provides the turbo encoder MegaCore function, which meets the W-CDMA standard. See Figure 2 for a block diagram. The turbo encoder uses 3,000 logic elements (LEs) and 10 embedded system blocks (ESBs) when implemented in an APEX 20K device.

Figure 2. Turbo Encoder Block Diagram



Block Interleaver

Systems that transmit digital data require error correction to reduce the effect of spurious or burst noise from the channel that can corrupt data. A block interleaving function writes data into a rectangular matrix and then reorders the columns of the matrix based on the transmission time interval (TTI) value. APEX device ESBs can store a matrix of elements. To permute the columns, the data is read out column by column in the right sequence. A software routine running in an embedded processor can generate the correct read address.

OVSF Channelization Codes

Transmissions from a single source are separated by channelization codes, i.e., download connections within one sector and the dedicated physical channel on the uplink. The OVSF channelization code preserves the orthogonality between different physical channels using a tree-structured orthogonal code. The tree-structured code is generated recursively using the following equation:

$$C_{2n} = \begin{bmatrix} C_{2n,1} \\ C_{2n,2} \\ C_{2n,2n} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} C_{n,1} & C_{n,1} \\ C_{n,1} & -C_{n,1} \end{bmatrix} \\ \begin{bmatrix} C_{n,n} & C_{n,n} \\ C_{n,n} & -C_{n,n} \end{bmatrix} \end{bmatrix}$$

Because the process is recursive, you can implement OVSF code generation in software in an Excalibur embedded processor PLD. The device's memory blocks can store the intermediate results.

Other operations within basestation subsystems may need to refer to the OVSF code assigned to different users. The content-addressable memory (CAM) in Altera devices can store the code so that it can be quickly accessed when needed. See the *Designing Wireless Basestations with APEX CAM White Paper* for more information.

Scrambling Codes

Scrambling codes make the direct sequence CDMA (DS-CDMA) technique more effective in a multipath environment. It significantly reduces the auto-correlation between different time delayed versions of a spreading code so that the different paths can be uniquely decoded by the receiver. Additionally, scrambling codes separate users and basestation sectors from each other by allowing them to manage their own OVSF trees without coordinating amongst themselves. The W-CDMA specification for the scrambling code generator is described below.

Downlink:

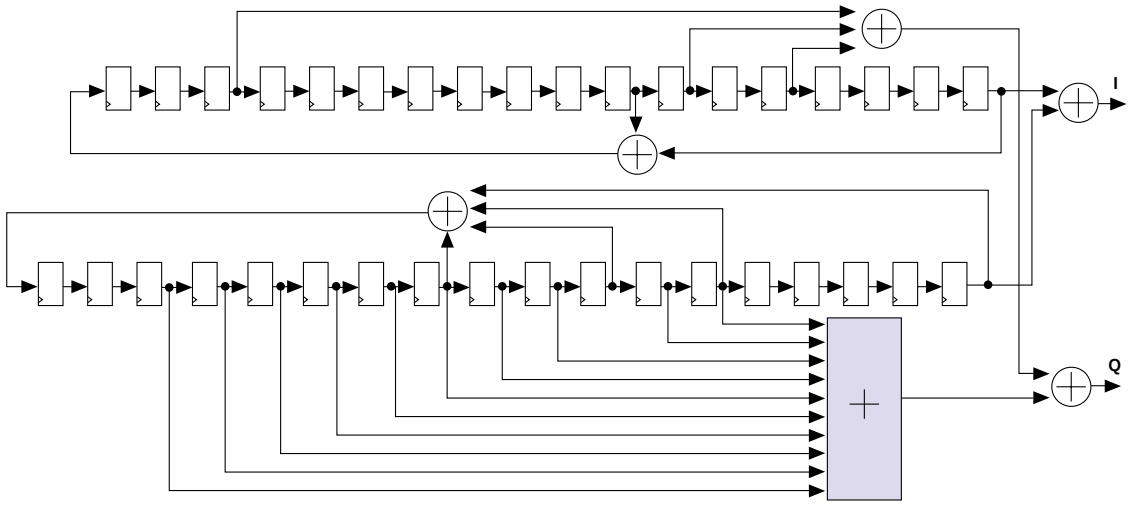
- 38,400 chips of 2^{18} Gold code
- 512 different scrambling codes
- Grouped for efficient cell search

Uplink:

- Long Code: 38,400 chips of 225 Gold code
- Short Code: 256 chips of very large Kasami code

Figure 3 shows the downlink scrambling code block diagram.

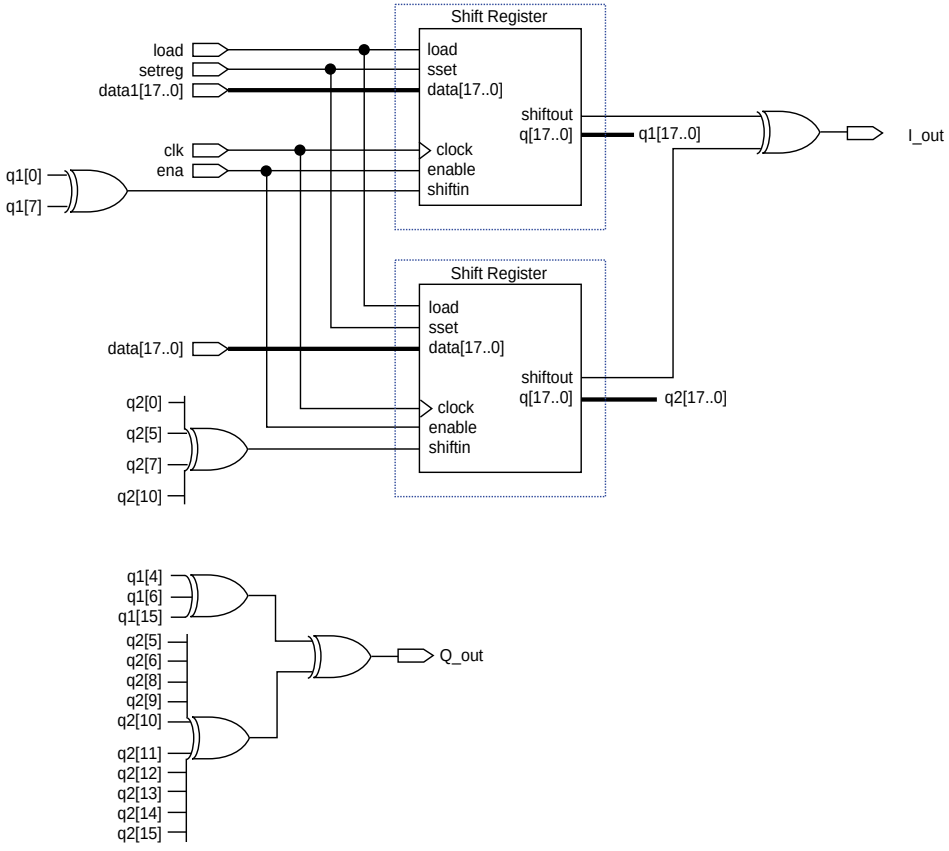
Figure 3. Scrambling Code Generator



You can design the scrambling code generator using the same LPM functions used for the convolutional encoder (i.e., LPM_SHIFTREG and LPM_XOR). Figure 4 shows a scrambling code generator schematic. The design highlights the ease with which the generator can be designed using LPM functions.

Figure 4. Scrambling Code Generator Schematic (Downlink)

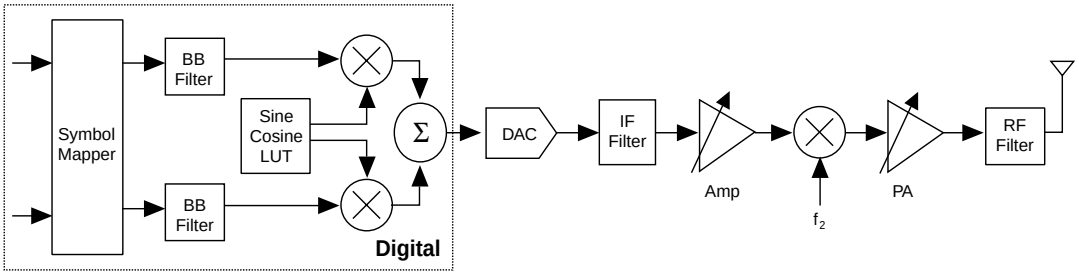
This design uses 43 LEs, which is 1% of the resources available in an EPF20K100E device.



QPSK Modulator

Figure 5 shows a modulator that performs baseband filtering and carrier modulation in the digital domain.

Figure 5. Digital I/Q Modulator



Using a digital I/Q modulator instead of an analog one has several advantages, including:

- Channels can be selected in the digital domain using a numerically controlled oscillator (NCO) and a digital mixer.
- The direct digital synthesizer gives more precise frequency selection and shorter settling time; it also provides good amplitude and phase balance.
- A digital filter provides extremely linear phase and a very low shape factor.

To meet the W-CDMA requirements, the following elements are needed:

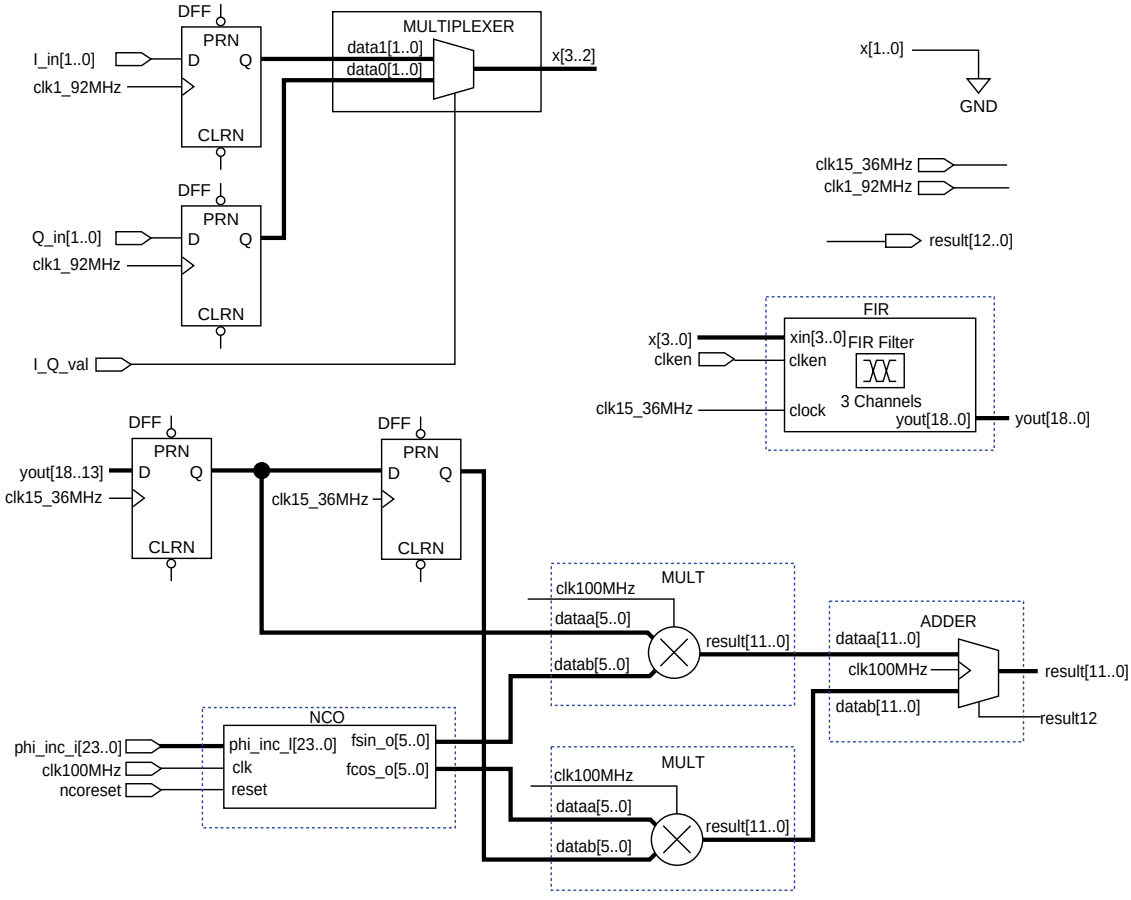
- Nyquist filter
  - Root raised cosine filter: $\alpha = 0.22$
  - Sampling rate: 3.84 Msps × 4
- NCO
  - 60-MHz bandwidth for channel mapping
  - High spurious free dynamic range (SFDR)

Altera provides the following IP functions, which you can use to build a complete modulator:

- FIR Compiler to create a root raised cosine interpolation filter
- NCO Compiler to create an NCO
- `LPM_MULT` LPM function to create a digital mixer

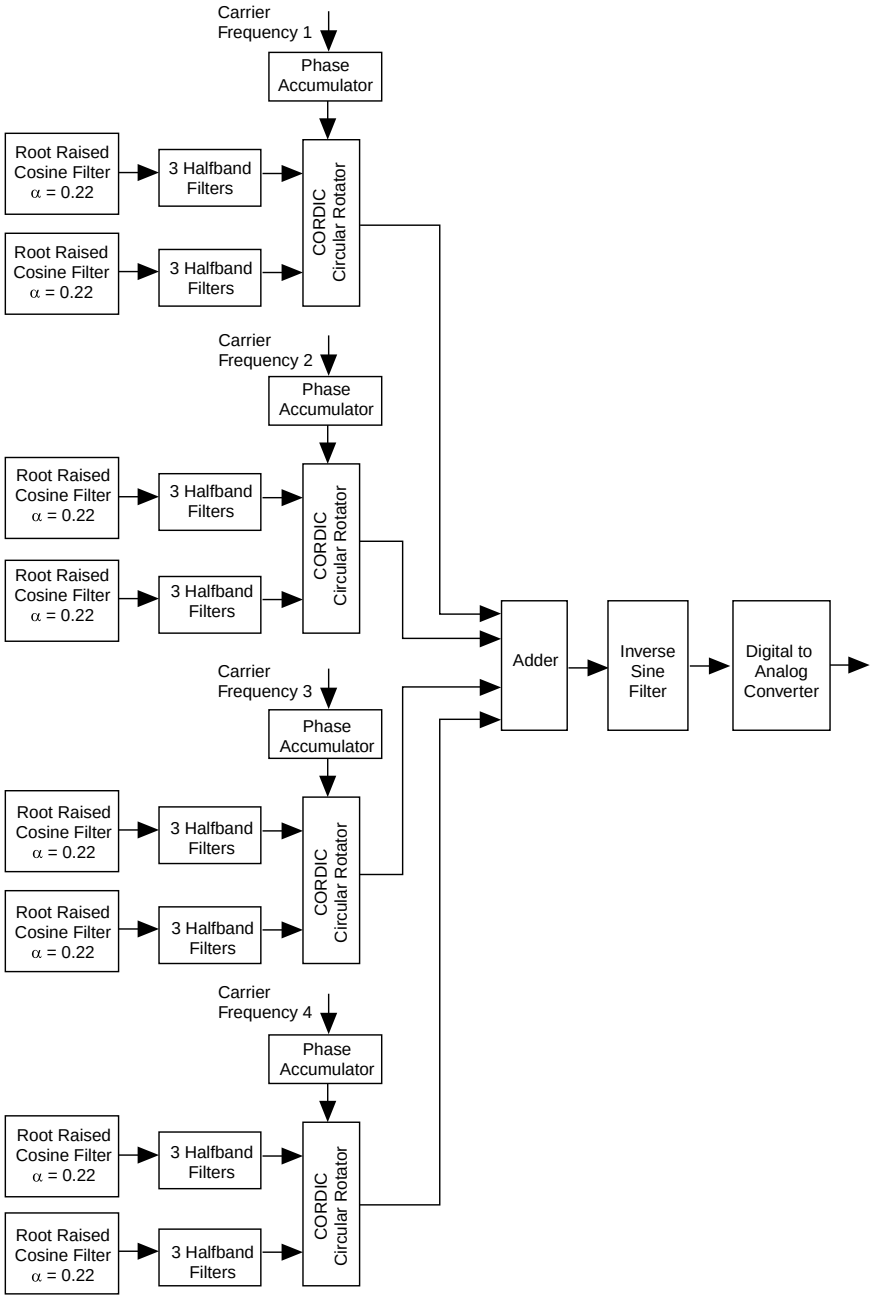
Figure 6 shows a functional QPSK modulator design. This design is not fully optimized, however it still only uses 2,092 LEs and 24 ESBs, which is 50% of the total LEs available in an EP20K100E and 92% of the total ESB bits.

Figure 6. QPSK Modulator Schematic (Downlink)



A novel approach is to implement a multi-carrier QAM modulator based on the CORDIC algorithm. See Figure 7. A quad modulator that fulfills the spectrum and error vector magnitude (EVM) specification of W-CDMA has been implemented in Altera PLDs and is discussed in *A Multicarrier QAM Modulator, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*. See "References" on page 20. Each of the modulators consist of a pair of root raised cosine filters. These half-band filters connect to the CORDIC rotator, and directly translate the baseband signal to intermediate frequency (IF). To compensate for the sinx/x roll-off effect of the digital-to-analog convertors, a band-pass filter with inverse sinx/x profile is employed.

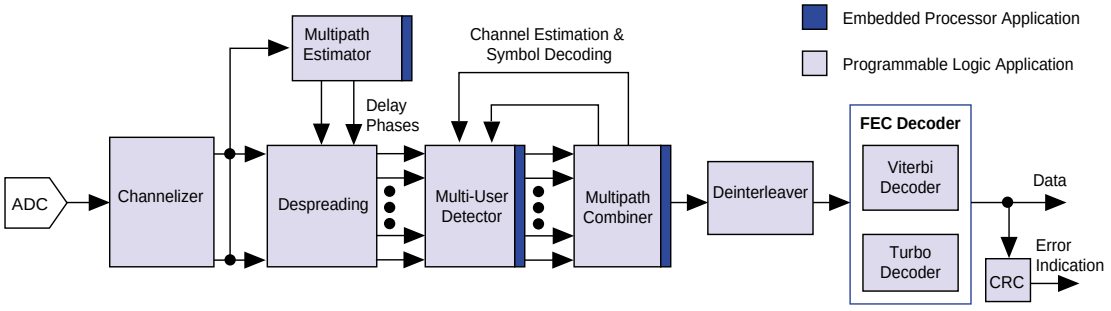
Figure 7. CORDIC-Based QAM Modulator



W-CDMA Receiver

This section describes the digital architecture of a receiver that supports the W-CDMA standard. Figure 8 shows a block diagram. Light shaded blocks can be implemented in an Altera PLD; dark shaded blocks can be implemented in software in the embedded processor of an Excalibur embedded processor PLD.

Figure 8. W-CDMA Receiver Architecture



I/Q Demodulator

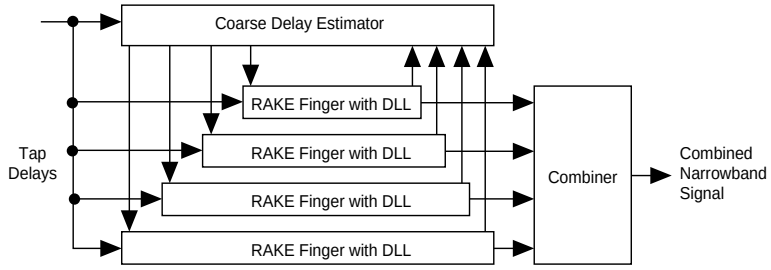
The I/Q demodulator can be created using Altera products in a manner similar to the QPSK modulator described on page 7.

Despreading

The radio environment of a wireless network system is a multipath environment. To be effective, the system requires a despreader that can simultaneously despread the numerous multipaths of both a single user as well as multiple users (if doing a joint detection). A RAKE receiver, with its multiple fingers to despread different multipaths, is well suited for this function.

A traditional approach, shown in Figure 9, uses a coarse delay estimation unit to find the appropriate tap values, and then triggers delay-locked loops (DLLs) connected to the finger to track the multipath. However, this implementation is not desirable because it is complex and decentralizes the process of tracking the multipaths.

Figure 9. Traditional DLL-Based Receiver



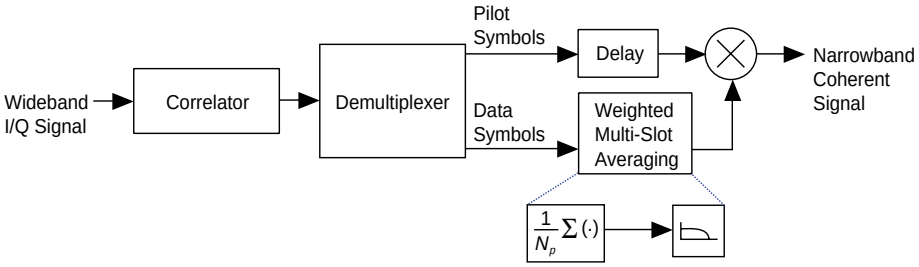
A more desirable implementation is a full-matched filter that gives a new tap value every sample time. A full-matched filter eliminates the need for dedicated DLLs and creates a centrally controlled RAKE receiver that is simpler than a distributed one with DLLs. High-density Excalibur embedded processor PLDs can implement a full-matched filter in programmable logic, and control logic in the embedded processor.

Channel Estimator & Signal Decoder

To correct for channel distortion, the system has complex amplitude and phase estimation. This action is part of the RAKE receiver, and is required for coherent detection. One of the schemes used to estimate complex amplitudes is a pilot symbol-assisted channel estimation filter, called a weighted multi-slot averaging (WMSA) channel estimation filter. In this scheme, the wideband signal is converted to a narrowband signal using a binary correlator. The pilot symbols are then demultiplexed from data symbols. The pilot symbols are averaged over multiple slots to get a better average over the slot. See Figure 10.

Excalibur PLDs can implement a RAKE receiver with the correlator portion in logic and the control portion in the embedded processor.

Figure 10. Channel Estimator & Signal Decoder



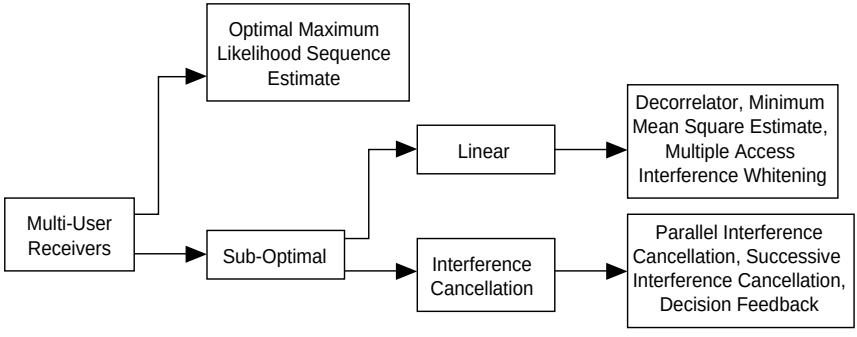
You can effectively implement the correlator and filter in an Altera PLD.

Multi-User Detector/Interference Cancellation

The capacity of a DS-CDMA system is interference limited. Every user acts as interference for ever other user. The more resistant the system is to interference, the more users can be served. Multi-user detection (MUD) techniques—also called joint detection and interference cancellation (IC)—reduce the effect of multiple access interference and increase system capacity.

The maximum likelihood sequence estimator (MLSE) is a well-known optimal detection algorithm. However, it is too complex for practical DS-CDMA systems. Therefore, most research and development efforts are focused on developing sub-optimal schemes. There are two classes of sub-optimal schemes: linear and IC. See Figure 11.

Figure 11. MUD Schemes



Simulation has shown that groupwise successive IC is the most promising scheme. In this scheme, users are grouped according to their spreading factor and then IC or a decorrelator is applied within the group. Processing starts with the lowest SF group and processes towards the highest SF group.

To illustrate how to implement MUD in a PLD, two IC-based schemes are discussed, wideband SIC and narrowband SIC.

Wideband SIC

In this scheme, the interfering signals are cancelled in a wideband domain. First, the RAKE receiver decorrelates the number of users and their multipaths. Next, the decorrelated signals are grouped based on their signal strength and spreading factor. The appropriate signals are regenerated using their corresponding spreading code and cancelled from the incoming wideband signal. Finally, the residual signal from the cancellation process is added back to the different signals that are tracked before they are decorrelated with their respective codes.

Figure 12 shows a block-level overview.

Figure 12. Wideband SIC Block-Level Overview

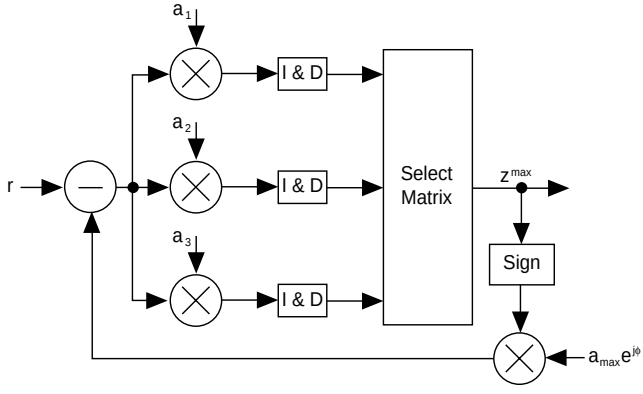
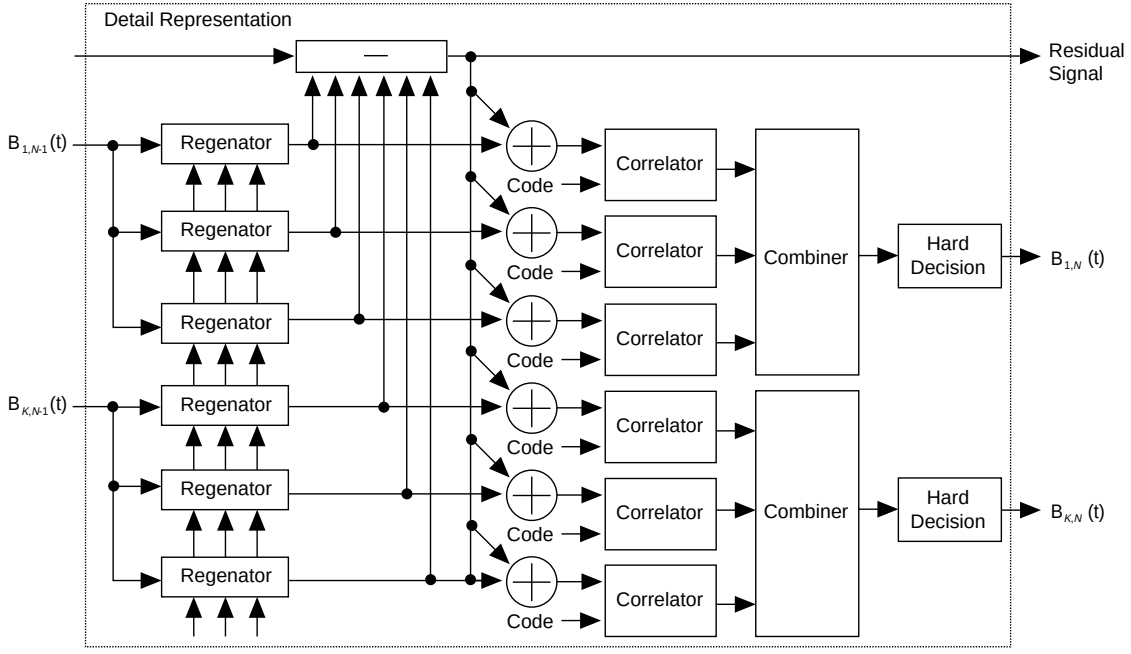


Figure 13 shows a detailed diagram.

Figure 13. Wideband SIC Detailed Block Diagram

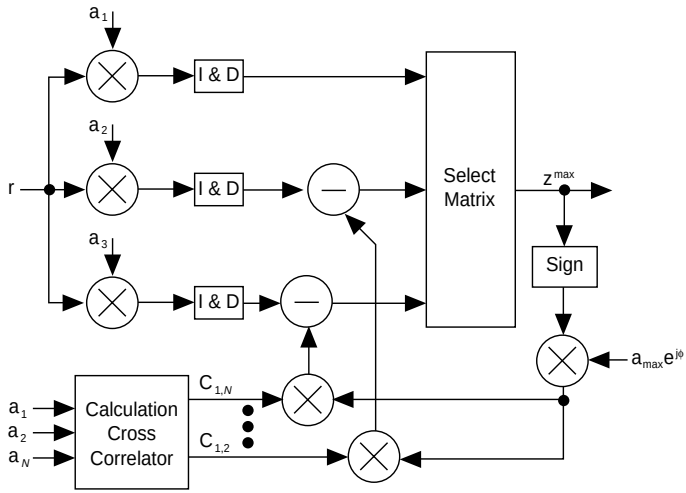


All of the blocks except the combiner can be implemented in programmable logic. The combiner—with its complex algorithm for weighted combining and low-speed signal processing requirement (3.84 Msps)—can be implemented effectively in software running in an Excalibur embedded processor PLDs.

Narrowband SIC

In this scheme, the interfering signals are cancelled in the narrowband domain. After the signals are grouped and regenerated (as they would be in a wideband SIC scheme), they are decorrelated by a cross-correlation matrix. The cross-correlation matrix contains the auto-correlation and cross-correlation coefficients between the different spreading codes. Cancelling the signals removes the interference due to correlation with other spreading codes. See Figure 14.

Figure 14. Narrowband SIC



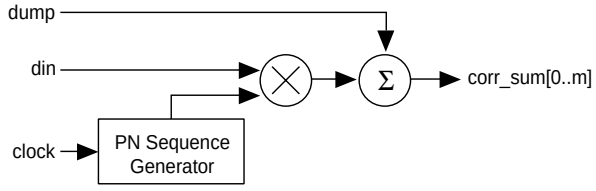
Evaluating the cross-correlation matrix is a computationally intensive task. A new matrix must be calculated and inverted every time the user profile changes or multipath tap changes. Therefore, the W-CDMA specification uses a 245 chips short code (called very long Kasami code). With short spreading code, this implementation is more feasible.

To evaluate the cross-correlation matrix, a number of algorithms that exploit the special structure of the matrix—namely the band and block Toeplitz structures—can be used. One approach is to extend the block-Toeplitz system matrix into a block circulant matrix that can be inverted with little computational effort using a block fast Fourier transform (FFT) function. For more information, refer to "Efficient Joint Detection Techniques in the Frequency Domain for Third Generation Mobile Radio Systems." See "References" on page 20. This approach is well-suited for implementation in programmable logic with a parallel architecture for efficient computation. Additionally, Altera provides the FFT processor function, which is also suited for this application.

Sequential Correlator

In the sequential correlator, each incoming sample is multiplied by a PN sequence that advances at the chip rate. In a practical implementation, the data values are soft symbols where a large value indicates more confidence that the symbol has been received correctly. Results from multiplication stage are accumulated over the symbol period. At the end of the period, the correlation sum is dumped. You can use the Sequential Correlator function from Nova Engineering, Inc., an AMPP partner, to implement the finger of a RAKE receiver as well as the correlator in MUD blocks discussed previously.

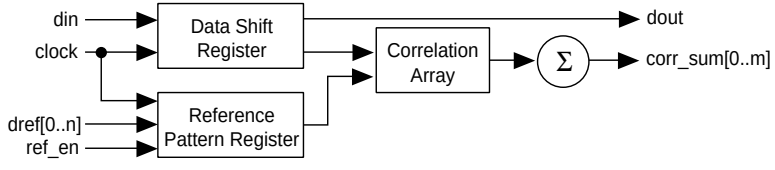
Figure 15. Sequential Correlator



Parallel Correlator

In the parallel correlator, data samples are held in a long shift register, and the pilot PN sequence is held in a reference pattern register. Each time a new sample is loaded into the data shift register, the contents of the two registers are multiplied and integrated to give a new correlation sum. See Figure 16. You can use the Parallel Correlator function from Nova Engineering, Inc., an AMPP partner, to implement the multipath delay estimator.

Figure 16. Parallel Correlator



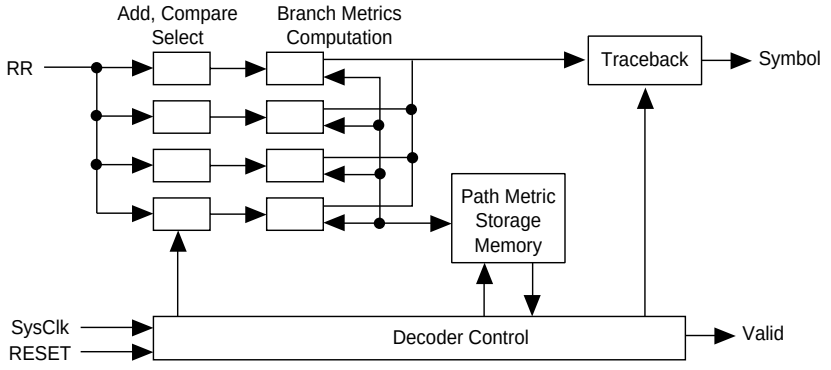
Decoders

There are two types of decoders that can be used in the receiver. The Viterbi decoder is used to decode signals encoded using convolutional encoders; the turbo decoder is used with the turbo encoder.

Viterbi Decoder

The Viterbi algorithm is the optimal algorithm to decode convolutionally encoded data. The complexity of Viterbi decoding is an exponential function of the constraint length. W-CDMA requires a decoder with a constraint length of 9, which poses an implementation challenge. Altera provides the Viterbi MegaCore function that meets W-CDMA requirements. See Figure 17 for a block diagram.

Figure 17. Viterbi Decoder Block Diagram



There are two different Viterbi implementations depending on the throughput requirements. See Table 1.

Table 1. Viterbi Throughput

Implementation	LEs	Speed
Serial	1,300	500 Kbps
Serial/parallel	2,600	2 Mbps

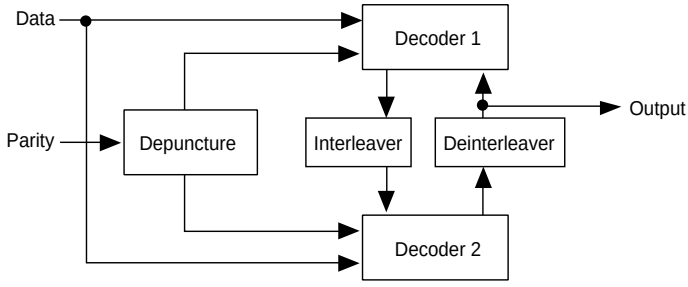
Turbo Decoder

The turbo decoder is used to decode turbo encoded data. The decoder should handle codes of different rates and block sizes encoded by the encoder. Altera provides the turbo decoder MegaCore function, which has the following features:

- Max-logMAP decoder for maximum performance
- Includes UMTS-specific interleaver
- Fully parameterized to tailor decoder to system requirements
- Memory bank swap mechanism for increased throughput

See Figure 18 for a block diagram.

Figure 18. Turbo Decoder Block Diagram



Conclusion

Third-generation wireless has the potential to offer exciting new services. However, the demand is unknown and related technologies are evolving. Also, a high throughput platform is required to support capacity enhancement techniques. These requirements demand a flexible solution that can also provide necessary performance. The Altera portfolio of IP functions, large PLDs with advanced features, and Excalibur embedded processor PLDs, offers the most complete solution for the third-generation W-CDMA standard.

References

H. Andoh, M. Sawahashi, and F. Adachi. "Channel Estimation Filter Using Time-Multiplexed Pilot Channel for Coherent RAKE Combining in DS-CDMA Mobile Radio," *IEICE Trans. Communications*, Vol. E81-B, No. 7, July 1998.

Juntti, M., "Performance of Multi-User Detection in Multi-rate CDMA Systems," *Wireless Personal Communication*, submitted.

Marius Vollmew, Jurgen Gotze, and Martin Haardt. "Efficient Joint Detection Techniques in the Frequency Domain for Third Generation Mobile Radio Systems," *IEEE International Conference in Third Generation Wireless Communication*, June 2000.

Jouko Vankka, et al. "A Multicarrier QAM Modulator," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol. 47, No. 1, January 2000.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com