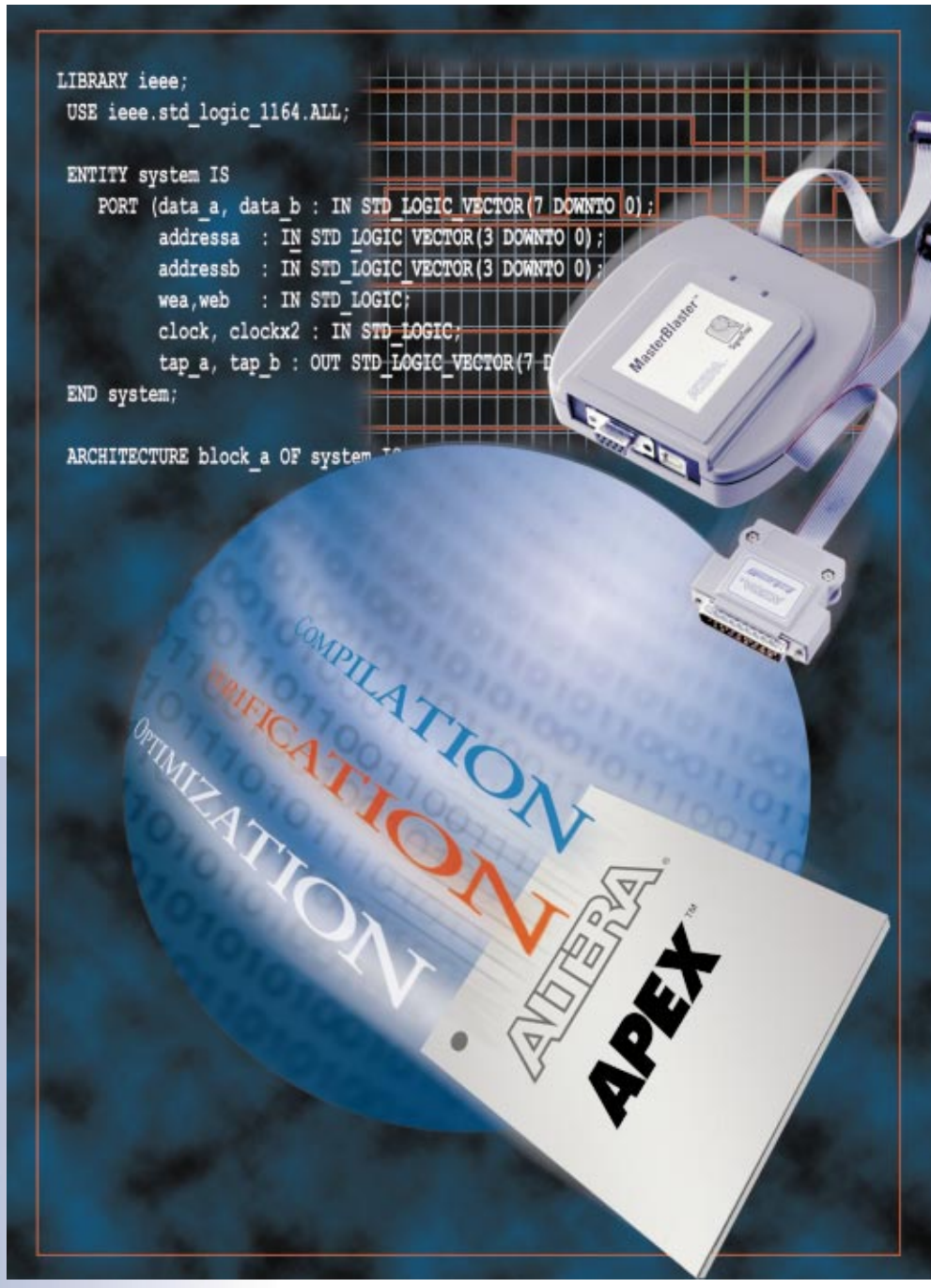
Quartus

The Next-Generation Development System for Programmable Logic

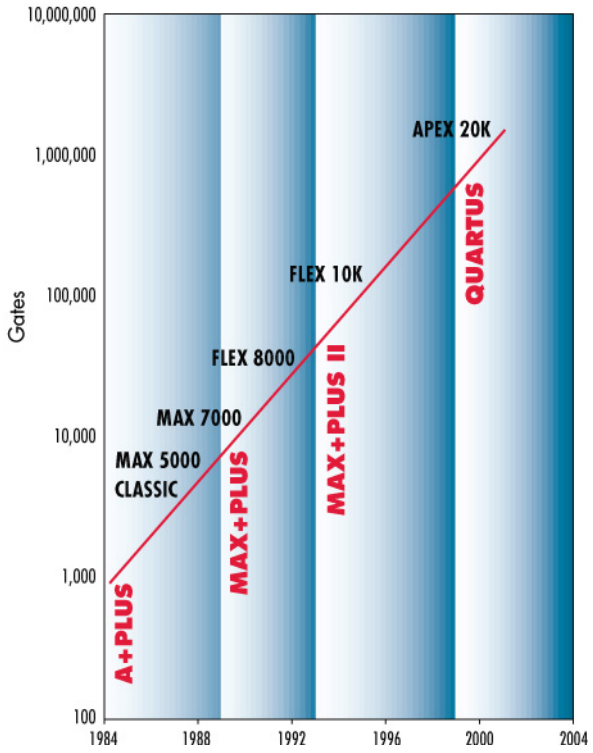


June 2000

Design Tools for Increasing Device Densities

As device densities increase, design methodologies for programmable logic devices (PLDs) must continue to evolve. The Quartus™ software, Altera's fourth-generation development system for programmable logic, allows designers to process multi-million gate designs with advancements never before seen in PLD development tools. With the Quartus software, Altera continues its commitment to provide development software with unmatched flexibility and performance.

Figure 1. Quartus Software Supports High-Density Design Methodology



The Quartus software offers new process advances that use state-of-the-art features to shorten design cycles. To streamline the development flow and increase productivity, the Quartus software supports system-level solutions with block-level editing, integration with standard source-control software, and expanded support for megafunctions. A new logic analysis solution reduces verification time by enabling engineers to see internal chip signal values while the system is running at speed.

Quartus software interfaces seamlessly with third-party EDA software tools, allowing designers to use the tools they are already familiar with to design for Altera devices. Altera software subscriptions even include a suite of third-party EDA tools so that all Quartus customers have access to world-class synthesis and simulation tools. The Quartus software is also "Internet-aware," providing up-to-the-minute information and file exchanges, including software updates, license files, and support services across the Internet. Altera effectively becomes a member of the design team by providing this unmatched level of technical support. Together, these features make the Quartus software the ideal platform for multi-million-gate designs.

Megafunctions for High-Density Design

Creating designs for system-on-a-programmable-chip architectures requires efficiency throughout the design cycle. Designers can use functions that have already been tested and optimized to further reduce their design time. Altera users have two primary choices of functions: Altera-created megafunctions—called MegaCore™ functions—that are optimized for Altera device architectures, and megafunctions from the Altera Megafunction Partners Program (AMPP℠). AMPP partners provide a broad portfolio of Altera-optimized megafunctions that are developed by third-party vendors.

Quartus software expands the support for megafunctions by enabling instance-specific assignments and greater control over synthesis. Customers can maintain assignments for each instance of a MegaCore or AMPP megafunction in a design rather than for each function.

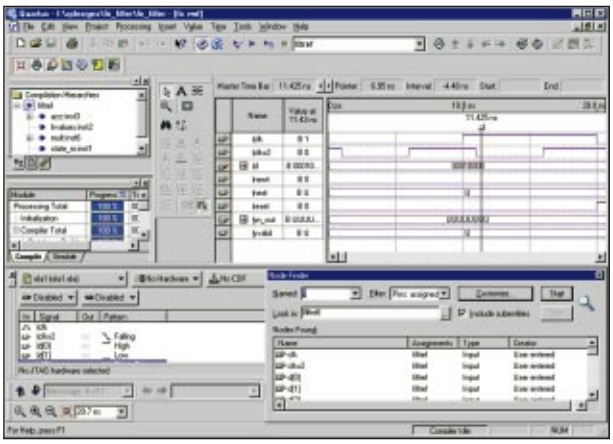
OpenCore Risk-Free Evaluation

The Quartus OpenCore™ evaluation feature offers you a risk-free method of evaluating AMPP and MegaCore functions. With the OpenCore feature, you can instantiate, compile, and simulate your designs to verify a function's size and performance before making a licensing decision. MegaCore functions can be downloaded for OpenCore evaluation from the Altera world-wide web site at **http://www.altera.com/IPmegastore**.

Improved Verification Flow & SignalTap Logic Analysis

Design verification has become the longest process in developing multi-million gate designs. The Quartus software reduces verification time by providing tight integration to register transfer level (RTL)-based simulation. The Quartus software also easily integrates with third-party simulators, allowing designers to choose the most efficient verification flow to fit their needs. In addition to running software simulations, designers can use Altera's SignalTap™ logic analysis solution to perform hardware debugging.

Figure 2. Quartus Verification Interface



For many designs, system-level verification is very time-consuming, and sometimes extremely difficult on devices with high I/O ball-grid array packages. SignalTap logic analysis facilitates the verification process by integrating the functionality of a logic analyzer within the software.

Using SignalTap logic analysis, designers can capture internal signals of a device and route them to pins for monitoring. The Quartus software inserts a logic analyzer megafunction that incorporates the functionality of a logic analyzer and the triggering options into the design. Data is stored in the device's embedded RAM block and reported to the Quartus waveform viewer via a download cable. The SignalTap logic analysis tool allows the design team to perform this analysis on a device running at actual speed.

SignalTap logic analysis accelerates the verification flow by building upon the fact that programmable logic offers the benefit of shortening design cycles. For verification purposes, PLDs offer specific advantages:

True System-Level Verification

Because PLDs remove the risks associated with silicon changes, multiple verification iterations can be made on PLDs. These iterations can be performed in-system at system clock speeds. Millions of true system vectors can be applied per second to test numerous operating conditions. Also, a PLD implementation enables development to begin earlier on real hardware, rather than on software models or emulators.

Elimination of the Probing Bottleneck

For PLDs with embedded RAM, a logic analyzer can be implemented in silicon, eliminating the need for an external analyzer. Because it is on-chip, the logic analyzer has full access to any signal in the design. Data is stored in the embedded RAM, and scanned out serially to preserve I/O pins. This data is then assembled on a PC and presented in a waveform display.

Flexibility

Changes in the design and configuration of the logic analyzer can be quick and painless with PLDs. Designers can continue using their verification tools and flows with the Quartus software and avoid the steep learning curve that is typically involved with using a new software tool. They can also take advantage of the innovative SignalTap logic analysis solution to perform system-level verification on chips running at speed. Designs can go into production much faster with these enhancements to the verification process.

SignalTap Plus

The SignalTap Plus system analyzer is a powerful system-level debug tool from Altera that enhances the on-chip debug capabilities of the SignalTap embedded logic analyzer (ELA) by adding 32 channels of external logic analysis capability. SignalTap Plus enables you to capture signals from internal PLD nodes and external board-level nodes simultaneously, and view them all in a single, time-correlated display. The new SignalTap Front Panel software provides stand-alone debugging capabilities. SignalTap Front Panel software runs separately or from within the Quartus software to control APEX™ device configuration, the SignalTap ELA, and the SignalTap Plus System Analyzer.

World-Class Synthesis & Simulation

All Altera subscription products now include world-class synthesis and behavioral simulation tools from Synopsys, Exemplar Logic, and Model Technology. These leading-edge tools are tightly integrated with Quartus through NativeLink™ integration to provide a seamless user interface and best-in-class quality of results (QoR).

The Synopsys FPGA *Express* software includes VHDL and Verilog synthesis support. FPGA *Express* provides a complete synthesis environment including Altera-specific architecture optimizations, static timing analysis, constraint management, and a schematic viewer. Designers have a full range of synthesis flows under their control in an easy-to-use interface. These flows include push-button, constraint-based, hierarchical, and script-based synthesis. Integration with Altera's Quartus software is also provided, allowing the ability to launch Quartus from within FPGA *Express*.

The LeonardoSpectrum software from Exemplar Logic includes VHDL or Verilog synthesis support. The LeonardoSpectrum synthesis tool combines push-button ease-of-use with powerful control and optimization features normally associated with workstation-based ASIC tools.

The Model Technology ModelSim software includes VHDL or Verilog simulation support. ModelSim is the world's leading HDL simulation tool. By including ModelSim with the Quartus software, Altera provides world-class simulation capabilities including support for HDL test benches and pre-place-and-route simulation. ModelSim also supports tool command language (Tcl) scripting for user-defined functions and automation.

Push-Button Support for Advanced Device Features

The Quartus MegaWizard™ Plug-In Manager combined with dedicated circuitry in APEX 20KE devices can be used to enable advanced design features such as content-addressable memory (CAM), phase-locked loops (PLLs), and low-voltage differential signaling (LVDS). With the MegaWizard Plug-In Manager interface, the designer simply answers a few design parameter questions and then clicks the "Finish" button to implement leading-edge functionality in a design. Advanced I/O standards such as GTL+, AGP, SSTL-3 Class I and many other I/O standards can be enabled by choosing a pin, choosing a standard from a drop-down list, then clicking the "Add" button.

Enhanced Timing Analysis Capabilities

As design complexity increases, the need for advanced timing analysis capabilities grows more critical. The Quartus software features an enhanced static timing analyzer to address this need. The Quartus Timing Analyzer measures delays of every path in a design and reports the maximum speed that the system clocks can run for a design. The Timing Analyzer can also report the allowable phase between related clocks, set up and hold times for all input registers, and clock-to-output times of all output registers.

The Quartus Timing Analyzer is automatically invoked during design compilation, removing the need to launch a separate manual timing analysis at the end of each successful compilation. To further simplify the process, all timing analysis results can be directly accessed via the Timing Analyses folder in the Compilation Report window. Through the report window, the designer has immediate access to the timing analysis results.

Designers can perform timing analysis on designs with single and multiple clocks, as well as with multicycle paths. The Quartus software also has the ability to break down individual timing results into several levels including delay path, clock path, and setup time. Furthermore, these paths can be located in the Floorplan View and in the HDL source code to facilitate the design optimization process.

Scripting with Tcl

The Quartus software allows designers to develop and run scripts in Tcl to perform a wide range of simple or complex functions. Using Tcl scripts in the Quartus software to automate compilation flows, perform common sequences of tasks, or even automate complex simulation test benches can save valuable design time. Tcl can also be used to create custom interfaces to third-party tools. Many engineers are already familiar with this standard scripting language, and Quartus help files provide details on how to use Tcl with the Quartus application program interface (API) for immediate productivity.

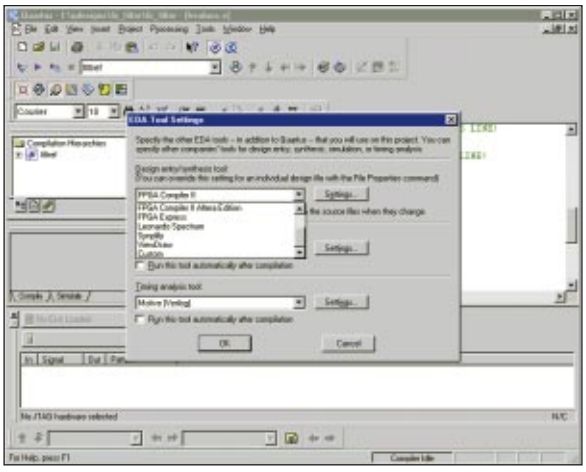
Collaborative Work Environment

As design densities enter the million-gate range, multiple engineers may work on a single project without interrupting the design cycle. The Quartus software uses a centralized object-oriented database that can be accessed by different engineers across a network. The Quartus software is also capable of integrating with standard revision control systems—such as RCS and PVCS—or custom revision control systems to track and prevent simultaneous changes to designs.

NativeLink Integration with Major Design Tools

Digital system design flows typically require the use of several different EDA tools to perform tasks from design entry and synthesis to verification and programming. These tools require efficient transfer of information. NativeLink integration facilitates the seamless transfer of information between the Quartus software and other EDA tools to enhance the overall productivity of the designer's EDA tool suite.

Figure 4. NativeLink Integration Provides Seamless Interface with Major EDA Tools



Altera has worked very closely with major EDA vendors to develop the best interface any PLD software has to offer. Altera opened the Quartus interface to various EDA partners to enable them to provide unmatched levels of integration. NativeLink integration provides a truly seamless interface to major EDA software tools to support existing design flows, eliminating the need to learn new design tools.

Improved Quality of Results

The NativeLink flow allows designers to use Quartus pre-place-and-route estimates in third-party EDA tools to optimize synthesis strategies, thereby improving the quality of synthesis results. Most third-party EDA tools can also be configured to launch the Quartus software to perform the place-and-route of a design immediately after synthesis. Designers are not required to learn a new software package; the Quartus software interfaces with a variety of standard EDA tools so the designer can use familiar tools. The Quartus software can perform synthesis and simulation by launching the third-party EDA tool specified by the designer, and each tool displays processing messages from the other tool.

Through NativeLink integration, third-party synthesis tools have an unprecedented level of control over the final mapping of designs targeting Altera devices. NativeLink integration with the Quartus software allows third-party EDA synthesis tools to directly map designs to device logic elements. Since it is not necessary to re-synthesize the design for the place-and-route process in the Quartus software, designers can fully realize the benefits of their third-party EDA synthesis tool capabilities.

Error-Location Capability

While most interfaces allow design information to be passed from one tool to another, they provide little or no interaction between tools. Using the Quartus software, error location and correction is easier than ever before. The Quartus software can identify the source of errors in the EDA tool's source design file, and the errors can be corrected directly in the EDA tool.

Internet-Based Support

The Quartus software is engineered with the latest Internet browser. Designers with Internet access can use Quartus software to connect directly to Altera's web site—including the ATLAS® Solutions database—from within the software. This direct access provides users with immediate solutions, hints, and workarounds to issues they may face during the design cycle.

Customers can also submit service requests directly to Altera Applications and monitor their progress via the Internet while in the Quartus software. The design files and user configuration details can be prepared for transfer to Altera automatically. This feature ensures

that the Altera Applications engineer working on the issue can accurately duplicate the design environment. With this feature, Altera effectively becomes an active member of the design team.

Automatic notifications of service packs, new device support, and online help updates are communicated on a daily basis by the Quartus software. Users are prompted to download or install the latest software upgrades, ensuring access to current devices and features.

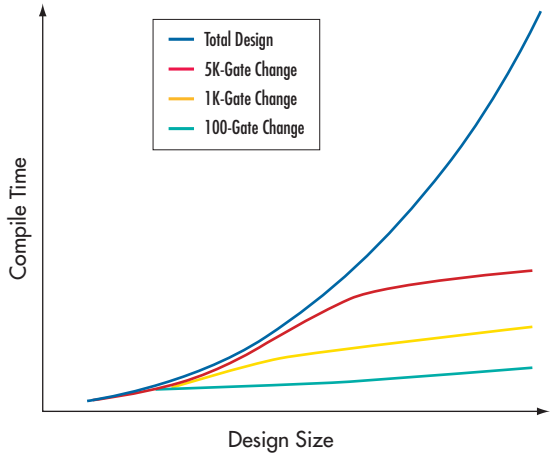
Designing for the Future

The Quartus development system is designed to be the leading-edge development tool for multi-million-gate design. To enhance its flexibility and performance, innovative features are constantly being added and refined.

Shortened Compilation Times with the nSTEP Compiler & CoreSyn Synthesis

Complex designs often require several design iterations to achieve the desired results. Before Quartus software, designers needed to perform a full compilation with each iteration before they could examine results. In future versions of the Quartus software, the nSTEP™ Compiler will allow designers to make changes and obtain results without running a full compilation. The Quartus software will compile only the portions of the design that have changed. This powerful feature will significantly shorten compile times, as shown in Figure 5, and maintain placement and timing in portions of the design that are unchanged.

Figure 5. nSTEP Compilation Enables Faster Compile Times



The nSTEP Compiler will analyze the design and then partition functions into the appropriate type of look-up table (LUT)-based logic element, product-term-based macrocell, or embedded memory logic block within the APEX architecture. Using Altera's CoreSyn™ synthesis capability, the nSTEP Compiler will then invoke the appropriate synthesis technology to optimize the logic for that architecture. This high level of control will allow the designer to achieve optimal results.

Team Design with BlockLock Capability

The BlockLock™ feature will provide the capability to design in a custom logic module or pre-verified intellectual property core, make pin and timing assignments, simulate the block to verify functional and timing performance, and then lock down the block to guarantee its placement and performance even after additional logic blocks are added to the design. BlockLock capability will allow teams of engineers to work on a design, enabling each designer to be responsible for individual blocks of logic in a multi-million gate PLD. Designers will even be able to reserve extra logic around a block for additional features or changes that may be needed as the design progresses or marketing requirements change. After all the blocks are designed and performance for each block is locked down, the system designer can integrate the individual blocks into a total system and verify the system performance without having to re-verify the performance of each individual block.

APEX: A Revolutionary Embedded Architecture

The Quartus development software supports the APEX device family, Altera's high-performance, high-density, embedded PLD family. APEX devices are designed for system-level integration and integrate LUT logic, product-term logic, and memory in a single device with densities up to 2.5 million maximum system gates. This revolutionary architecture, called MultiCore™ architecture, combines and enhances the strengths of the FLEX® 10K, FLEX 6000, and MAX® 7000 architectures to provide an efficient, high-performance solution for system-level applications.

APEX devices are made up of MegaLAB™ blocks which contain logic array blocks (LABs) and an advanced embedded structure called an embedded system block (ESB). The ESB can be configured as product-term logic, LUT logic, dual-port RAM, ROM, or content-addressable memory (CAM). APEX devices offer enhanced ClockLock™, ClockBoost™, and ClockShift™ circuitry, and support multiple I/O interfacing standards including LVCMOS and LVTTL, GTL+, SSTL-3, SSTL-2, HSTL, CTT, AGP, LVPECL, as well as LVDS with performance up to 622 Mbits per second. APEX devices are also the first PLDs to be PCI and PCI-X compliant.

ACEX: Optimized for Low Cost & High Performance

Altera's new ACEX™ device families consist of mid-density-range LUT-based PLDs, optimized to provide low cost and high performance for price-sensitive volume applications. Key ACEX applications include products such as cable and xDSL modems, low-cost switches, and routers.

The 1.8-V ACEX 2K family features devices based upon 0.18-µm process technology, ranging from 20,000 to 150,000 typical gates. ACEX 2K devices are fully 64-bit, 66-MHz PCI and PCI-X compliant, and feature embedded dual-port RAM and advanced packaging technologies. ACEX 2K devices feature support for PLL circuitry, capable of driving two separate ClockLock- and ClockBoost-generated signals for extensive clock management capability. In addition, ACEX 2K devices support a wide range of specialized I/O standards that enable effective high-speed board-level communications.

The Convenience of Subscription

Customers can purchase development tool subscriptions from Altera for 12-month periods. With the Altera Development Tools Subscription Program, customers receive the latest version of the Quartus and MAX+PLUS® II software to support Altera's complete range of programmable logic devices. Customers also have the option to use the world-class HDL synthesis and simulation software included with the subscription. Customers can license fully-functional, Altera-specific versions of Synopsys FPGA Express for VHDL and Verilog synthesis, Exemplar Logic LeonardoSpectrum software for VHDL or Verilog synthesis, and Model Technology ModelSim HDL simulation software for VHDL or Verilog simulation.

With the Altera Subscription Program, customers receive periodic updates of all licensed software for 12 months. Updates include support for the latest Altera PLDs, new software features, performance enhancements, and the most current on-line and printed documentation. At the end of the 12-month period, customers must purchase a renewal subscription in order to continue receiving software updates. If customers choose not to renew the subscription, the versions of Altera software already received will continue to work.

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