Customer Application

Altera Delivers Speed for GigaNet ATM Protocol Engine

Industry:	Communications
End Product:	Intel Paragon™ Supercomputer
Design Application:	ATM OC-12c Protocol Engine™
Altera Products:	EPF81188A, EPM7032, EPM7128E, EPM7160E, EPM7192E, EPM7256E, MAX+PLUS II

Designing for Speed & Flexibility

GigaNet develops high-performance ATM-based protocol engines that interface to supercomputers. The OC-12c Protocol Engine was designed for use in the Intel Paragon supercomputer to allow customers to communicate with ATM networks at OC-12c, OC-48, and OC-192 rates. Speed for this design was critical since the interface needed to run at OC-12c rates under worst-case conditions. The designers also wanted the flexibility to scale the design to OC-192 rates through parallel implementations.

Choosing a Programmable Logic Vendor

The design team implemented much of the design in programmable logic to meet flexibility and time-to-market demands. They chose the specific devices based on speed and density requirements.

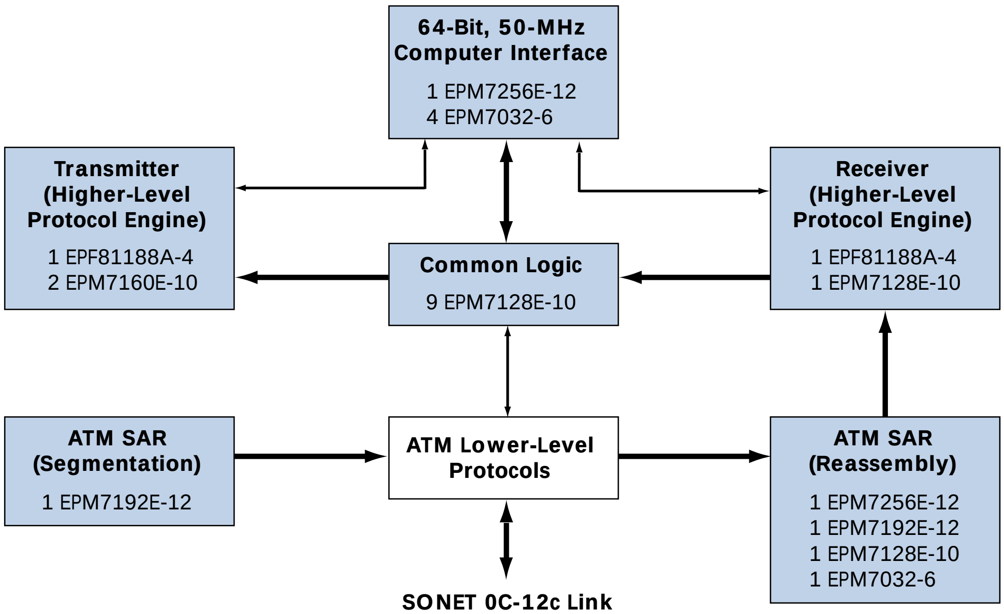
"We needed a register-intensive product for calculating TCP/IP checksums at 400 Mbytes per second and we needed a macrocell architecture to incorporate the wide state machines and deep pipelines of the higher-level protocol algorithms," says David Follett, the architect of the project.

In addition, having a single programmable logic vendor was essential because "we needed a single toolset that was well integrated with our Viewlogic WorkView Plus board-level simulator," says Follett.

Altera Provides the Answer

All programmable logic vendors were considered during the selection process, but Altera was the only supplier that met GigaNet's speed, density, and tool requirements. The final

GigaNet ATM OC-12c Protocol Engine



In the ATM OC-12c Protocol Engine, the transmit side processes the data received from the computer, segments it into 53-byte ATM cells, and sends it to the network link. The receiver then reassembles the ATM cells received from the network link, processes the data, and sends it on to the computer.

design incorporated 24 Altera devices using clock frequencies from 50 to 100 MHz.

"The FLEX 8000 architecture was ideal for implementing the fast checksum with its multiple high-speed adders. Implementing the ATM algorithm at our required speed was particularly tricky due to the large state machines, but MAX 7000 devices helped us meet the challenge," says Follett.

The Benefits of Tool Integration

The GigaNet designers expected to use Altera's MAX+PLUS II software for chip design and some multi-chip functional simulation while using WorkView Plus to verify the larger blocks and the entire board. However, they ended up using the MAX+PLUS II Simulator extensively for functional and timing simulation because it is so well integrated with the MAX+PLUS II design entry tools.

"The integration of the tools is the best I've seen," says Follett. "The timing simulator provided very accurate information that allowed us to modify the design and obtain our mandated speed."

The multi-chip simulation capability also allowed the GigaNet team to simulate one functional block with nine chips and verify both functionality and timing parameters. The timing information from MAX+PLUS II was then imported into WorkView Plus for board-level simulation.

A Winning Solution

FLEX 8000 and MAX 7000 devices, together with MAX+PLUS II software, provided the winning solution for GigaNet.

"Altera was the only supplier that met our demand for high density, blazing speed, and well-integrated tools. And MAX+PLUS II enabled us to verify functionality, integrate many of the elements, and validate the aggressive speed requirements."

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