AMPP Catalog
June 1998

About this Catalog

June 1998

AMPP Catalog Contents

This catalog provides information on Altera Megafunction Partners Program (AMPP℠) partners and provides descriptions of megafunctions from each AMPP partner. The information in this catalog is current as of the printing date, but megafunction specifications and availability are subject to change. For the most current information, refer to the Altera® world-wide web site at **http://www.altera.com**.

Each megafunction description includes a list of key features, a functional description with information on applicable standards compliance, and a table with fitting and performance specifications. Megafunctions are grouped into the following functional areas:

- Bus and Interface
- Processor and Peripheral
- Telecommunication and Data Communication (Telecom and Datacom)
- Digital Signal Processing (DSP)

For additional details on megafunctions, including availability, pricing, and delivery terms, designers should contact the AMPP partner directly.

Each AMPP partner profile contains contact, background, and historical information on the partner company. The partner profile may also include a list of available megafunctions and a description of additional services.

How to Contact Altera

For additional information about Altera products, consult the sources shown in Table 1. For information on how to contact an Altera sales office, see "Altera Sales Offices" in this catalog.

Table 1. Contact Information

Information Type	Access	U.S. & Canada	All Other Locations
Literature	Altera Express	(800) 5-ALTERA	(408) 544-7850
	Altera Literature Services	(888) 3-ALTERA lit_req@altera.com	(888) 3-ALTERA lit_req@altera.com
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
	Fax	(408) 544-8186	(408) 544-7606
Technical Support	Telephone Hotline (6:00 a.m. to 6:00 p.m. Pacific Time)	(800) 800-EPLD	(408) 544-7000
	Fax	(408) 544-6401	(408) 544-6401
	Electronic Mail	sos@altera.com	sos@altera.com
	FTP Site	ftp.altera.com	ftp.altera.com
General Product Information	Telephone	(408) 544-7104	(408) 544-7104
	World-Wide Web	http://www.altera.com	http://www.altera.com

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Introduction

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Overview

As programmable logic device (PLD) density continues to increase, Altera recognizes that designers require design tools that will improve their productivity and allow them to keep pace with the increasing capacity of PLDs. A design methodology that uses pre-built megafunctions offers this productivity increase. The successful development of megafunctions requires close cooperation between the intellectual property (IP) developers and PLD vendors. The Altera Megafunction Partners Program (AMPP℠) program, established in August 1995, was created to bring the advantages of megafunctions to users of Altera® PLDs.

The AMPP program identifies megafunction developers, trains them on Altera device architectures and tools, and promotes the partners' megafunctions through Altera's broad marketing and sales channel. Altera does not develop nor participate in the licensing or delivery of AMPP megafunctions; the actual delivery and licensing of megafunctions is coordinated between the designer and the AMPP partner.

Altera carefully selects each AMPP partner and works with each partner to promote megafunctions. By recruiting a diverse group of participants, Altera provides the widest range of megafunctions while minimizing product overlapping. An AMPP partner must meet at least two criteria:

- Have the ability to respond to Altera's world-wide business
- Have a roadmap of future megafunctions with a specific application focus

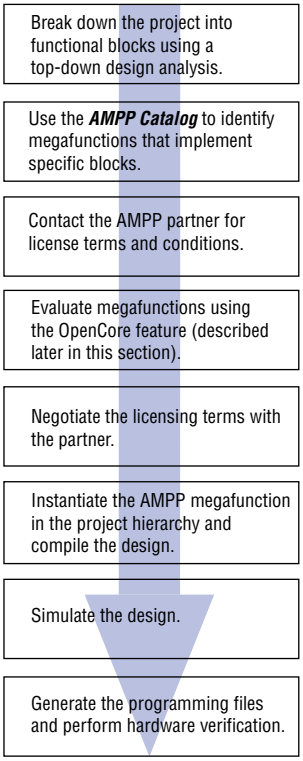
AMPP partners attend training sessions provided by Altera, and are encouraged to continue training. Partners are updated on the software tools used to optimize their megafunctions for specific Altera device families. Partners also receive encryption software, which protects the ownership of their megafunctions during the customer evaluation phase. AMPP partners and the Altera sales staff work closely together to establish relationships with customers and to provide timely resources during megafunction evaluation and implementation.

About AMPP Megafunctions

AMPP megafunctions are optimized for specific Altera device architectures. The optimization process usually involves setting compilation and synthesis options to maximize density and performance. AMPP megafunctions are then refined until they are as fast and small as possible.

Figure 1 illustrates the typical process for evaluating, licensing, and using AMPP megafunctions.

Figure 1. Using AMPP Megafunctions



AMPP megafunctions can also be programmed and/or customized. Programmable megafunctions can be configured "on-the-fly," which changes behavior or specific function settings (e.g., a shift register with a dynamically adjustable maximum depth). Customizable megafunctions are modified by AMPP partners to create new versions. Megafunctions that are customized may be included in the quoted license fee, but are typically subject to additional modification or consulting fees.

Parameterized Megafunctions via MegaWizard Plug-Ins

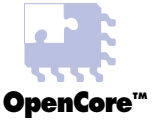
Altera is the first PLD vendor to offer customers the capability to alter key megafunction parameters without restricting the end user's design flow. MegaWizard™ Plug-Ins allow users to customize megafunctions to meet specific design objectives, greatly reducing the time spent specifying a custom function. Because MegaWizard Plug-Ins are a recent innovation, AMPP partners are still in the process of creating plug-ins for many of their megafunctions; check with the AMPP partner directly for availability.

Available Formats

All AMPP megafunctions are available in post-synthesis Altera Hardware Description Language (AHDL) format, a fully minimized and optimized netlist that can be used without risk of changes during design processing. Although VHDL and Verilog HDL files are available from most partners, a source code license is usually more expensive than a post-synthesis netlist license because the source code versions represent more intrinsic value.

Altera recommends using post-synthesis netlists to avoid synthesis variation issues during design processing. This process ensures that engineering effort is not required to reoptimize the behavioral source code.

OpenCore Feature



Altera's MAX+PLUS® II software provides the OpenCore™ feature, which allows designers to evaluate megafunctions prior to licensing. The OpenCore feature allows designers to compile a megafunction and determine its size and speed, but it prevents the designer from generating programming or configuration files. This feature allows AMPP partners to offer OpenCore evaluations without risking their licensing interests.

To receive an OpenCore version of a specific megafunction, contact the AMPP partner directly for an authorization code; the AMPP partner will generate this code based on your MAX+PLUS II PC or UNIX workstation identification.

Megafunctions in the Design Flow

AMPP megafunctions are intended as "drop-in" design elements for all design flows supported by the MAX+PLUS II software. Although the megafunctions are developed as stand-alone functions, they can be integrated with other megafunctions and logic in a top-down design methodology. The ideal design flow assesses a project's functional block requirements and assigns megafunctions to implement different portions of a system. Once the megafunction blocks are defined, designers can focus on design elements that are proprietary or cannot be implemented with megafunctions. For design flows that use only the MAX+PLUS II software, the designer can use the megafunction in a Graphic Design File (**.gdf**), AHDL Text Design File (**.tdf**), Verilog Design File (**.v**), or VHDL Design File (**.vhd**).

AMPP megafunction support extends to third-party design flows that are currently supported by Altera tools. For design flows that use standard EDA tools in addition to the MAX+PLUS II software, designers can instantiate AMPP megafunctions in a design by specifying the cell and port names in an HDL design file. During design processing, the EDA tool will pass the megafunction's cell and port names into the EDIF netlist file. The EDA tool does not process beyond the name level during compilation; the MAX+PLUS II software replaces the cell name with the actual functional specification. Once the megafunction is part of a MAX+PLUS II project hierarchy, the designer must specify three synthesis options before the megafunction can be processed by the MAX+PLUS II software:

- Assign the megafunction to a clique, which ensures that the placement of the megafunction is optimized for high performance.
- Assign the WYSIWYG logic synthesis style, which instructs the MAX+PLUS II software to turn off logic synthesis when it processes the megafunction.
- Apply any top-level timing assignments provided by the AMPP partner to the hierarchy before design processing.

For information on cliques, logic synthesis styles, and instantiating functions, go to MAX+PLUS II Help.

During compilation, the MAX+PLUS II software recognizes the megafunction as an AMPP megafunction and verifies the megafunction license. The MAX+PLUS II software then completes design processing according to the permissions granted by the AMPP megafunction license.

Performance & Density Specifications

The performance and density specifications in this catalog apply to megafunctions that are compiled as stand-alone designs. Additional logic synthesis may affect the performance or density of a megafunction, particularly when the function is combined with other megafunctions or logic. Megafunctions shipped as post-synthesis AHDL files have minimal performance or density variations, because additional design processing is not required. Megafunctions supplied as behavioral source code files may change in performance or density, depending on the design and the target device. Timing cannot be determined until synthesis and place and route of the final design is complete.

Each AMPP megafunction has a performance metric that provides performance information when the megafunction is compiled as a stand-alone project. The metric is usually a global clock speed or $\mathbf{f_{MAX}}$, but in some cases, other metrics such as a propagation delay or samples/second is given. The global clock setup time (t_{SU}) and global clock-to-output (t_{CO}) delay are also useful parameters. Contact the AMPP partner to determine which additional performance metrics are available for the megafunction.

In general, a global clock frequency is not affected by the I/O delays that route the signal off-chip, whereas the t_{SU} and t_{CO} parameters are directly affected by on-chip and off-chip routing. If a megafunction is integrated with other logic or megafunctions on the same device, the set-up and clock-to-output delays are reduced because off-chip/on-chip delays are not required.

Subsequent versions of the MAX+PLUS II software, megafunction design modifications, or the availability of faster speed-grade devices may affect density or performance characteristics. Contact the AMPP partners for the latest megafunction specifications.

AMPP Megafunction Package Contents

An AMPP megafunction package typically contains the following items (items that accompany every package are highlighted in blue):

- Megafunction license
- Megafunction design file (typically a post-synthesis netlist)
- Symbol File (**.sym**) for use in MAX+PLUS II GDFs
- Include File (**.inc**) for use in MAX+PLUS II TDFs
- VHDL and Verilog HDL instantiation templates
- Megafunction documentation
- Top-level timing assignments
- Help file (typically in HTML)
- Simulation stimulus file(s)

AMPP partners provide different levels of support and documentation. Designers should contact the AMPP partner directly to ensure that appropriate support is provided. Most partners will supply sophisticated simulation information, such as pre-synthesis bus simulation models for use in third-party logic synthesis tools prior to processing in the MAX+PLUS II software.

Licensing AMPP Megafunctions

AMPP megafunctions are licensed directly from AMPP partners. The terms and conditions of each AMPP megafunction license may vary from partner to partner. Each AMPP partner typically specifies the megafunction licensing terms based on the needs of the end user. AMPP megafunction license options may include:

- Duration of the license (e.g., lifetime, 1 year, or 6 months)
- Source-code access
- OpenCore feature

AMPP megafunction licenses are generally limited to Altera PLDs. You should receive written permission before targeting an AMPP megafunction for a non-Altera PLD (e.g., a gate array). Such use of an AMPP megafunction may require an additional license and/or payment to the AMPP partner.

The duration of an AMPP megafunction license typically defines the period of time during which the AMPP megafunction may be compiled as part of a MAX+PLUS II project. Once the programming file for an Altera PLD has been created, AMPP megafunction licenses generally convey unlimited lifetime manufacturing rights. Limitations in the use of the licensed megafunction vary from partner to partner.

To protect the embedded IP, AMPP megafunctions are typically shipped as encrypted files. Although the megafunction design file has a standard filename (e.g., **function.tdf**), the file appears corrupted when opened with a text editor. The encrypted megafunction design file is actually a binary file. Authorization and decryption are handled by the MAX+PLUS II software, using a megafunction authorization code that is generated and supplied by the AMPP partner.

AMPP megafunction licenses use the same authorization process as the MAX+PLUS II software. The MAX+PLUS II software for PCs uses an embedded license system, based on the serial number of the MAX+PLUS II software guard (guard ID). UNIX workstation versions of the MAX+PLUS II software use the FLEXlm license manager and treat each AMPP megafunction as a new MAX+PLUS II feature. UNIX workstation licensing can either be locked or floating node, depending on the licensing partner's policy.

AMPP megafunction licenses are supplied by individual AMPP partners, not by Altera. Altera cannot generate licenses for AMPP megafunctions.

AMPP Megafunction Pricing

Designers should contact the appropriate AMPP partner for a quote or estimate of a megafunction license. To help determine the cost of a megafunction license and to ensure that the megafunction successfully integrates with the end application, be prepared to provide the AMPP partner the following information:

- Relevant megafunction parameters (e.g., bus width, resolution)
- License duration requirements (e.g., lifetime, 6 months)
- Target device architecture (e.g., FLEX® 10K, MAX® 9000 devices)
- Netlist-only or source-code license
- Any requirements for modifications or feature changes
- Any requirements for design migration (e.g., to an ASIC)

Technical Support

AMPP megafunctions are carefully developed by AMPP partners to ensure the highest possible quality. If a problem is traced to a megafunction, the AMPP partner is responsible for resolving the problem.

If a problem arises with integrating the megafunction with other logic, Altera will provide appropriate engineering support.

Warranty

The megafunctions in this catalog, as well as other megafunctions and services available from the AMPP partners, are provided without warranty by Altera. Altera expressly disclaims all warranties, express and implied, with respect to the megafunctions supplied by the AMPP partners, including, but not limited to, implied warranties of merchantability, fitness for a particular purpose, title and non-infringement.

The AMPP partners may offer guarantees or warranties for design performance or functionality; contact individual AMPP partners for details.

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Overview

Implementing a bus interface function that meets design specifications is a challenging task that requires considerable design expertise. Altera Megafunction Partners Program (AMPP℠) partners offer pre-synthesized and pre-verified solutions for standard serial and parallel buses. Using AMPP megafunctions can shorten the development cycle dramatically, not only during the design entry phase using the OpenCore™ feature, but also during the simulation phase with hardware-proven solutions and testbenches. AMPP partners also have the expertise to provide drivers for complex bus protocols such as peripheral component interconnect (PCI), FireWire, and universal serial bus (USB).

Contents

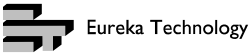
The bus and interface section contains the following functions:

Parallel Bus

Serial Bus

32-Bit PCI Target

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 2107-A112



- Fully compliant with peripheral component interconnect Special Interest Group's (PCI-SIG) ***PCI Local Bus Specification, Revision 2.1***
- Supports zero-wait state burst mode data transfer
- Internal write buffer to maximize data bandwidth
- Optional first-in first-out (FIFO) interface
- 33-MHz operating frequency

General Description

The 32-bit PCI target megafunction provides a user-friendly interface between a target device and a PCI bus. This megafunction is a very compact design that minimizes logic cell count while providing a high-bandwidth data transfer. The megafunction performs all data transfer functions requested by the PCI bus master. To maximize data bandwidth, the megafunction provides an internal write buffer and supports burst mode data transfer. All PCI configuration requests are processed locally by the megafunction.

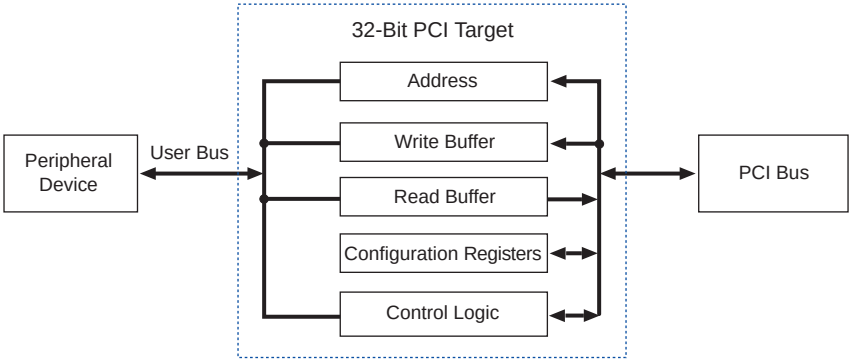
Modifiable Parameters

The megafunction is available in Altera Hardware Description Language (AHDL), Verilog HDL, VHDL, and netlist format. Eureka Technology can customize the megafunction to meet user requirements. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 1 shows the block diagram for the 32-bit PCI target megafunction.

Figure 1. 32-Bit PCI Target Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K10	-3	310	0	33 MHz	Non-burst target design
EPF6016	-2	310	–	33 MHz	Non-burst target design

32-Bit PCI Target

Vendor: PLD Applications
Target Application: Digital signal processing (DSP), high-speed data transfer, bus migration, technology migration
Additional Deliverables: Simulation file, constraint file, development board, user guide, reference design
ID Code: 73E2-1104

- 32-bit, 33-MHz PCI function
- Fully compliant with PCI-SIG ***PCI Local Bus Specification, Revision 2.1***
- Optimized for the Altera FLEX® 10K and FLEX 6000 device architectures
- Fully synchronous design
- Tested on hardware
- Supports full-speed burst up to 132 Mbytes/second
- Provides zero-wait state data transfers
- Medium-speed decoder
- Fully customizable function
- Support for two base address registers (BARs)
- Zero pre-placed or pre-routed logic
- 3 to 5 minute compilation time

General Description

The 32-bit PCI target megafunction is a 32-bit, 33-MHz PCI bus interface that is used for high-speed data transfer applications.

This megafunction provides a simple and flexible interface between the PCI bus and a user-developed back-end design. The megafunction comes with a set of AHDL and VHDL back-end reference designs that designers can customize for their own project. These reference designs include interfaces that use FLEX 10K embedded array blocks (EABs) as synchronous SRAM buffers or FIFO buffers. Another back-end design provides an interface to an external SRAM buffer.

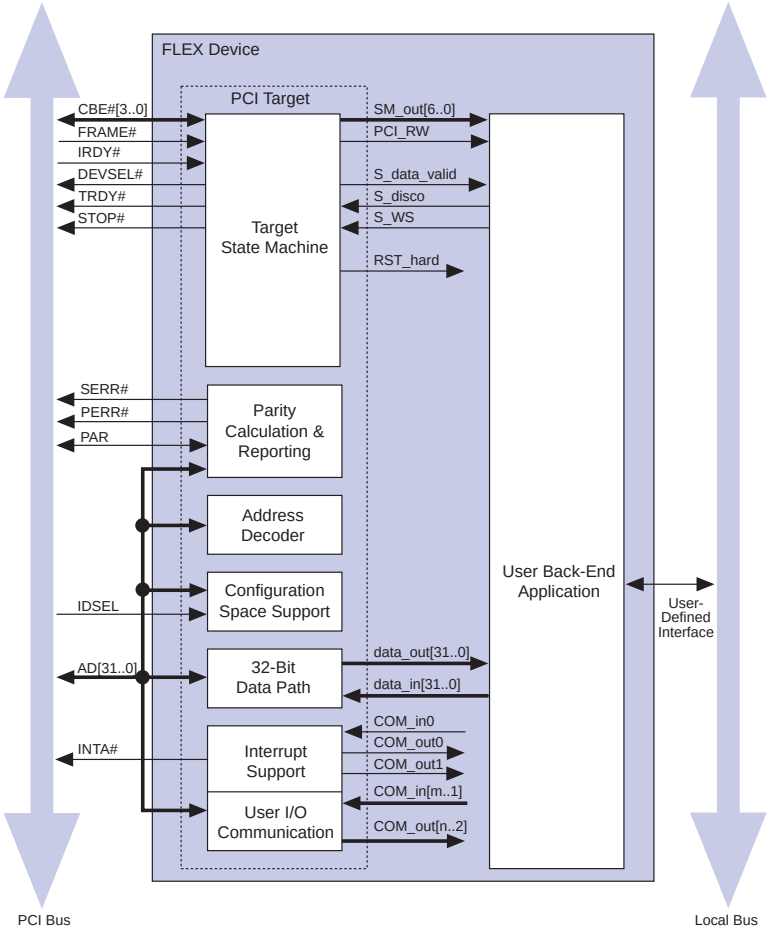
In addition to the required target features, the megafunction handles one interrupt line, supports fast back-to-back accesses, and implements a 32-bit user-configurable generic I/O port. The megafunction can still be customized to support additional user-specified features (e.g., multiple BARs and additional user I/O ports).

This 32-bit PCI target megafunction has been extensively simulated and tested on hardware using PLD Applications' commercialized PCI_GEN02 (FLEX 10K-based) and PCI_GEN6K (FLEX 6000-based) PCI prototyping boards.

Block Diagram

Figure 2 shows the block diagram for the 32-bit PCI target megafunction.

Figure 2. 32-Bit PCI Target Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-2	347	0	60 MHz	Contact PLD Applications
EPF10K30	-1	347	0	91 MHz	Contact PLD Applications
	-3	347	0	40 MHz	Contact PLD Applications
EPF6016	-2	356	–	46 MHz	Contact PLD Applications

32-Bit PCI Master/Target

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 2107-B040

- Fully compliant with PCI-SIG ***PCI Local Bus Specification, Revision 2.1***
- Supports zero-wait state burst data transfer
- Provides bus initiator and target capability
- 33-MHz operating frequency

General Description

The 32-bit PCI master/target megafunction is a flexible interface between a bus master device, such as a direct memory access (DMA) controller or video coprocessor, and the PCI bus. The megafunction supports high bandwidth data transfer up to 133 Mbytes/second. All PCI configuration registers are included in the megafunction, and configuration requests are processed locally by the megafunction.

This megafunction also includes PCI target capability, which is useful for transferring data as a target and for setting up the control register of a bus mastering device.

The megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format.

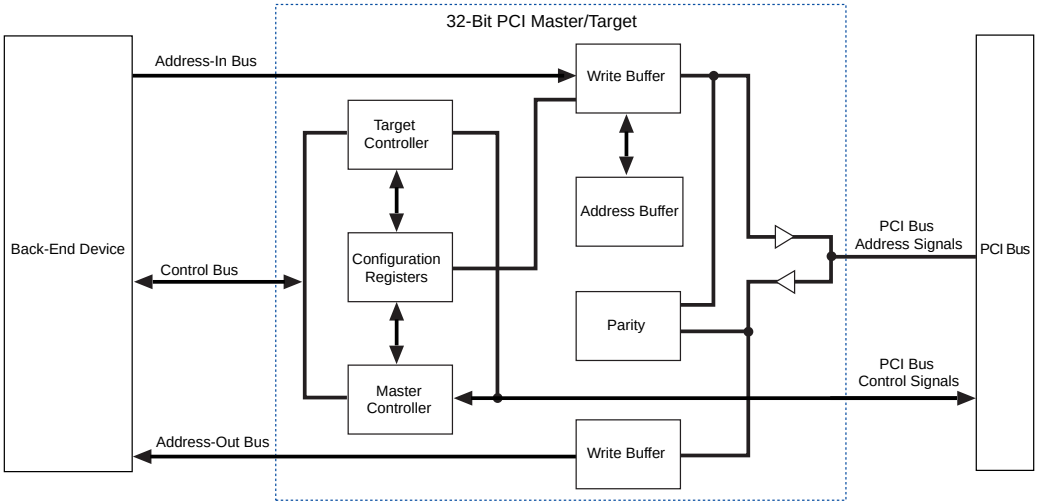
Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 3 shows the block diagram for the 32-bit PCI master/target megafunction.

Figure 3. 32-Bit PCI Master/Target Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EFP10K10	-3	650	0	33 MHz	Contact Eureka Technology
EPF6016	-2	650	–	33 MHz	Contact Eureka Technology

32-Bit PCI Master/Target

Vendor: PLD Applications
Target Application:
DSP, high-speed data transfer, bus migration, technology migration
Additional Deliverables:
Simulation file, constraint file, development board, user guide, reference design
ID Code: 73E2-1204

- 32-bit, 33-MHz PCI function
- Fully compliant with PCI-SIG ***PCI Local Bus Specification, Revision 2.1***
- Optimized for the Altera FLEX 10K and FLEX 6000 device architectures
- Fully synchronous design
- Tested on hardware
- Supports full-speed burst up to 132 Mbytes/second as initiator or target
- Provides zero-wait state data transfers as a master or target
- Automatic reiteration of interrupted transactions
- Supports a dual-mode DMA engine accessible from the PCI side and from the local side
- Medium-speed decoder as a target
- Fully customizable function

General Description

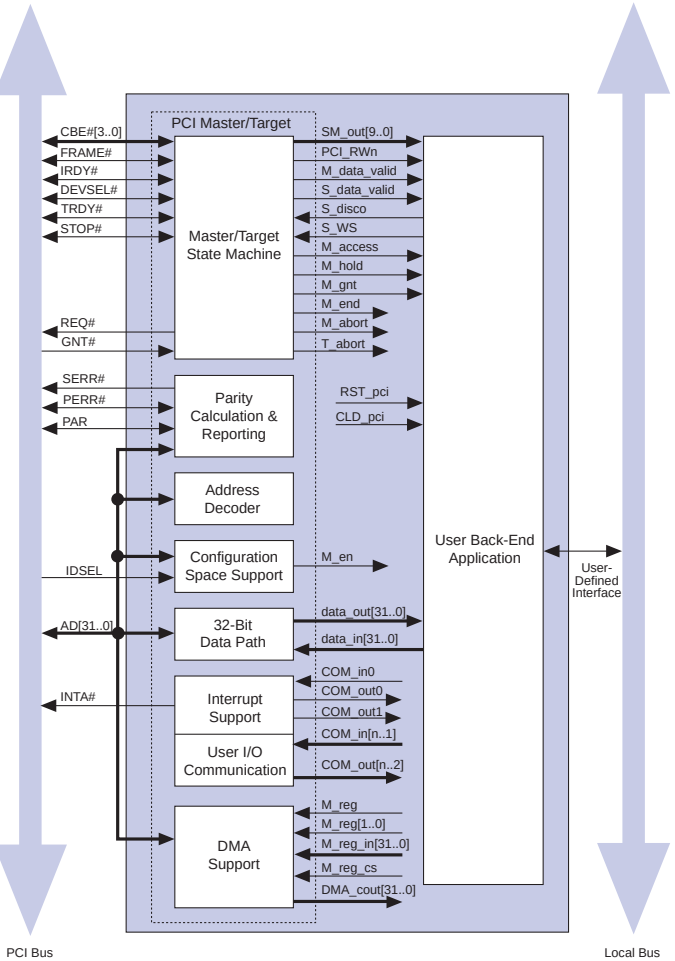
The 32-bit PCI master/target megafunction is a 32-bit, 33-MHz PCI bus interface that is used for high-speed data transfers and real-time computing applications. This megafunction provides a simple and flexible interface between the PCI bus and a user-developed back-end design. The megafunction comes with a set of AHDL and VHDL back-end reference designs that designers can customize for their own project. These reference designs include interfaces that use FLEX 10K EABs as synchronous SRAM buffers or FIFO buffers. Another back-end design provides the interface to an external SRAM buffer.

The 32-bit PCI master/target megafunction is fully parameterizable. In addition to the required master and target features, the megafunction handles one interrupt line, supports fast back-to-back accesses as a target, and implements a 32-bit user-configurable generic I/O port. It also supports all types of master and target transaction terminations, and automatically reiterates interrupted transactions when allowed. The megafunction can still be customized to support specific features (e.g., multiple BARs, additional user I/O ports, additional DMA channels, and optional master features). The megafunction has been extensively simulated and tested on hardware, using PLD Applications' commercialized PCI_GEN02 (FLEX 10K-based) and PCI_GEN6K (FLEX 6000-based) PCI prototyping cards.

Block Diagram

Figure 4 shows the block diagram for the 32-bit PCI master/target megafunction.

Figure 4. 32-Bit PCI Master/Target Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-2	812	0	49 MHz	Contact PLD Applications
EPF10K30	-1	812	0	75 MHz	Contact PLD Applications
	-3	812	0	35 MHz	Contact PLD Applications
EPF10K20	-3	812	0	39 MHz	Contact PLD Applications
EPF6016	-2	821	–	37 MHz	Contact PLD Applications

64-Bit PCI Target

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 2107-C42A

- Fully compliant with PCI-SIG ***PCI Local Bus Specification, Revision 2.1***
- 64-bit PCI bus
- Zero-wait state burst data transfer with internal write buffer
- 33-MHz operating frequency

General Description

The 64-bit PCI target megafunction is designed for interfacing user logic with a 64-bit PCI bus. This megafunction is a very compact design that minimizes logic cell count while offering double the bandwidth performance of a 64-bit bus system.

An internal write buffer is included in this design to support zero-wait state burst transfer and a very long burst length. The megafunction can transfer data up to 266 Mbytes/second. Both 64-bit and 32-bit data transfer rates are supported by this megafunction. All compliant configuration registers are included in the megafunction and all configuration accesses are processed automatically.

The megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with features and customization. Contact Eureka Technology for a logic cell count that is based on user specifications.

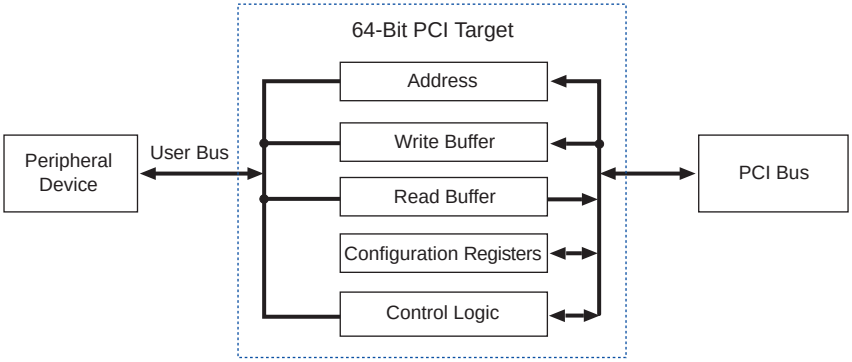
Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 6 shows the block diagram for the 64-bit PCI target megafunction.

Figure 5. 64-Bit PCI Target Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K30	-3	500	0	33 MHz	Contact Eureka Technology
EPF6016	-2	500	–	33 MHz	Contact Eureka Technology

64-Bit PCI Target

Vendor: PLD Applications
Target Application:
DSP, high-speed data transfer applications, bus migration, technology migration
Additional Deliverables:
Simulation file, constraint file, development board, user guide, reference design
ID Code: 73E2-1164

- 64-bit, 33-MHz PCI function
- Fully compliant with PCI-SIG ***PCI Local Bus Specification, Revision 2.1***
- Optimized for the Altera FLEX 10K and FLEX 6000 device architectures
- Fully synchronous design
- Tested on hardware
- Supports full-speed burst up to 266 Mbytes/second
- Provides zero-wait state data transfers
- Medium-speed decoder
- Fully customizable function
- Zero pre-routed or pre-placed logic
- 5-minute typical compilation time

General Description

The 64-bit PCI target megafunction extends the 32-bit PCI target megafunction data path to 64 bits. The megafunction is intended for applications with a 64-bit data path capable of supporting burst transfers up to 266 Mbytes/second.

The 64-bit PCI target megafunction maintains the functionality of the 32-bit PCI target megafunction. In addition, the back-end application can enable/disable support for 64 bits. When 64-bit support is enabled, the megafunction indicates to back-end applications the nature of the transfer (i.e., 32 or 64 bits). When 64-bit support is disabled, the megafunction behaves exactly like the 32-bit version.

Modifiable Parameters

The following megafunction parameters can be modified:

Modifiable Parameters (Part 1 of 2)

Parameter	Description
VENDOR_ID	Vendor identification
DEVICE_ID	Device identifier
REVISION_ID	Revision number
CLASS_CODE	Class code identifier
PREFETCH	Memory attributes
SERR_ENABLE	SERR# control
SPACE_TYPE	Device memory space type (I/O or MEM)

Modifiable Parameters (Part 2 of 2)

Parameter	Description
SPACE_SIZE	Device memory space size
MEM_LOCATE	Device memory space location
COM_IN	User-configurable input port size
COM_OUT	User-configurable output port size

Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K50V	-1	440	0	63 MHz	Contact PLD Applications
EPF10K30	-1	440	0	98 MHz	Contact PLD Applications
	-3	440	0	39 MHz	Contact PLD Applications
EPF10K20	-3	440	0	49 MHz	Contact PLD Applications
EPF6024	-2	440	–	63 MHz	Contact PLD Applications
EPF6016	-2	440	–	49 MHz	Contact PLD Applications

64-Bit PCI Master/Target

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 2107-C061

- Fully compliant with PCI-SIG ***PCI Local Bus Specification, Revision 2.1***
- 64-bit PCI bus
- Zero-wait state burst data transfer
- Includes both bus master and bus target functions

General Description

The 64-bit PCI bus master/target megafunction interfaces bus mastering devices, such as DMA controllers or video coprocessors, to the PCI bus. It processes all data requests from the bus mastering device and translates them into PCI bus requests.

This megafunction is designed for a 64-bit PCI bus system, which doubles the data bandwidth of a 32-bit PCI system. It supports zero-wait state burst transfers and a very long burst length. The megafunction supports up to a 266 Mbytes/second data transfer rate, and both 64-bit and 32-bit data transfers.

The 64-bit PCI master/target megafunction contains the functions of a bus master and a bus target. The device data and status can be accessed as a PCI master or target. All compliant configuration registers are included in the megafunction and all configuration accesses are processed automatically. This megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format.

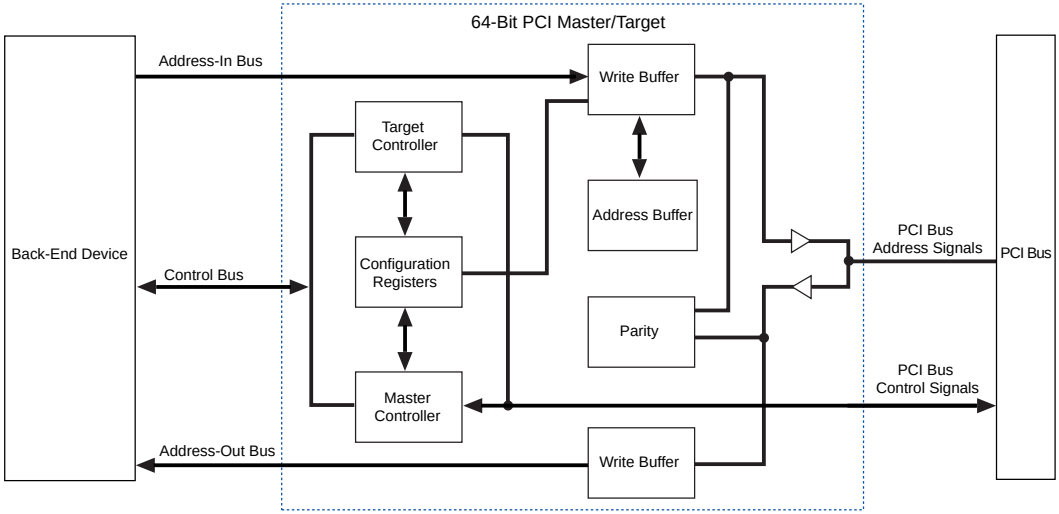
Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements.

Block Diagram

Figure 6 shows the block diagram for the 64-bit PCI bus master/target megafunction.

Figure 6. 64-Bit PCI Master/Target Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K30	-2	1,050	0	33 MHz	Contact Eureka Technology
EPF6016	-3	1,050	–	33 MHz	Contact Eureka Technology

64-Bit PCI Master/Target

Vendor: PLD Applications
Target Application:
DSP, high-speed data transfer, bus migration, technology migration
Additional Deliverables:
Simulation file, constraint file, development board, user guide, reference design
ID Code: 73E2-1264

- 64-bit, 33-MHz function
- Fully compliant with PCI-SIG ***PCI Local Bus Specification, Revision 2.1***
- Optimized for the FLEX 10K and FLEX 6000 device architectures
- Fully synchronous design
- Tested in hardware
- Supports full-speed burst up to 266 Mbytes/second as initiator or target
- Provides zero-wait state data transfers as an initiator or target
- Automatic reiteration of interrupted transactions
- Supports a dual-mode DMA engine accessible from the PCI side and from the local side
- Medium-speed decoder as a target
- Fully customizable megafunction

General Description

The 64-bit PCI master/target megafunction extends the 32-bit PCI master/target megafunction data path to 64 bits. The megafunction is intended for applications with a 64-bit data path capable of supporting burst transfers up to 266 Mbytes/second.

The 64-bit PCI master/target megafunction maintains the functionality of the 32-bit PCI master/target megafunction. In addition, the back-end application can enable or disable the support for 64 bits. When 64-bit support is enabled, the megafunction indicates to the back-end application whether the data transfer is 32 bits or 64 bits. When 64-bit support is disabled, the megafunction behaves exactly like the 32-bit version.

Modifiable Parameters

The following megafunction parameters can be modified:

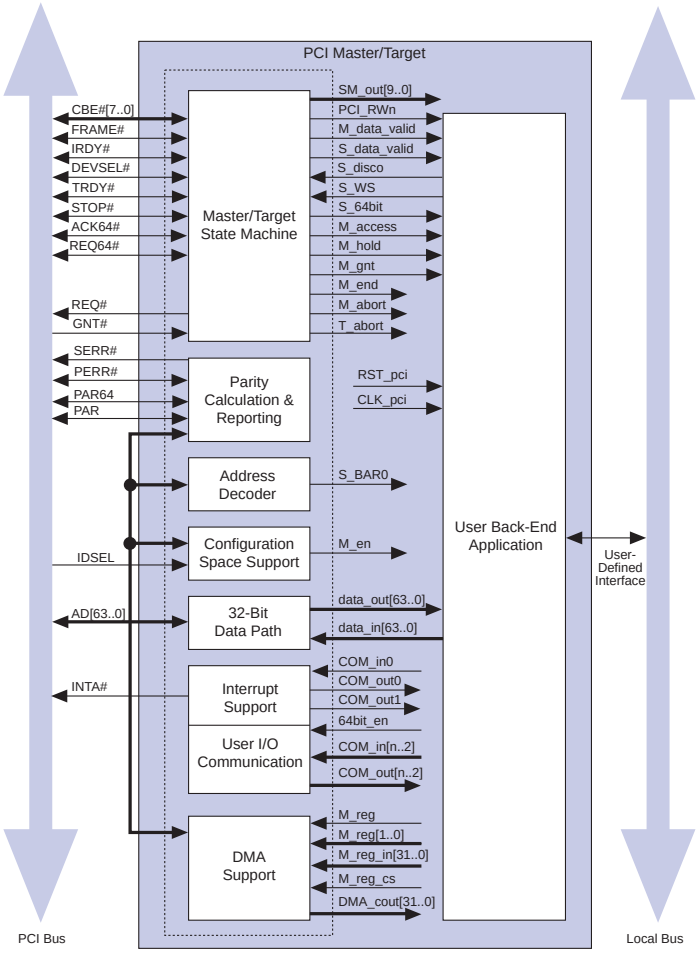
Modifiable Parameters

Parameter	Description
VENDOR_ID	Vendor identifier
DEVICE_ID	Device identifier
REVISION_ID	Revision number
CLASS_CODE	Class code identifier
MIN_GNT	Minimum grant time
MAX_LATENCY	Maximum latency time
PREFETCH	Memory attributes
SERR_ENABLE	SERR# control
SPACE_TYPE	Device memory space type (I/O or MEM)
SPACE_SIZE	Device memory space size
MEM_LOCATE	Device memory space location
COM_IN	User configurable input port size
COM_OUT	User configurable output port size
STATISTIC_REG	Optional statistic register

Block Diagram

Figure 7 shows the block diagram for the 64-bit PCI master/target megafunction.

Figure 7. 64-Bit PCI Master/Target Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-2	915	0	44 MHz	Contact PLD Applications
EPF10K30A	-1	915	0	62 MHz	Contact PLD Applications
EPF10K30	-3	915	0	35 MHz	Contact PLD Applications
EPF10K20	-3	915	0	37 MHz	Contact PLD Applications
EPF6016	-2	915	–	37 MHz	Contact PLD Applications

IEEE 1284 Parallel Slave Interface

Vendor: SIS Microelectronics
Target Application: Asynchronous parallel communications
Additional Deliverables: Simulation file
ID Code: 7D0E-1284

- Bidirectional interface between host computers and peripheral devices
- Uses standard parallel port found on many computer systems
- Fully tested, includes a complete test suite
- Configurable for compatible mode timing of nACK and BUSY ports
- Asserts interrupt or DMA requests when the transmit buffer is empty or the receive buffer contains data

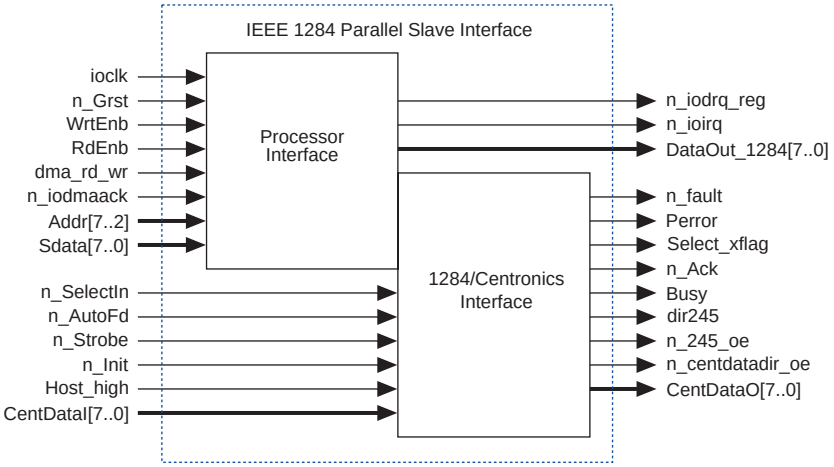
General Description

The IEEE 1284 parallel slave interface megafunction is an interface for fully interlocked, asynchronous bidirectional parallel communications between host computers and peripherals. The megafunction is compatible with the 8-bit IEEE 1284 and Centronics parallel port (printer) interfaces, and it can read data from and write data to the parallel printer port interface. It supports five operational modes: forward compatibility mode, extended capabilities port (ECP) mode with forward-only run-length encoding (RLE), ECP mode (forward and reverse), reverse nibble mode, and request device ID using nibble mode (reverse mode).

Block Diagram

Figure 8 shows the block diagram for the IEEE 1284 parallel slave interface megafunction.

Figure 8. IEEE 1284 Parallel Slave Interface Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30	-3	1,350	0	33 MHz	Contact SIS Microelectronics
EPF6016	-2	910	–	27 MHz	Contact SIS Microelectronics

PCI Host Bridge

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 1207-D410

- Fully compliant with PCI-SIG ***PCI Local Bus Specification, Revision 2.1***
- Connects the host CPU to the PCI bus to initiate PCI data transfers
- Supports zero-wait state burst data transfer
- Initiates PCI configuration access

General Description

The PCI host bridge megafunction provides an interface between the host CPU and the PCI bus. It allows the host CPU to access target devices residing on the PCI bus. The megafunction initiates PCI data read and write transfers upon request from the CPU.

The host bridge megafunction contains the functions necessary to initiate PCI data transfers. In addition, the megafunction is capable of initiating PCI configuration accesses. Configuration cycles are used by the host CPU to set up all PCI devices and to obtain device status. The megafunction supports both the standard configuration mechanism and user-specific configuration mechanisms.

The PCI host bridge megafunction is designed for very high bandwidth data transfer. Zero-wait state bursting and write buffering are supported. The megafunction handles data retry and automatically restarts PCI access upon retry. The PCI host bridge megafunction interfaces with many different types of CPUs, including big endian and small endian machines (e.g., *x*86 and all CPUs from the PowerPC family, including the 60*x*, 740/50, and 860). Through a generic internal bus, the megafunction can interface with virtually any available CPU.

This megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with customization and with feature changes. Contact Eureka Technology directly for a logic cell count that is based on user specifications.

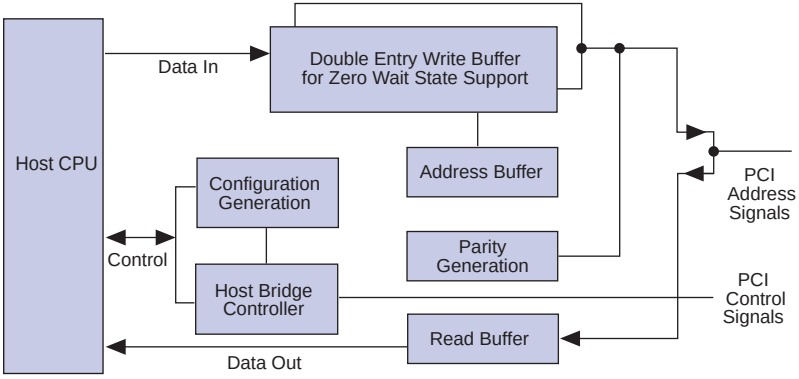
Modifiable Parameters

Eureka Technology can customize the design according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 9 shows the block diagram for the PCI host bridge megafunction.

Figure 9. PCI Host Bridge Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EFP10K10	-3	500	0	33 MHz	Contact Eureka Technology
EPF6016	-2	500	–	33 MHz	Contact Eureka Technology

PowerPC Bus Master

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 1207

- Compatible with all PowerPC bus architectures
- Interfaces with bus mastering or bus snooping devices such as DMA controllers
- Supports address pipelining and separate address and data tenure

General Description

The PowerPC bus master megafunction is a bus master that executes bus transactions on the PowerPC host bus. A simple and efficient user interface allows the user logic to reside directly on the PowerPC bus for high-performance data transfer. Together with the PowerPC bus slave, PowerPC bus arbiter, and PCI host bridge megafunctions, this megafunction provides the complete system core logic function of a PowerPC-based system.

To maximize system performance, the PowerPC bus master megafunction supports advanced features of the PowerPC bus such as address pipelining, address retry, bus parking, and separate arbitration for the address and data buses. This megafunction also supports both single beat and burst data transfers, and it allows address pipelining with two outstanding memory accesses.

The megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with customization and with feature changes. Contact Eureka Technology directly for a logic cell count that is based on user specifications.

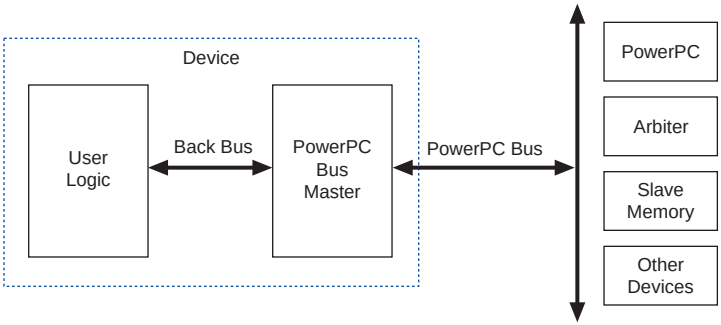
Modifiable Parameters

Eureka Technology can customize the megafunction according to specific user requirements, such as adding pipelining or using either snoop-only or regular data transfer. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 10 shows the block diagram for the PowerPC bus master megafunction.

Figure 10. PowerPC Bus Master Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EFP10K10	-3	160	0	50 MHz	160: With snoop only and pipelining 320: With regular data transfer and pipelining
EPF6016	-2	160	–	50 MHz	
EPM7128	-7	80	–	66 MHz	Contact Eureka Technology

PowerPC Bus Slave

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Simulation files, test vectors, top-level design template, training
ID Code: 1207-0108

- Compatible with all PowerPC bus architectures
- Interfaces with SRAM, SBRAM, FLASH, and user local buses
- Supports data bursting with standard asynchronous SRAM
- Supports address pipelining and separate address and data tenure

General Description

The PowerPC bus slave megafunction is a multi-function interface between the PowerPC bus and user devices such as asynchronous SRAM, synchronous burst SRAM, FLASH, and user local buses. Together with the PowerPC bus master, PowerPC bus arbiter, and PCI host bridge megafunctions, this megafunction provides the complete system core logic function of a PowerPC-based system.

To maximize system performance, the megafunction supports advanced features of the PowerPC bus such as address pipelining, address retry, bus parking, and separate arbitration for the address and data buses. The megafunction also supports both single beat and burst data transfer, and it allows address pipelining with two outstanding memory accesses.

The megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with customization and feature changes. Contact Eureka Technology for a logic cell count that is based on user specifications.

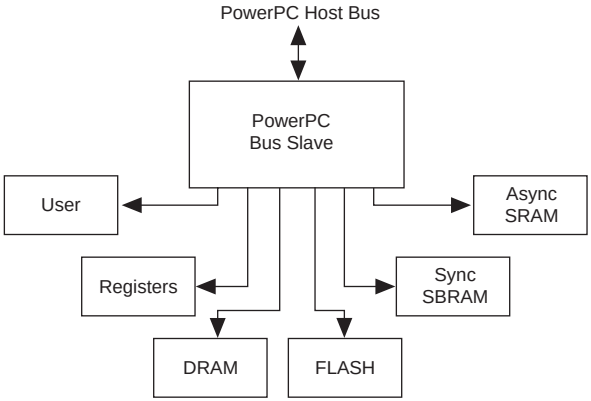
Modifiable Parameters

Eureka Technology can customize the megafunction according to specific user requirements, such as 32- or 64-bit data, pipelining, type of back-end device, adren mapping, and amount of memory mapped by the slave. Contact Eureka Technology or visit their web site for more information.

Block Diagram

Figure 11 shows the block diagram for the PowerPC bus slave megafunction.

Figure 11. PowerPC Bus Slave Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EFP10K10	-3	170	0	50 MHz	32-bit data, pipelined, back-end burst, and two memory spaces
EPF6016	-2	170	–	50 MHz	

CAN Bus

Vendor: SICAN Microelectronics
Target Application: Automotive electronics, home automation, simple sensor/actuator systems
Additional Deliverables: Simulation file, user guide
ID Code: 18CD-47A4

- Compatible with ***CAN Specification, Revision 2.0B*** passive/active
- Completely synchronous flipflop design
- Self-test mode
- Readable error counters
- Data transfer rate up to 1 Mbit/second
- Cycle frequency of 12 MHz

General Description

The Controller Area Network (CAN) bus megafunction fulfills all protocol functions according to ***CAN Specification, Revision 2.0B***, including extended functionality (***CAN Specification, Revision 2.0B*** active). The CAN bus megafunction incorporates all the features required by ***CAN Specification Revision 2.0***, including error handling capabilities, stuff bit generation, cyclic redundancy code (CRC), and multiple sample points.

The CAN bus megafunction has a universal interface for connection to the receive and transmit buffers, allowing the megafunction to be optimized for specific applications. The megafunction does not contain receive or transmit buffers; these buffers must be implemented externally.

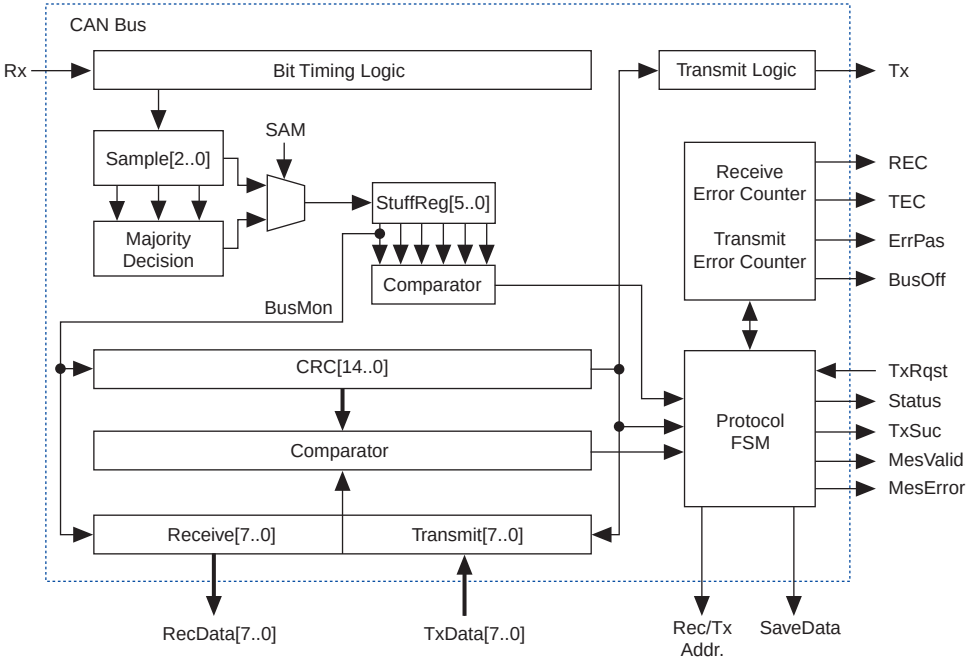
Modifiable Parameters

SICAN can customize the size of the data output on the back-end device.

Block Diagram

Figure 12 shows the block diagram for the CAN bus megafunction.

Figure 12. CAN Bus Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K20	-3	720	0	12 MHz	8-bit data output

IEEE 1394 Link Layer Controller (LLC-I)

Vendor: SIS Microelectronics
Target Application:
Home local-area network (LAN), asynchronous transfer mode (ATM) bridge, real-time multimedia, digital satellite system (DSS), set-top boxes
Additional Deliverables:
Simulation file, demonstration board
ID Code: 7D0E-1394

- Conforms to IEEE 1394-1995 standard for cable environments
- IEEE 1394a standard support on IEEE approval
- Generic 32-bit host bus interface
- Optional asynchronous host clock/cable clock
- Supports IEEE 1394-Annex J physical interface

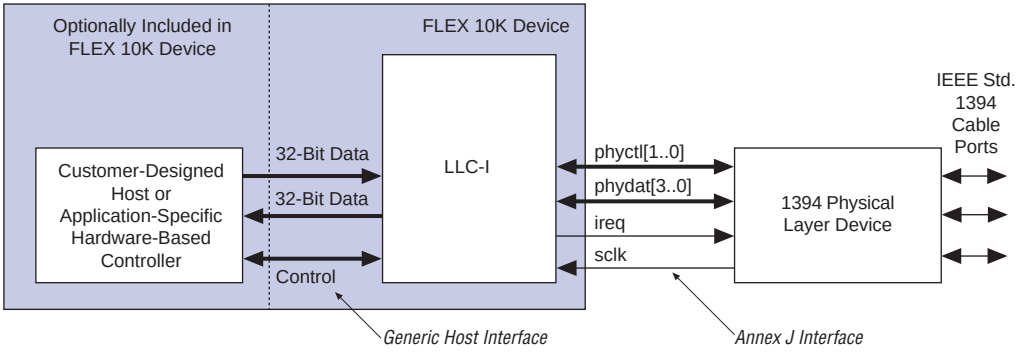
General Description

The IEEE 1394-compatible LLC-I megafunction provides IEEE 1394 asynchronous packet link layer support between a controller implementing the IEEE 1394 transaction layer and an external device implementing the IEEE 1394 physical layer.

Block Diagram

Figure 13 shows the block diagram for the IEEE 1394-compatible LLC-I megafunction.

Figure 13. IEEE 1394-Compatible LLC-I Megafunction Block Diagram



Device Utilization Example *Note (1)*

Device	Speed Grade	Utilization		Performance *Note (2)*	Parameter Setting
		Logic Cells	EABs		
EPF10K100A	-1	3,352	6	50 MHz	Contact SIS Microelectronics

Notes:
(1) This information is preliminary.
(2) Data on the Annex J interface is clocked at 49.152 MHz.

IEEE 1394 Link Layer Controller

Vendor: Simple Silicon
Target Application:
Home LAN, ATM bridge, real-time multimedia, DSS, set-top boxes
Additional Deliverables:
User manual, netlist core, behavioral testbench, test cases, evaluation kit, Verilog HDL source code
ID Code: A441-BE01

- Compliant with ***IEEE 1394 Specification, Draft 8.0 Version 2***
- Supports both asynchronous and isochronous data transfer modes
- Designed for 100 Mbytes per second (Mbps), 200 Mbps, and 400 Mbps bus speeds
- Supports PCI/industry-standard architecture (ISA) interface
- Includes transaction layer, node controller, and bus management facility
- Provides physical layer (PHY) interface compliant with IEEE 1394 specification
- Supports external FIFO and ROM interfaces
- Includes testbench and test suites covering the functionality, protocol, and error conditions

General Description

The IEEE 1394 link layer controller megafunction is the hardware implementation of the link layer and hardware portions of the transaction layer and node controller protocols. The megafunction sends and receives data by forming it into packets, adding headers, and generating and checking the CRCs. When the megafunction wants to send data, it tells the PHY to gain access to the serial bus. When the PHY has accessed the bus, the megafunction sends parallel data to the PHY for serialization transmission through the cable. As data is received by the PHY, it delivers and sends the data to its link. The link determines whether the data is meant for it by reading the address in the header. If it is, the data is accepted and stored appropriately. If not, the data is ignored. A PCI interface is also available with the megafunction.

Modifiable Parameters

The following megafunction parameters can be modified:

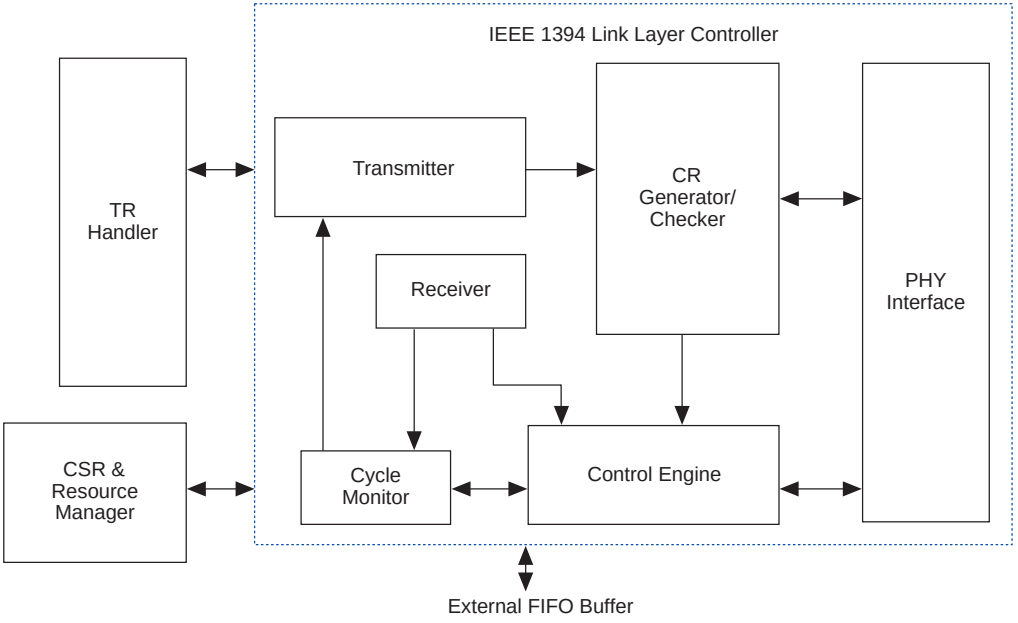
Modifiable Parameters

Parameter	Description
MAX_SPEED	Maximum speed can be 100 Mbps, 200 Mbps, or 400 Mbps.
DATA BUS WIDTH	For link PHY interface. Data bus width can be 2, 4, or 8 bits.

Block Diagram

Figure 14 shows the block diagram for the IEEE 1394 link layer controller megafunction.

Figure 14. IEEE 1394 Link Layer Controller Megafunction Block Diagram



Device Utilization Example *Notes (1), (2)*

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100	-3	4,296	0	50 MHz	Contact Simple Silicon

Notes:
(1) External FIFO buffers can be modeled as EABs, if needed.
(2) The megafunction is designed to support both isochronous and asynchronous modes. However, most applications require only one or the other. Choosing only one mode can result in over 30% savings in logic cell utilization.

IIC Master

Vendor: SICAN Microelectronics
Target Application: Serial data transfer, communication interface for processors, simple two-wire bus system
Additional Deliverables: Simulation file, user guide
ID Code: 18CD-5A7B

- Random read and write accesses
- Usable for multiple devices
- Variable IIC clock generation

General Description

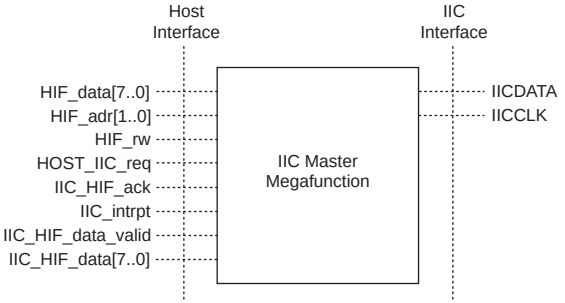
The inter integrated circuit (IIC) master megafunction receives data via the IIC data bus. The IIC master megafunction addresses the IIC slave and supports the transmitting and receiving of data. The received bus data is converted to 8 bits in read mode.

The IIC clock is programmable via a clock divider register. The IIC clock is a single master device that supports an address/data write and a random access read via the IIC bus interface. For more information, contact SICAN Microelectronics Corporation.

Block Diagram

Figure 15 shows the block diagram for the IIC master megafunction.

Figure 15. IIC Master Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K10	-4	243	3	25 MHz	Contact SICAN Microelectronics

IIC Slave

Vendor: SICAN Microelectronics
Target Application: Serial data transfer, communication interface for processors, simple two-wire bus system
Additional Deliverables: Simulation file, user guide
ID Code: 18CD-9A7A

- Random read and write accesses
- Usable for multiple devices
- Up to 8 devices can be connected to the IIC bus

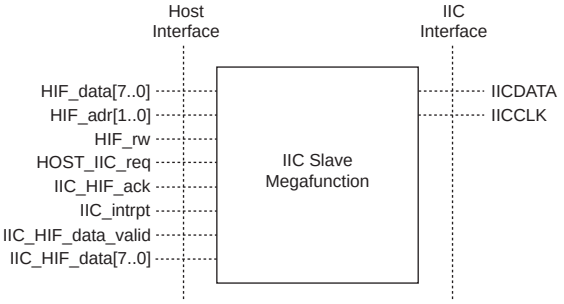
General Description

The IIC slave megafunction receives data via the IIC data bus. It is addressed by an IIC master and supports the transmitting and receiving of data. The received bus data is converted to an 8-bit address and 8-bit data. The IIC slave megafunction also supports the read process by receiving an address and transmitting the data at the DATA_in port. For more information, contact SICAN Microelectronics Corporation.

Block Diagram

Figure 16 shows the block diagram for the IIC slave megafunction.

Figure 16. IIC Slave Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-4	125	3	25 MHz	Contact SICAN Microelectronics

USB Function Controller

Vendor: Sapien Design
Target Application:
High-speed interface PC peripherals, including audio, video, and storage devices
Additional Deliverables:
Simulation test environment available
ID Code: BI0E-1100

- Fully compliant with ***USB Specification, Revision 1.0***
- Automatic hardware-managed protocol
- Up to 16 End Points of any type
- Simple application interface

General Description

The USB function controller megafunction implements the complete ***USB Specification, Revision 1.0*** and is suitable for audio, human interface, and storage applications. This megafunction automatically manages all USB protocol requirements in hardware. It also offers a fast, low-risk method of implementing a USB connection that can be easily integrated into any application.

The USB function controller megafunction efficiently uses the Altera FLEX 10K, FLEX 8000, and FLEX 6000 architectures and offers a low-risk prototype or production solution. This megafunction is available in EDIF netlist, Verilog HDL, or VHDL format.

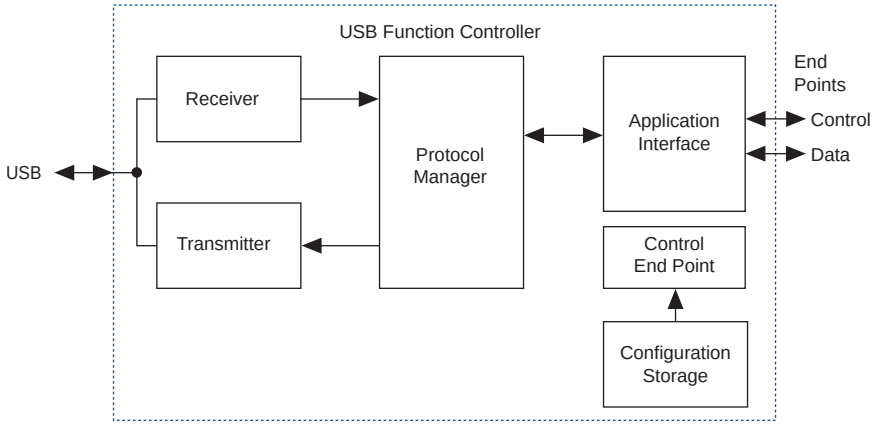
The megafunction is comprised of receiver, transmitter, protocol manager, configuration storage, and application interface logic blocks. The receiver and transmitter blocks support low-level USB protocol operations, such as bit-stuff, NRZI, PID, and CRC. The receiver block decodes the destination of incoming packets and classifies them according to the transfer type. It also checks the CRC and detects bit errors for reporting to the protocol manager. The transmitter block formats packets from the data stream, adding the appropriate CRC header and other protocol requirements.

The protocol manager is responsible for managing higher-level USB protocol functions, such as `ACK`, `NACK`, and `STALL` handshakes. The protocol manager responds to control transfers by accessing the configuration storage for configuration transfers. The configuration storage contains the device, configuration, interface, and End Point descriptor information, which is used to dynamically define and configure the megafunction. The application interface communicates with the USB through the protocol manager and, in turn, is used by the application logic to transfer data, control, and status.

Block Diagram

Figure 17 shows the block diagram for the USB function controller megafunction.

Figure 17. USB Function Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance *Note (1)*	Parameter Setting
		Logic Cells	EABs		
EPF10K20	-4	1,120	3	12 MHz	3 End Points
EPF81500A	-4	1,172	–	12 MHz	Contact Sapien Design

Note:

(1) The standard USB operating frequency is 12 MHz. However, these devices are capable of operating at higher speeds.

USB Function Controller

Vendor: Simple Silicon
Target Application: Computer telephony, plain old telephone service (POTS), integrated services digital network (ISDN), private branch exchange (PBX), printers, scanners, keyboards, HID, audio, compressed video
Additional Deliverables: User manual, documentation, netlist core, behavioral testbench, test cases, evaluation kit, Verilog HDL source code
ID Code: A441-BE02

Simple Silicon, Inc.

- Fully compliant with ***USB Specification, Revision 1.0***
- Supports up to 16 End Points (user-selectable number, depending on application)
- Supports back-end execution of vendor-specific and class-specific USB requests
- Extensive set of back-end interface signals are provided to access FIFO buffers and to indicate events like suspend, start of frame (SOF), change in configuration, and remote wakeup
- Supports four transfer types: isochronous, control, bulk, and interrupt
- Includes extensive test suites covering the functionality, protocol check, and error conditions
- User can write tests using high-level constructs like SETUP and IN
- Compatible with the available USB transceiver devices
- Supports both 12-Mbps and 1.5-Mbps transfer rates

General Description

The USB function controller megafunction consists of four main modules: serial interface engine (SIE), control engine, End Point FIFO buffer, and digital phase-locked loop (PLL). The SIE consists of a transmitter, receiver, suspend detector, and reset detector. The function core can be used to design and prototype any USB peripheral device. A working keyboard function demonstration and prototype board is available for evaluation.

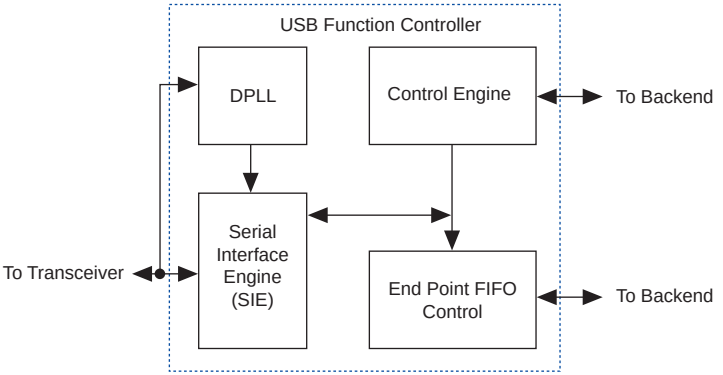
Modifiable Parameters

Simple Silicon can customize the number of End Points and the End Point FIFO depth to meet user specifications. The default number of End Points is 4.

Block Diagram

Figure 18 shows a block diagram of the USB function controller megafunction.

Figure 18. USB Function Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K70	-3	3,240	0	48 MHz	Full-speed operation with 4 End Point FIFO buffers.
EPF10K30	-4	1,592	0	6 MHz	Low-speed operation with 2 End Point FIFO buffers.

USB Host Controller

Vendor: Sapien Design
Target Application:
USB host control for embedded systems
Additional Deliverables:
Board, simulation files
ID Code: BIOE-2100

- Compatible with ***USB Specification, Revision 1.0***
- Automatic, hardware-managed protocol
- Supports suspend, resume, and reset signaling

General Description

The USB host controller megafunction implements the complete ***USB Specification, Revision 1.0*** for host controllers and is suitable for embedded system applications that drive USB devices. The megafunction automatically manages all USB protocol requirements in hardware. It offers a fast, low-risk method of implementing a USB connection that can be integrated into any application. The megafunction is available in netlist, Verilog HDL, or VHDL register transfer language (RTL) format.

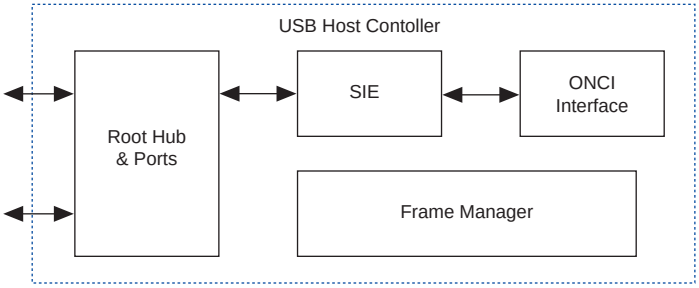
The Serial Interface Engine (SIE) performs receiver and transmitter functions, including packet formation and serialization. The SIE also supports low-level USB protocol operations, such as bit-stuff, NRZI, PID, and CRC. The SIE decodes incoming packets, checks the CRC, and detects bit errors, which are all reported to the frame manager. The SIE formats outgoing packets, adding the appropriate header CRC and other protocol requirements.

The Frame Manager generates SOF packets, schedules periodic and non-periodic packets into frames, and manages data and handshake packets. The system processor queues packets, which contain headers with direction, size, and destination information, into memory. Packet locations are written to channel registers, and subsequent packets are chained together. Packets that time out or return a NACK signal are automatically retried. Packet sizes are used as a criteria for inclusion into a frame. For more information, contact Sapien Design.

Block Diagram

Figure 19 shows the block diagram for the USB host controller megafunction.

Figure 19. USB Host Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30	-4	1,250	3 to 6	12 MHz	Contact Sapien Design
EPF81500A	-4	1,250	–	12 MHz	Contact Sapien Design

USB Host Controller

Vendor: Simple Silicon
Target Application:
USB modems, applications requiring USB compliance
Additional Deliverables:
User manual, netlist core, testbench, test cases, evaluation kit, VHDL and Verilog HDL source code
ID Code: A441-BE04

- Compatible with ***USB Specification, Revision 1.0***
- 80-ms USB watchdog timer
- 10-µs USB reset timer
- On-board USB ports for four USB End Points
- Supports all four transfer types: control, interrupt, isochronous, and bulk
- Suspend and resume ability
- Fully static operation: 0 Hz to 40 MHz
- PCI interface
- Fully independent finite state machine eliminates need of companion processor/controller

General Description

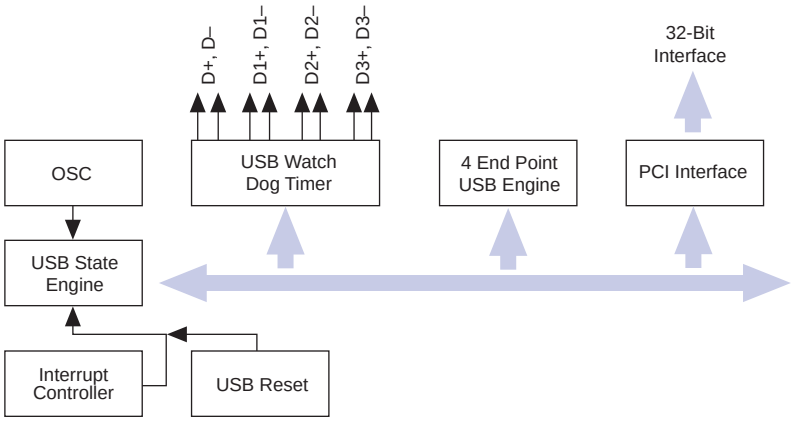
The USB host controller megafunction is a USB device-side host controller with a PCI interface. This megafunction provides four specification-compliant USB End Points and a PCI interface for ultimate design flexibility. The megafunction provides a low-cost, yet high-performance intelligent design that simplifies upgrade paths for most of today's leading PC manufacturers. The megafunction can seamlessly connect to any PCI-based 486, Pentium, PowerPC, or MIPS platform. This megafunction can be utilized to create a PCI-compatible add-on board or can be added directly to a motherboard design without additional "glue logic."

The megafunction provides excellent USB performance and compatibility at a low cost by allowing use of any PCI-compatible processor. This megafunction allows a simple upgrade path from current serial-based micro-architectures to an all-inclusive performance-enhanced USB strategy. The device can interface with any high-performance PCI-based 486, Pentium, or PowerPC processor. By combining a versatile 32-bit PCI interface with an on-board USB, the megafunction provides a flexible and cost-effective solution to many USB applications, including joystick, CD-ROM, mouse, scanner, printer, modem, or PBX.

Block Diagram

Figure 20 shows the block diagram for the USB host controller megafunction.

Figure 20. USB Host Controller Megafunction



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K40	-3	2,471	0	50 MHz	Contact Simple Silicon

USB Hub Controller

Vendor: Simple Silicon
Target Application:
Home LAN, ATM bridge, real-time multimedia, DSS, set-top boxes
Additional Deliverables:
User manual, documentation, netlist core, behavioral testbench, test cases, evaluation kit, Verilog HDL source code
ID Code: A441-BE03

- Fully compliant with ***USB Specification, Revision 1.1 RC2***
- Works with commercially available USB transceivers
- Supports both bus-powered and self-powered mode
- Supports test mode, which improves simulation speed
- Supplied with user-friendly test environment
- Test vectors cover the USB compliance checklist
- Supports full and low speeds
- Supports standard USB requests and hub-specific requests, as required by the ***USB Specification, Revision 1.1 RC2***

General Description

The USB hub controller megafunction manages multiple USB connections. Hubs can also act as peripherals, for example, when a printer simultaneously serves as a USB peripheral and USB hub, which allows other USB peripherals to connect to the peripheral. The megafunction consists of a repeater, a hub, and port controllers. The megafunction contains a 4× digital PLL, which recovers synchronized clocks and data from the received USB data. The USB hub controller megafunction is supported with a behavioral host model, USB bus analyzer models, and extensive test suites.

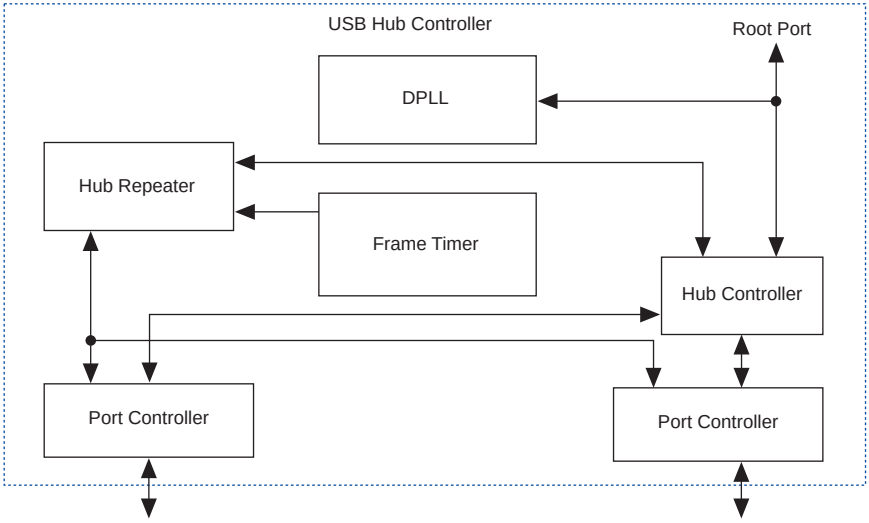
Modifiable Parameters

Simple Silicon can customize the number of downstream ports (the default is two) and whether the power switch is on or off.

Block Diagram

Figure 21 shows the block diagram for the USB hub controller megafunction.

Figure 21. USB Hub Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50	-3	2,278	0	48 MHz	12 MHz operation with 4× clock

VUSB Embedded Host Controller

Vendor: VAutomation
Target Application:
USB peripherals, USB hosts that do not require full OHCI functionality
Additional Deliverables:
VUSB reference manual
ID Code: 3A0F-BA12

- Integrated USB microcontrollers for USB host and device applications
- Verified in silicon, 100% USB 1.0 compliant
- Uses embedded 8-bit reduced instruction set computers (RISC) CPU for USB command processing
- Supports low/full speed devices and any number of End Points and configurations
- Easily modified to support class or vendor-specific commands
- Applications may required only a 6-MIP RISC CPU

General Description

VAutomation's VUSB megafunctions are complete solutions for your USB embedded host peripheral function requirements. The megafunction has been verified in silicon and is fully compliant with USB 1.0 specification.

The embedded host controller megafunction is ideal for applications that do not require the cost, bulk, and complexity of open human computer interaction (HCI)-compliant host controllers. It allows a USB host controller to be embedded within devices that have simple, well-defined requirements for interfacing to USB peripherals, such as a digital camera that needs to print directly to a USB printer without the intervention of a PC.

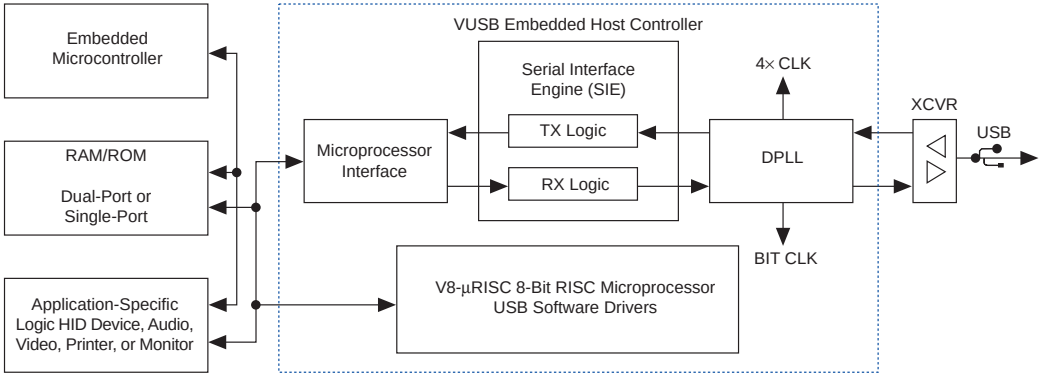
Unlike traditional USB functions, the VUSB megafunctions are intelligent functions. Most USB protocols are implemented in software that executes on the embedded V8-µRISC 8-bit RISC microprocessor, which allows the VUSB megafunction to be a one-function USB solution, eliminating the need for an off-chip processor. In conjunction with a memory-based FIFO architecture, the megafunction allows you to easily accommodate changes (e.g., buffer size) in the specification, application, or operating system.

The embedded RISC microprocessor delivers 6 MIPS in a FLEX 10K device, much of which is available for non-USB tasks. This excess bandwidth, coupled with a wide range of CPU peripherals and a robust set of development tools, allows the VUSB megafunction to be a single-function solution for many USB applications.

Block Diagram

Figure 22 shows the block diagram for the VUSB host controller megafunction.

Figure 22. VUSB Embedded Host Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50	-1	2,479	0	12 Mbits	Contact VAutomation

Notes:

Processor & Peripheral

June 1998

Overview

Embedding processor megafunctions in programmable logic not only provides board space reductions, but also improves the performance of traditional devices by reducing the number of clock cycles per instruction, thereby increasing the system clock frequency. Processor and peripheral megafunctions can improve the flexibility of microcontrollers by providing a larger address space memory for an unlimited combination of peripherals, e.g., I/O ports, timers, and universal asynchronous receiver/transmitters (UARTs).

The user can specify a wide range of parameters for each processor and create virtually an unlimited number of instructions, based on the instruction templates. Processor compilation and assembly are almost instantaneous so that the processor architecture, instruction set, and design can all be varied continuously for the best trade-offs in processor and design size/complexity.

Contents

The processor and peripheral section contains the following functions:

Microcontroller

Microprocessor

Peripheral

Peripheral *(Continued)*

UART

C49410 Microprogram Controller

Vendor: CAST
Target Application:
High-speed bit slice designs
Additional Deliverables:
VHDL simulation files, user guide
ID Code: 2AA5-C002

- 16-bit data width that addresses up to 65,536 words
- Internal loop counter can be preset to a 16-bit down-counter for repeating instructions and counting loop interactions
- Four address sources—Microprogram address may be selected from microprogram counter branch address bus, 33-level push/pop stack, or internal holding register
- 16 powerful micro-instructions
- Output enable controls for three branch address sources
- Positive-edge-triggered registers
- Developed in VHDL and synthesized to approximately 9,500 gates, depending on the process used
- Functionally based on the Integrated Device Technology IDT49C410 device

General Description

The C49410 microprogram controller megafunction is an address sequencer that controls the execution sequence for micro-instructions stored in microprogram memory. The megafunction can sequentially access the micro-instructions and can provide conditional branching to any micro-instructions within the 65,536-microword range. In addition, a 33-deep last-in first-out (LIFO) stack provides a microsubroutine return linkage and looping capability.

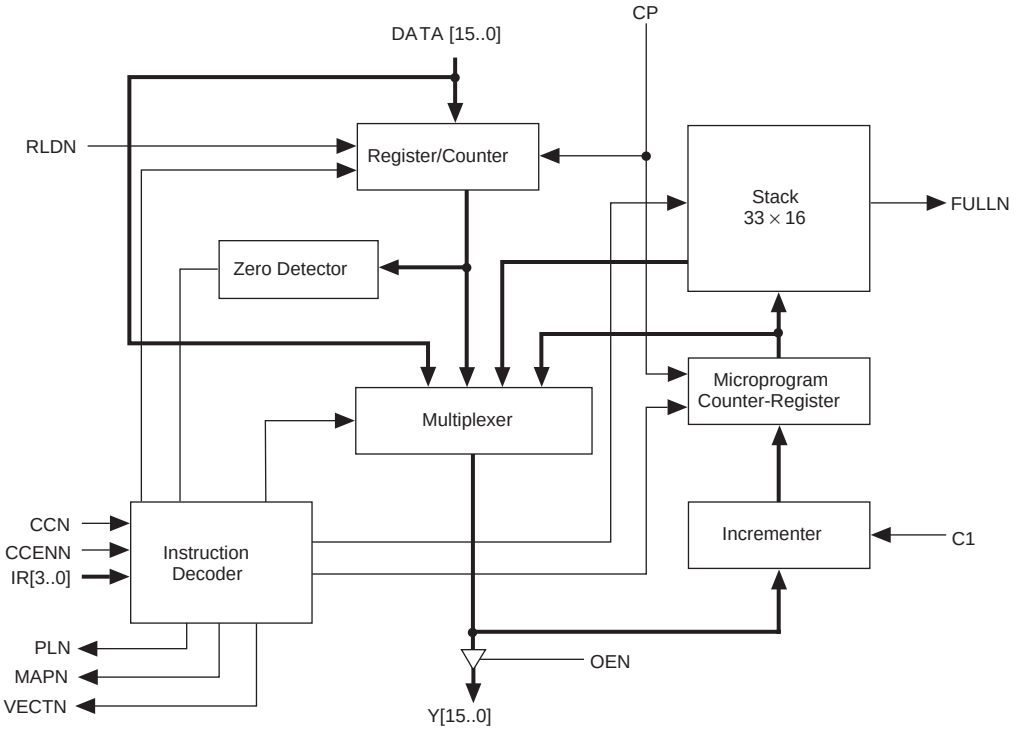
Modifiable Parameters

CAST can modify the megafunction's data width and stack depth to meet user specifications.

Block Diagram

Figure 1 shows the block diagram for the C49410 microprogram controller megafunction.

Figure 1. C49410 Microprogram Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	1,291	0	35 MHz	Contact CAST
EPF6016	-2	1,139	–	17 MHz	Contact CAST

C8051 Microcontroller Unit

Vendor: CAST
Target Application:
8-bit mcu
Additional Deliverables:
VHDL source code, synthesis scripts, testbench, assembler programs, modeling notes, compilation notes, simulation notes, synthesis notes
ID Code: 2AA5-C017

- 8-bit control unit
- 8-bit arithmetic logic unit with 8 × 8-bit multiplication and division
- Instruction decoder
- Four 8-bit input/output ports
- Two 16-bit timers/counters
- Serial peripheral interface in full duplex mode
- Two-level priority interrupt system
- Five interrupt sources
- Internal clock prescaler and phase generator
- 256 bytes of read/write data memory
- 64 Kbytes of external program memory space
- 64 Kbytes of external data memory space
- Functionality based on the Intel 8051 8-bit controller
- C8051 megafunction is licensed from Evatronix S.A.

General Description

The C8051 microcontroller unit megafunction is a fast, single-chip, 8-bit microcontroller and is a derivative of the 80C51 microcontroller family. The megafunction is a fully functional 8-bit embedded controller that executes all ASM51 instructions and has the same instruction set as the 80C51. The C8051 megafunction accesses instructions from two kinds of program memory, serves software and hardware interrupts, and provides serial communications interface and timer systems.

The C8051 microcontroller unit megafunction is a high-performance, synthesizable 80C51 function specifically designed for reusability. It can operate at frequencies up to 11 MHz in FLEX® devices.

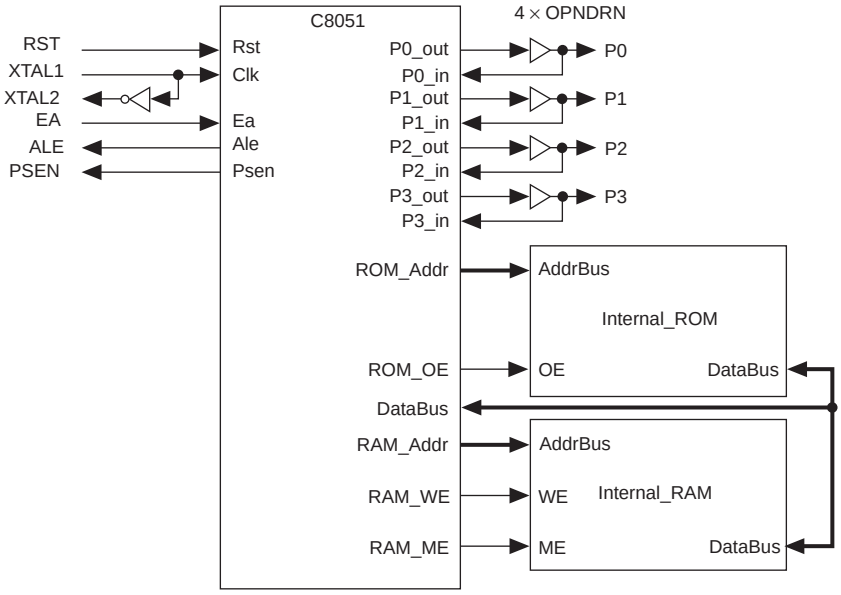
The Super8051 consists of the following modules:

- *Functional core*—C8051 megafunction
- *Program memory*—Internal_ROM
- *Data memory*—Internal_RAM
- *Open drain I/O pins*—OPNDRN

Block Diagram

Figure 2 shows the block diagram for the C8051 microcontroller unit megafunction.

Figure 2. C8051 Microcontroller Unit Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	2,398	0	8 MHz	Contact CAST

RAW8051/8052

Vendor: Richard Watts Associates
Target Application: Low-power microcontroller
Additional Deliverables: Full user manual, VHDL design walkthrough
ID Code: DE73-8052

- Fast 8051/8052 CPU megafunction with 100% software code compatibility
- Three times faster than a standard 8052 at the same clock frequency
- Reduced instruction cycle time
- Optimized for Altera® programmable logic devices (PLDs), with application-specific integrated circuit (ASIC) versions available for easy migration
- Available as CPU only, 8051, and 8052 variations
- Evaluation board available for prototyping

General Description

The RAW8051/8052 megafunction implements an enhanced industry-standard 805*X* microcontroller. On average, the megafunction executes software three times faster than a standard 805*X*,while maintaining 100% software code compatibility. In addition to the standard 805*X* peripherals, the megafunction implements an additional data pointer for faster memory copies and indexing. An extended memory version is also available for taking the addressing range up to 4 Mbytes.

The RAW8051/8052 megafunction is supported by a variety of standard EDA development tools.

Modifiable Parameters

The following megafunction parameters can be modified:

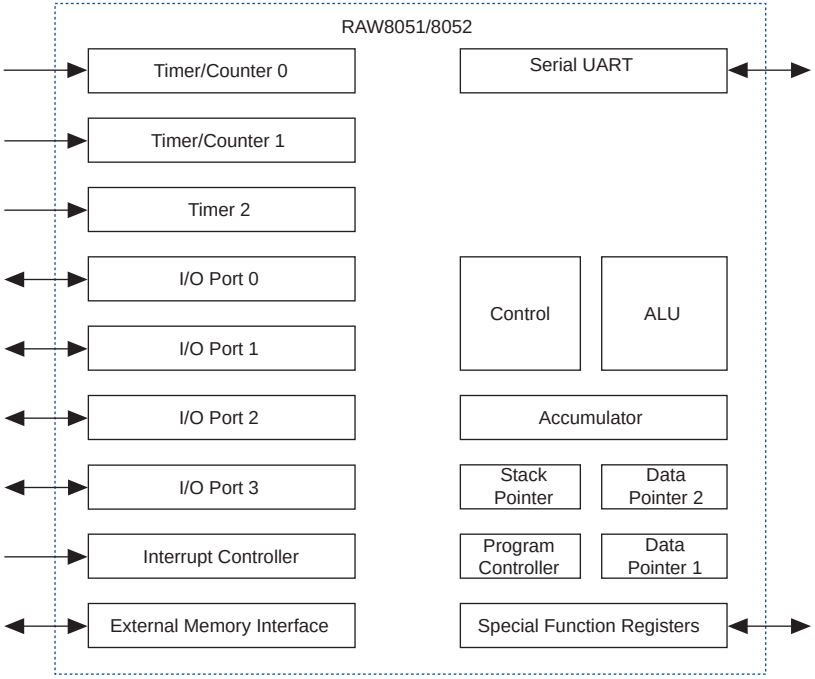
Modifiable Parameters

Parameter	Description
C	Number of counters
I	Number of I/O ports
SM	External memory size
T	Type of CPU core: 8051 or 8052
U	Number of UARTs

Block Diagram

Figure 3 shows the block diagram for the RAW8051/8052 megafunction.

Figure 3. RAW8051/8052 Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	2,177	1	21 MHz	C = 2, I = 6, SM = 644, T = 8052, U = 1
EPF10K40	-1	1,825	1	11 MHz	C = 2, I = 6, SM = 644, T = 8051, U = 1

C2910A Microprogram Controller

Vendor: CAST
Target Application: Serial data communications applications, modem interface
Additional Deliverables: VHDL testbench, VHDL simulation files, user guide
ID Code: 2AA5-C001

- 12-bit data width that addresses up to 4,096 words
- Internal loop counter—Pre-settable 12-bit down-counter for repeating instructions and counting loop interactions
- Four address sources—Microprogram address may be selected from microprogram counter, branch address bus, 9-level push/pop stack, or internal holding register
- 16 powerful micro-instructions
- Output enable controls for three branch address sources
- Positive-edge-triggered registers
- Functionality based on the AMD AM2910A device

General Description

The C2910A microprogram controller megafunction is an address sequencer that controls the execution sequence for the micro-instructions stored in microprogram memory. The megafunction can sequentially access the micro-instructions, and it provides conditional branching to any micro-instructions within the 4,096-microword range. In addition, a nine-deep LIFO stack provides a microsubroutine return linkage and looping capability.

Modifiable Parameters

CAST can modify the following megafunction parameters:

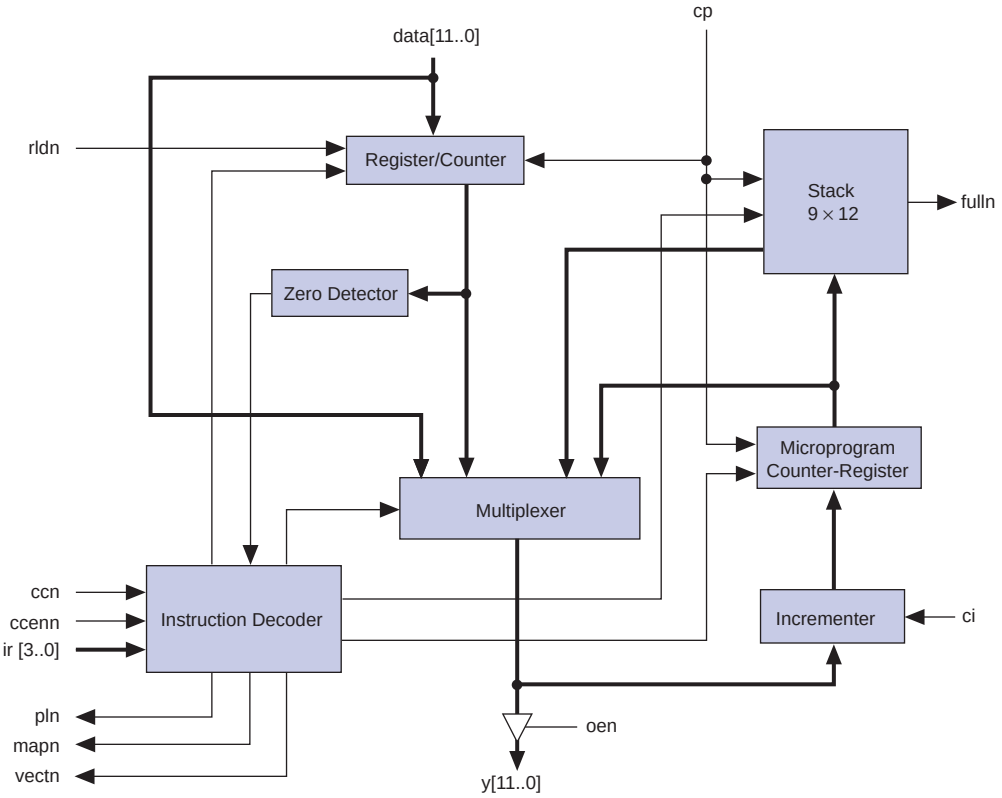
Modifiable Parameters

Parameter	Description
D	Data width
S	Stack width

Block Diagram

Figure 4 shows the block diagram for the C2910A microprogram controller megafunction.

Figure 4. C2910A Microprogram Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-1	346	0	50 MHz	D = 12 bits, S = 9 × 12
EPF6016	-2	355	–	27 MHz	

BareCore 8052-A

Vendor: Richard Watts Associates
Target Application: 8-bit µcu
Additional Deliverables: Full user manual, VHDL design walkthrough
ID Code: DE73-8052

- Fast 8052/32 CPU with 100% software code compatibility
- Three times faster than a standard product 8052
- Reduced execution cycle time
- ASIC versions available for easy migration
- Evaluation board available for prototyping

General Description

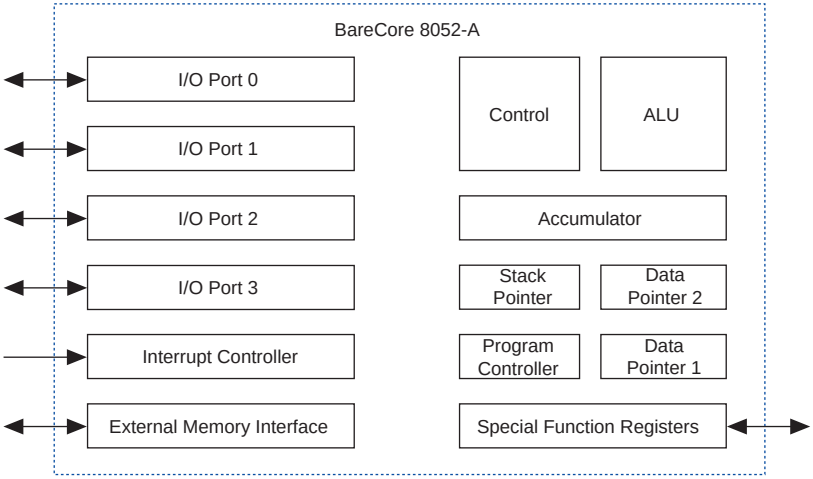
The BareCore 8052-A megafunction implements an enhanced industry-standard, 8052 8-bit microcontroller. On average, the megafunction executes software three times faster than a standard 8052 device while maintaining 100% software code compatibility. A Philips-compatible extra data pointer is provided for faster memory copies and indexing.

The BareCore 8052-A megafunction is supported by a wide variety of standard EDA development tools. The megafunction allows designers to use existing software code and achieve performance that is comparable to reduced instruction set computer (RISC) megafunctions.

Block Diagram

Figure 5 shows the block diagram for the BareCore 8052-A megafunction.

Figure 5. BareCore 8052-A Megafunction Block Diagram



Device Utilization Example *Note (1)*

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30	-3	1,400	1	11 MHz	Contact Richard Watts Associates

Note:
(1) This example is optimized for minimum area. Speed improvements are possible.

FLEXCore

Vendor: Hammer Cores
Target Application: Embedded controller/processor
Additional Deliverables: User guide, FLEXCore utility (Windows 3.1 and Windows 95)
ID Code: C4D5-CFC0

- Computer instruction set computer (CISC) architecture
- Up to 20-MHz system clock
- 2 to 26 registers
- 8- to 24-bit data and address path
- 1 to 7 interrupts (individually vectored)
- Up to 16-Mbyte addressing capability
- Ships with complete development tools

General Description

The FLEXCore megafunction is an embedded controller/processor with a user-defined architecture and instruction set. The megafunction is designed to replace small board-level embedded control applications. Processor performance is on the order of an 8051 device on the low end, and an 8086 device on the high end.

The user can specify a wide range of parameters for the processor and create virtually an unlimited number of instructions, based on the instruction templates. The processor specifications are compiled with the processor compiler, and an assembler is provided for software development. Processor compilation and assembly are almost instantaneous, so that the processor architecture, instruction set, and code can all be continuously varied for the best trade-off in processor and code size/complexity.

The arithmetic logic unit (ALU) can perform up to 18 separate operations. Microcoded multiplies, both signed and unsigned, can also be specified. Any register can be specified to act as an index register for another register.

The FLEXCore megafunction offers non-multiplexed address and data buses. The address and data buses and the internal processor are the same width. All data transfers occur on the rising edge of the system clock. A read/write line and two data buses, one for the output data and one for the input data, are provided. For connection to devices outside of the PLD, the buses may be connected at the I/O pins with a tri-state buffer, controlled by the FLEXCore megafunction's read/write line.

The megafunction is designed specifically for Altera FLEX 10K devices. The processor is defined first, using the processor compiler, and software is written and assembled with the assembler command. The processor compiler and assembler output files are used by the MAX+PLUS® II development system to compile the processor system.

Modifiable Parameters

The following megafunction parameters can be modified:

Modifiable Parameters

Parameter	Description
BW	Datapath, processor data widths
NUMINTS	Interrupts, number of interrupts
REGS	Registers, number of data/address registers

Block Diagram

Figure 6 shows the block diagram for the embedded processor FLEXCore megafunction.

Figure 6. Embedded Processor FLEXCore Megafunction Block Diagram

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	368	4	20 MHz	BW = 8, NUMINTS = 3, REGS = 7

RISC Processor

Vendor: Hammer Cores
Target Application:
Very fast embedded controller/processor
Additional Deliverables:
User guide, ASX assembler
ID Code: C4D5-F8IC

- RISC architecture
- High performance
- Fully user parameterized
- DSP instruction set extension
- Ships with assembler

General Description

The RISC processor megafunction is a user-parameterizable, high-performance 5-stage pipeline RISC processor optimized for Altera FLEX 10K devices. The data path width is 16 bits, and the processor features a compact 16-bit instruction set. The megafunction executes one instruction per clock cycle, at speeds up to 50 MIPs.

The user can specify the stack depth and the number of core registers, inputs, and outputs. The I/O ports operate at the same speed as the core registers, and are memory-mapped to the data space.

The megafunction's assembler specifies the construction of the core. If DSP instructions, such as multiplies, are found, the assembler will instruct the processor to include a single cycle multiplier-accumulator (MAC) to the function. If only single-bit shifts are used for the shift/rotate instructions, a small barrel shifter is used. Otherwise, a full-featured barrel shifter is included.

Block Diagram

Figure 7 shows the block diagram for the RISC processor megafunction.

Figure 7. RISC Processor Megafunction Block Diagram

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	850	4	48 MIPS	REGISTERS = 8, STACKWIDTH = 6, INPORT = 7, OUTPORT = 2

V6502 Microprocessor

Vendor: VAutomation
Target Application:
General-purpose embedded computing and control
Additional Deliverables:
Reference manual
ID Code: 3A0F-6502

- Code compatible with the Rockwell R65C02 device
- 70 instructions, 210 opcodes, 15 addressing modes
- 8-bit ALU with binary and decimal arithmetic
- 64-Kbyte addressing capability
- Fully synchronous and static design

General Description

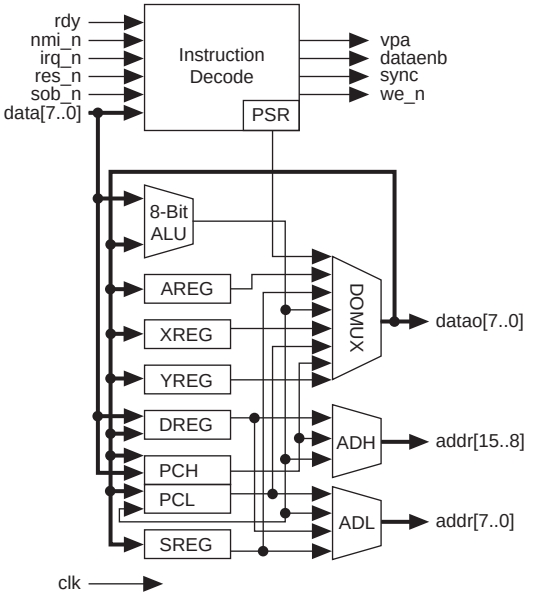
The V6502 microprocessor megafunction is a high-performance, 8-bit microprocessor. The megafunction is functionally based on and compatible with the Rockwell R65C02 device. In addition, assemblers and C compilers are available for the megafunction from third-party developers.

The V6502 microprocessor megafunction has been completely redesigned using the latest high-speed design techniques to produce a high-performance microprocessor with a minimal gate count. The megafunction is easily integrated with user-specified logic and other megafunctions.

Block Diagram

Figure 8 shows the block diagram for the V6502 microprocessor megafunction.

Figure 8. V6502 Microprocessor Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K40	-3	920	0	14 MHz	Contact VAutomation

V8-µRISC

Vendor: VAutomation
Target Application:
General-purpose embedded computing and control
Additional Deliverables:
Reference manual
ID Code: 3A0F-B008

- RISC architecture for low gate count and high performance
- High code density, many opcodes are a single byte
- 33 opcodes and 4 addressing modes
- 8-bit ALU
- 64-Kbyte addressing capability
- Eight 8-bit general-purpose registers
- Multiple register banks that minimize interrupt latency
- 16-bit program counter and stack pointer
- Seven maskable interrupts, one non-maskable interrupt
- Assembler, C Compiler, simulator, and debugger available
- IntelliCore Prototyping System available for evaluation and rapid product development

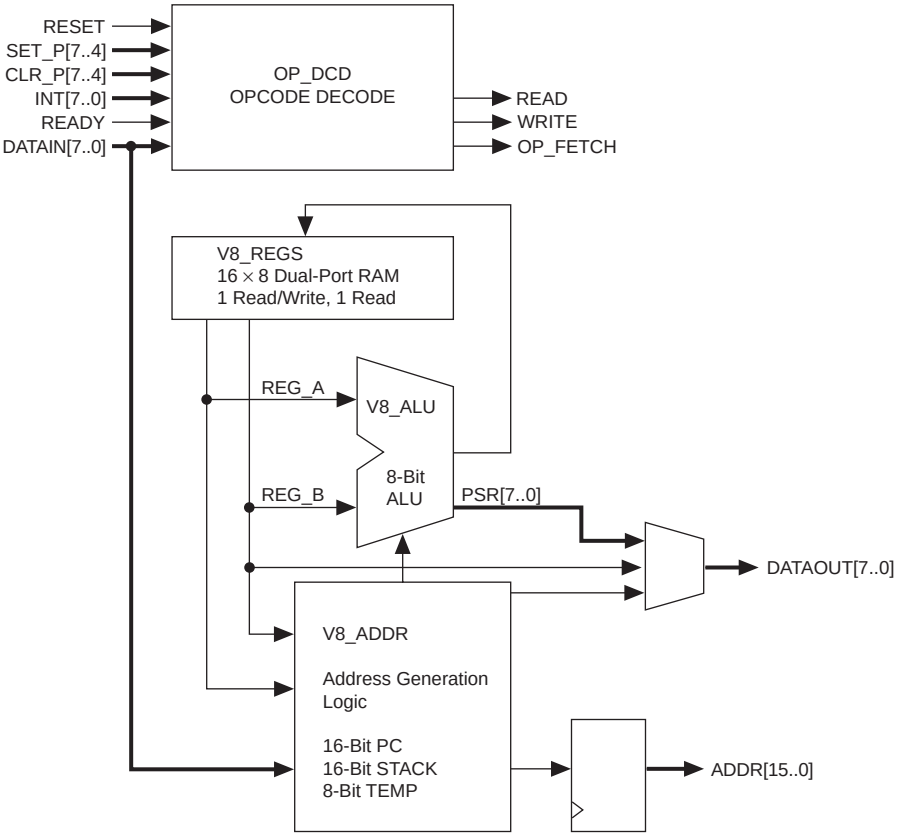
General Description

The 8-bit RISC microprocessor (V8-µRISC) megafunction is a general-purpose processor function. It combines a small gate count with single clock cycle execution for many instructions to deliver a high-performance 8-bit microprocessor with a very small footprint. The V8-µRISC megafunction comes with a set of standard peripherals, including a timer, UART, direct memory access (DMA) controller, DRAM controller, IIC EEPROM interface, P1284 parallel interface, and page register design, to expand the address space to 8 Mbytes. The megafunction and its peripherals allow high-performance custom microcontrollers to be implemented within Altera PLDs.

Block Diagram

Figure 9 shows the block diagram for the V8-µRISC megafunction.

Figure 9. V8-µRISC Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K20	-3	888	0	12 MHz	Contact VAutomation

VZ80 Microprocessor

Vendor: VAutomation
Target Application:
General-purpose embedded computing and control
Additional Deliverables:
Reference manual
ID Code: 3A0F-BA80

- Code compatible with the Zilog Z80 device
- 158 instructions, 10 addressing modes
- 8-bit ALU with binary and decimal arithmetic
- 64-Kbyte addressing capability
- Fully synchronous and static design

General Description

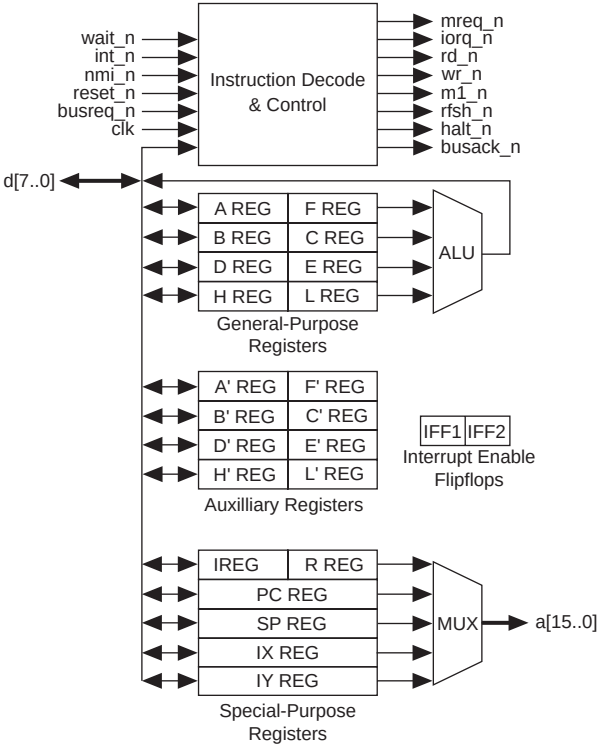
The VZ80 microprocessor megafunction is a powerful, medium-gate-count microprocessor that includes block transfers and bit test, set, and reset instructions. The megafunction is functionally based on and compatible with the Zilog Z80 device. In addition, assemblers and C compilers are available for the megafunction from third-party developers.

The megafunction has fast context switch capability with an entire auxiliary register set. The megafunction is easily integrated with user-specified logic and other megafunctions.

Block Diagram

Figure 10 shows the block diagram for the VZ80 microprocessor megafunction.

Figure 10. VZ80 Microprocessor Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K40	-3	2,028	0	10 MHz	Contact VAutomation

C8254 Programmable Interval Timer/Counter

Vendor: CAST
Target Application:
Event counters, elapsed-time indicators, programmable one-shots
Additional Deliverables:
VHDL testbench
ID Code: 2AA5-C016

- Status read-back command
- Counter latch command
- Read/write least significant bit (LSB) only, most significant bit (MSB) only, or LSB first then MSB
- Six programmable counter modes
  - Interrupt on terminal count
  - Hardware retriggerable one-shot
  - Rate generator
  - Square wave mode
  - Software-triggered strobe
  - Hardware-triggered strobe (retriggerable)
- Binary or binary coded decimal (BCD) strobe
- Based on the Intel 82C54 device, with improved clock input rates up to 30 MHz

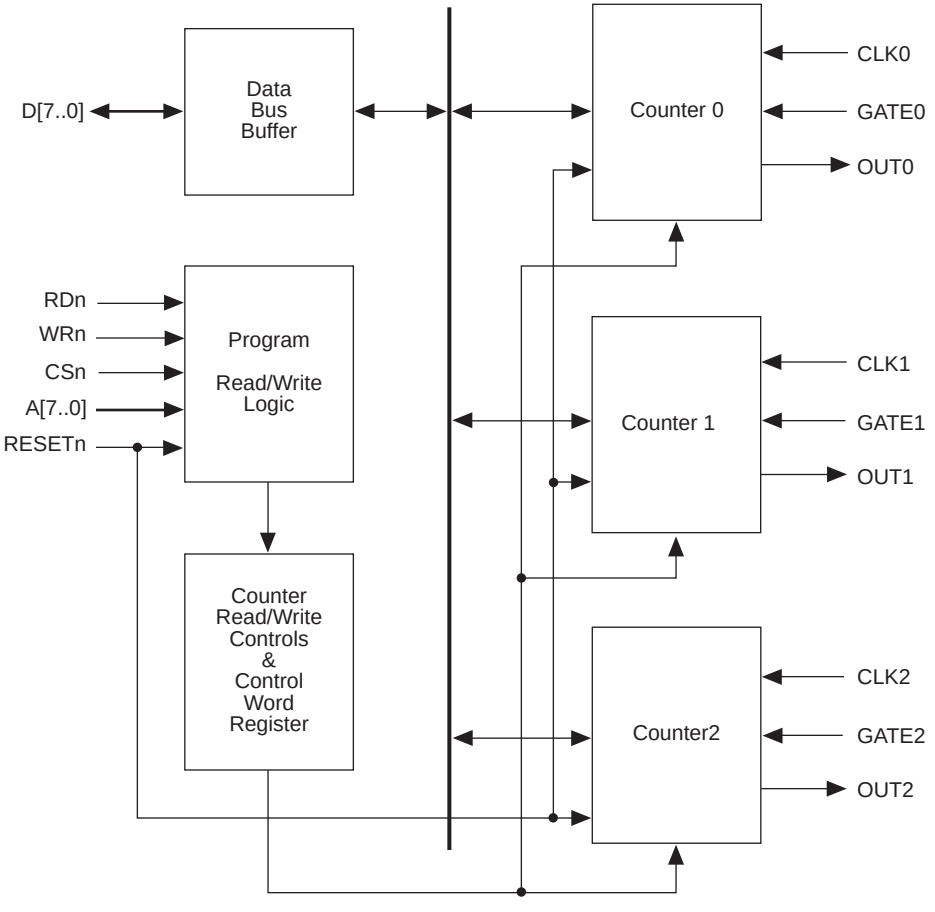
General Description

The C8254 programmable interval time/counter megafunction is a high-performance device that is designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, and each counter may operate in a different mode. All modes are software programmable. The C8254 megafunction solves one of the most common problems in any microcomputer system: the generation of accurate time delays under software control. Instead of setting up timing loops in software, the C8254 megafunction can be programmed to match requirements by programming one of the counters for the desired delay.

Block Diagram

Figure 11 shows the block diagram for the C8254 programmable interval timer/counter megafunction.

Figure 11. C8254 Programmable Interval Timer/Counter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	784	0	30 MHz	Contact CAST

C8255A Programmable Peripheral Interface

Vendor: CAST
Target Application:
Printers, keyboards, displays, floppy disk controllers, cathode ray tube (CRT) controllers, machine tools, D/A and A/D converters
Additional Deliverables:
VHDL testbench
ID Code: 2AA5-C007

- Three 8-bit peripheral ports: A, B, C
- Three programming modes for peripheral ports
  - Mode 0 (basic input/output)
  - Mode 1 (strobed input/output)
  - Mode 2 (bidirectional)
- Total of 24 programmable I/O lines
- Eight-bit bidirectional system data bus with standard microprocessor interface controls
- Developed in VHDL and synthesized up to 1,000 gates, depending on the process used
- Functionally based on the Intel 8255A device

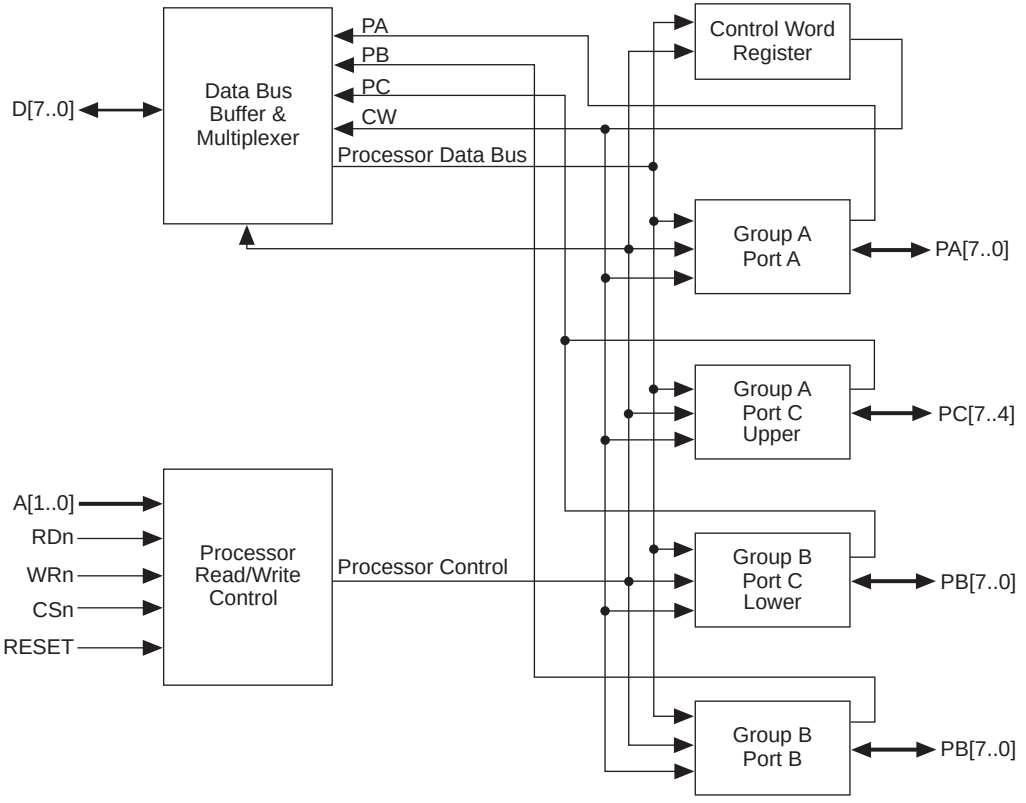
General Description

The C8255A programmable peripheral interface megafunction reduces the external logic normally needed to interface peripheral devices. The 8255A/82C55A devices replace a significant percentage of the logic required to support a variety of byte-oriented input/output interfaces. The megafunction's functional configuration is programmed by the system software, so external logic is not required to interface peripheral devices.

Block Diagram

Figure 12 shows the block diagram for the C8255A programmable peripheral interface megafunction.

Figure 12. C8255A Programmable Peripheral Interface Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	178	0	158 MHz	Contact CAST

C8259A Programmable Interrupt Controller

Vendor: CAST
Target Application:
Real-time, interrupt-driven microcomputer designs
Additional Deliverables:
VHDL testbench
ID Code: 2AA5-C013

- Eight vectored priority interrupts per megafunction. Up to 64 vectored priority interrupts with cascading
- Programming for all C8259A modes and operational features
  - MCS-80/85 and 8088/8086 processor modes
  - Fully nested mode and special fully nested mode
  - Special mask mode
  - Buffered mode
  - Pool command mode
  - Cascade mode with master or slave selection
  - Automatic end-of-interrupt mode
  - Specific and non-specific end-of-interrupt commands
  - Automatic rotation
  - Specific rotation
  - Edge- and level-triggered interrupt input modes
  - Reading of interrupt request register (IRR) and in-service register (ISR) through data bus
- Developed in VHDL and synthesizes up to 2,000 gates, depending on the process used
- Functionally based on the Intel 8259A and Harris 82C59A devices

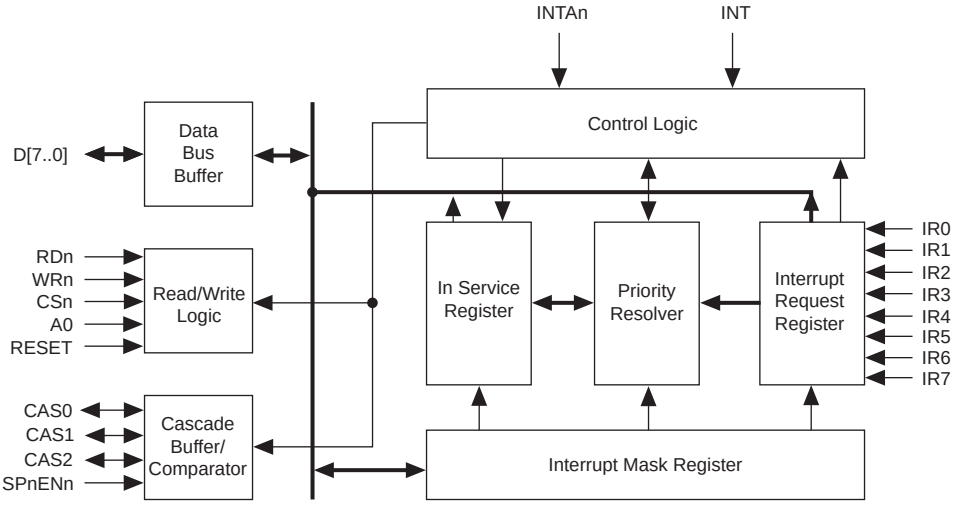
General Description

The C8259A programmable interrupt controller megafunction manages up to 8 vectored priority interrupts for a processor. Using multiple instantiations of the megafunction and programming it to cascade mode allows up to 64 vectored interrupts. More than 64 vectored interrupts can be accomplished by programming the megafunction to poll command mode.

Block Diagram

Figure 13 shows the block diagram for the C8259A programmable interrupt controller megafunction.

Figure 13. C8259A Programmable Interrupt Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-1	552	0	30 MHz	Contact CAST

C29116A 16-Bit Microprocessor

Vendor: CAST
Target Application:
16-bit mpu
Additional Deliverables:
VHDL testbench, simulation files
ID Code: 2AA5-5007

- 8- or 16-bit data width
- Powerful field insertion/extraction and bit manipulation instructions rotate and merge, rotate and compare, and bit manipulation instructions provided for complex bit control
- 32 working 16-bit registers
- 16-bit barrel shifter
- Immediate instruction capability may be used for storing constants in microcode or for configuring a second data port
- Developed in VHDL and synthesizes to approximately 3,800 gates (excluding RAM) depending on the process used
- Functionality based on the AMD's AM29116A device

General Description

The C29116A 16-bit microprocessor megafunction is a microprogrammable 16-bit bipolar microprocessor whose architecture and instruction set is optimized for high-performance peripheral controllers, such as graphics controllers, disk controllers, communications controllers, front-end concentrators, and modems. The device also performs well in microprogrammed processor applications. In addition to its complete arithmetic and logic instruction set, the megafunction's instruction set contains functions particularly useful in controller applications: bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic redundancy code (CRC) generation.

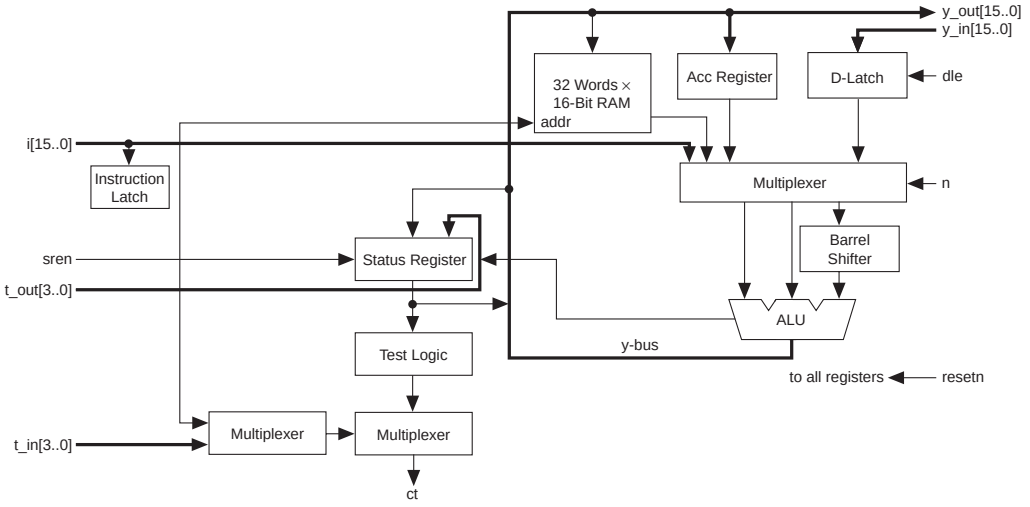
Modifiable Parameters

The C29116A 16-bit microprocessor megafunction can be customized to include a larger data width. Contact CAST directly for any required modifications.

Block Diagram

Figure 14 shows the block diagram for the C29116A 16-bit microprocessor.

Figure 14. C29116A 16-Bit Microprocessor Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	1,119	3	22 MHz	Data width = 16 bits
EPF10K20	-3	1,131	3	10 MHz	Data width = 16 bits
EPF6024	-2	1,198	–	9 MHz	Data width = 16 bits

DMA Controller

Vendor: CAST
Target Application:
PCI-based or CPU-based systems
Additional Deliverables:
VHDL RTL source code, testbench and test vectors, synthesis and simulation scripts
ID Code: 2AA5-C018

- Two independent fully programmed DMA channels
- Memory-to-memory, memory-to-peripheral, and peripheral-to-memory data transfers
- Single- or dual-address transfers, 8 or 16 transfers
- 16-bit data bus, 24-bit address bus
- Flexible request generation: Internal maximum rate or limited rate, external cycle steal or burst
- Two 16-bit transfer counters
- Operand packing and unpacking for dual-address transfers
- Supports all M68000 bus termination modes (DTACK, BERR, HALT)
- Provides full DMA handshake for burst and cycle steal transfers
- Allows M68000 devices to supersede DMA activity

General Description

The two-channel DMA controller megafunction is designed to complement the performance and architectural capabilities of the M68000 family of microprocessors by moving blocks of data in a quick, efficient manner with minimum intervention from a processor.

The bus interface of the DMA controller megafunction was designed in accordance with the M68000 bus specification.

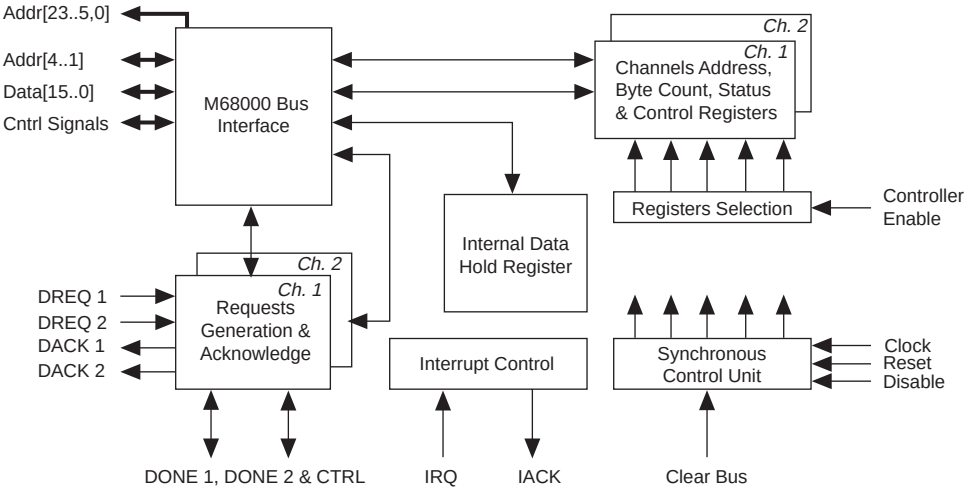
Modifiable Parameters

The DMA controller megafunction can be customized to include additional channels. Contact CAST for any required modifications.

Block Diagram

Figure 15 shows the block diagram for the DMA controller megafunction.

Figure 15. DMA Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	1,353	0	24 MHz	2 channels
EPF10K30	-3	1,353	0	14 MHz	2 channels
EPF6024	-2	1,510	–	13 MHz	2 channels

DMA Controller

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Documentation
ID Code: 2107-0661

- General-purpose DMA controller
- Up to 16 DMA channels
- Supports both synchronous and asynchronous DMA transfers
- Designed for PCI and other CPU bus systems

General Description

The DMA controller megafunction is designed for data transfer in different system environments. Two module types—type 0 and type 1—are provided, and the user can choose the number of each module type. Type 0 modules are designed to transfer data residing on the same bus, and Type 1 modules are designed to transfer data between two different buses. Each module can support up to 4 DMA channels; the megafunction supports up to 16 total DMA channels.

Each DMA channel can be programmed for various features, such as transfer size, synchronized and unsynchronized transfer control, transfer priority, interrupt generation, memory and IO address space, and address change direction. This megafunction is designed to work with 32-bit and 64-bit bus systems, including the PCI bus, PowerPC bus, and other CPU host buses. It can also be integrated with other megafunctions to form a complete functional block.

This megafunction is available in Altera Hardware Description Language (AHDL), Verilog HDL, VHDL, and netlist format.

Modifiable Parameters

Eureka Technology can customize the parameters shown in the following table according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

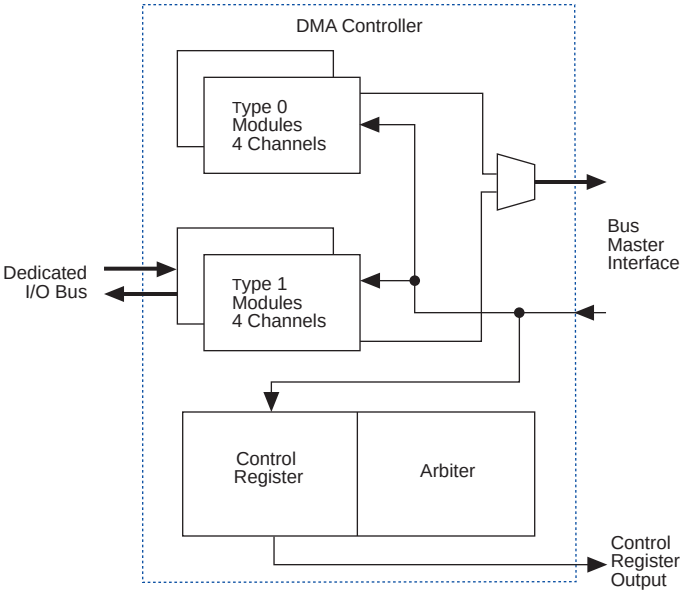
Modifiable Parameters

Parameter	Description
N	Number of channels
WIDTH	Width of the I/O bus

Block Diagram

Figure 16 shows the block diagram for the DMA controller megafunction.

Figure 16. DMA Controller Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10	-3	100	0	50 MHz	N = 1, WIDTH = 32 bits
EPF6016	-3	100	–	50 MHz	

PowerPC Bus Arbiter

Vendor: Eureka Technology
Target Application:
All PCI-based systems
Additional Deliverables:
Documentation
ID Code: 2107-0300

- Compatible with all PowerPC bus architectures
- Manages up to 8 bus masters
- Supports address pipelining, address only transaction, address retry, and separate address and data bus tenure
- Fixed and rotating priority

General Description

The PowerPC bus arbiter megafunction arbitrates the PowerPC address and data buses to allow multiple bus masters or processors to co-exist on the host bus. The megafunction is designed for the PowerPC host bus and works with all PowerPC CPU families and embedded controllers. The megafunction can be used as a stand-alone function or it can be incorporated in the same device with the bus master or slaves. Both fixed and round-robin priority schemes can be implemented with the arbiter.

To maximize system performance, the megafunction supports advanced features of the PowerPC bus, such as address pipelining, address retry, bus parking, and separate arbitration for the address and data buses. The megafunction allows address pipelining with two outstanding memory accesses.

The megafunction is available in AHDL, Verilog HDL, VHDL, and netlist format. Megafunction sizes vary with customization and with feature changes. Contact Eureka Technology directly for an LE count that is based on user specifications.

Modifiable Parameters

Eureka Technology can customize the parameters shown in the following table according to specific user requirements. Contact Eureka Technology or visit their web site for more information.

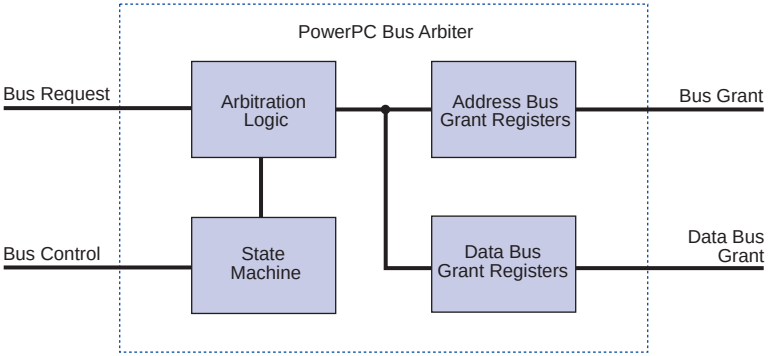
Modifiable Parameters

Parameter	Description
N	Number of ports: 4 or 8
AS	Architecture scheme: fixed priority, rotating priority, or user-specific priority
BP	Bus parking: highest priority or most recently used priority

Block Diagram

Figure 17 shows the block diagram for the PowerPC bus arbiter megafunction.

Figure 17. PowerPC Bus Arbiter Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EFP10K10	-3	110	0	50 MHz	8 ports, fixed-priority architecture scheme, and highest-priority bus parking
EPF6016	-2	110	–	50 MHz	
EPM7128	-1	70	–	66 MHz	

C6850 ACIA

Vendor: CAST
Target Application:
Serial data communications applications, modem interface
Additional Deliverables:
VHDL testbench, VHDL simulation files, user guide
ID Code: 2AA5-C005

- Programmable data word length, parity, and stop bits
- Parity, overrun, and framing error checking instructions and counting loop interactions
- Functionally based on the Motorola MC6850 device with improved transmission rates over the 1.0 Mbps specification
- False start bit deletion
- Peripheral modem control functions
- C6850 megafunction is licensed from MOXSYN S.R.L.

General Description

The C6850 asynchronous communications interface adapter (ACIA) megafunction provides asynchronous serial communication to the MC6800 processor family.

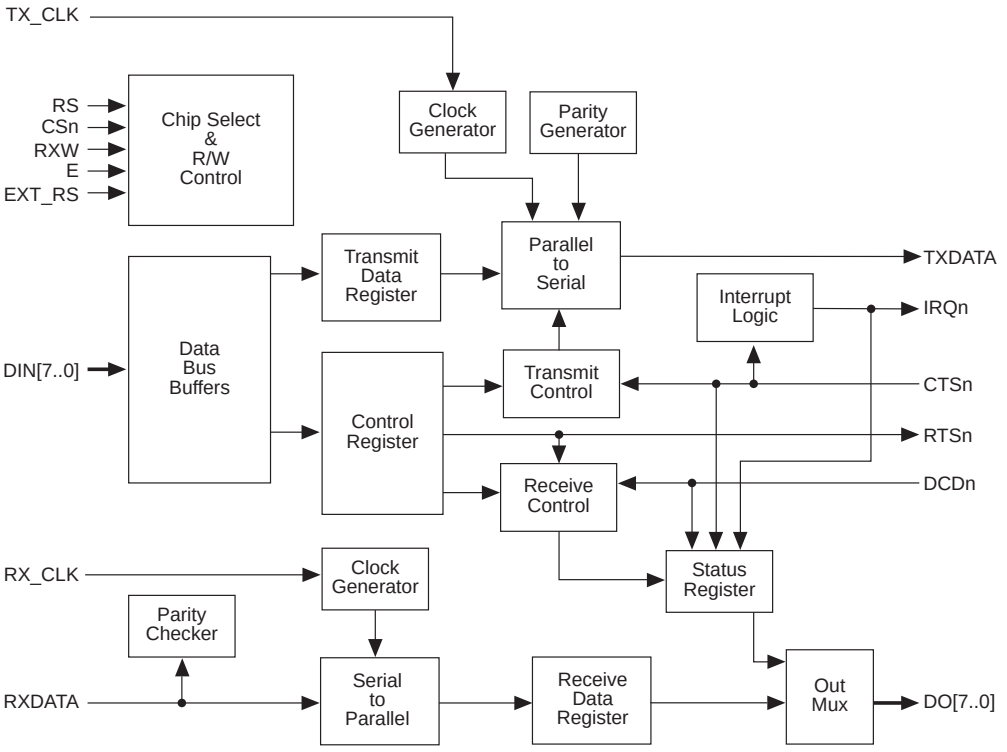
The megafunction has select, enable, read/write, interrupt, and bus interface logic features that allow data transfers over an 8-bit bidirectional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data.

In addition, a programmable control register provides the megafunction with a transmit control, a receive control, an interrupt control, variable word lengths, and clock division ratios. Three control lines are provided for peripheral or modem operation.

Block Diagram

Figure 18 shows the block diagram for the C6850 ACIA megafunction.

Figure 18. C6850 ACIA Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance *Note (1)*	Parameter Setting
		Logic Cells	EABs		
EPF10K10A	-1	185	0	TX: 74 MHz RX: 106 MHz	Contact CAST
EPF6016	-2	185	–	TX: 54 MHz RX: 38 MHz	Contact CAST

Note:
(1) TX is the transmit clock frequency and RX is the received clock frequency.

C8251 Programmable Communications Interface

Vendor: CAST
Target Application:
Serial data communications applications, modem interface
Additional Deliverables:
VHDL testbench, VHDL simulation files, user guide
ID Code: 2AA5-C012

- Synchronous and asynchronous operation
- Programmable data word length, parity, and stop bits
- Parity, overrun, and framing error checking instructions and counting loop interactions
- Functionality based on the Intel 8251A device
- Increases transmission rates up to 1.750 Mbps
- Divide-by-1, -16, and -64 mode
- False start bit deletion
- Automatic break detection
- Internal and external synchronous character detection
- Peripheral modem control functions
- C8251 megafunction is licensed from MOXSYN S.R.L.

General Description

The C8251 programmable communications interface megafunction provides data formatting and control to a serial communication channel.

The megafunction has select, read/write, interrupt, and bus interface logic features that allow data transfers over an 8-bit bidirectional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data, supporting both synchronous and asynchronous operation.

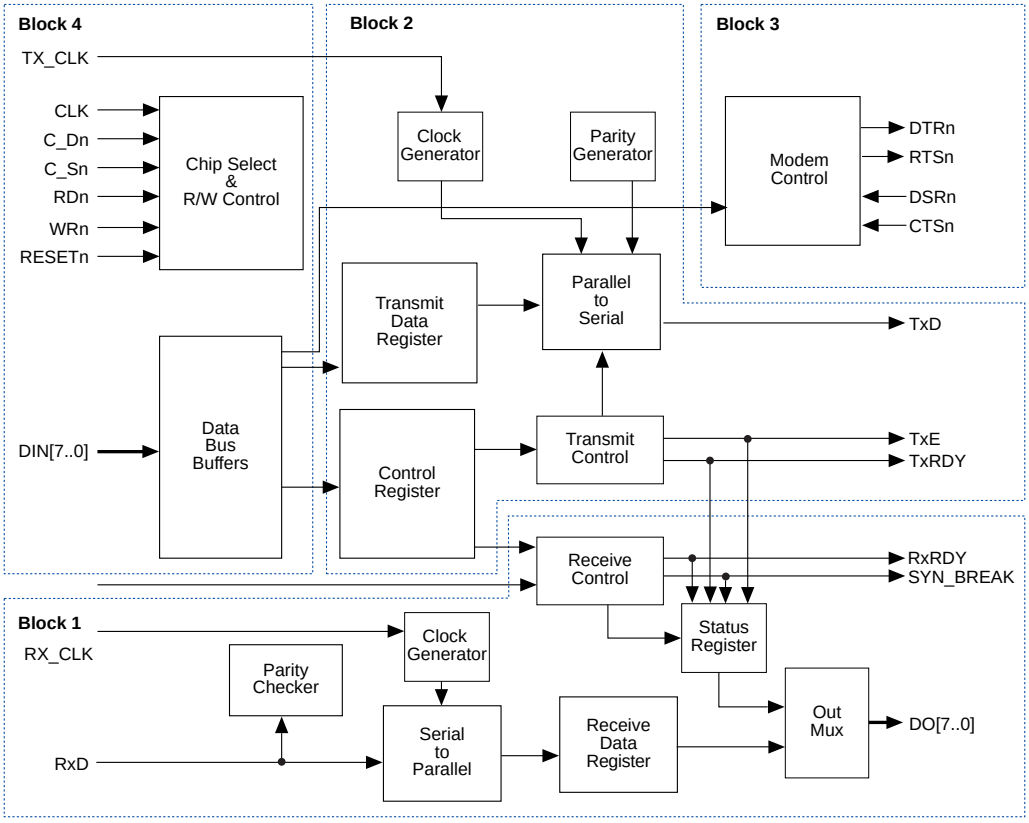
Modifiable Parameters

The C8251 megafunction can be customized to include a 16-bit internal baud rate generator. Either the synchronous or asynchronous sections can be removed to reduce the overall logic utilization. Contact CAST directly for any required modifications.

Block Diagram

Figure 19 shows the block diagram for the C8251 programmable communications interface megafunction.

Figure 19. C8251 Programmable Communications Interface Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance *Note (1)*	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	525	0	TX: 32 MHz RX: 32 MHz	No baud rate generator

Note:

(1) TX is the transmit clock frequency and RX is the received clock frequency.

C16450 UART

Vendor: CAST
Target Application:
Serial data communications applications, modem interface
Additional Deliverables:
VHDL testbench, VHDL model, user guide
ID Code: 2AA5-C011

- Full double buffering
- Independently controlled transmit, line status, receive, and data set interrupts
- Programmable data word length (5 to 8 bits), parity, and stop bits
- Parity, overrun, and framing error checking
- Increases transmission rates up to 1.5 Mbps
- Programmable baud rate generator allows division of any reference clock by 1 to ($2^{16} - 1$) and generates an internal 16× clock
- False start bit detection
- Automatic break generation and detection
- Internal diagnostic capabilities
- Peripheral modem control functions
- C16450 megafunction is licensed from MOXSYN S.R.L.

General Description

The C16450 megafunction provides asynchronous serial communication for the ISA bus and the Intel 80*x*86 processor. The megafunction has select, read/write, interrupt, and bus interface logic features that allow data transfers over an 8-bit bidirectional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data, supporting asynchronous operation.

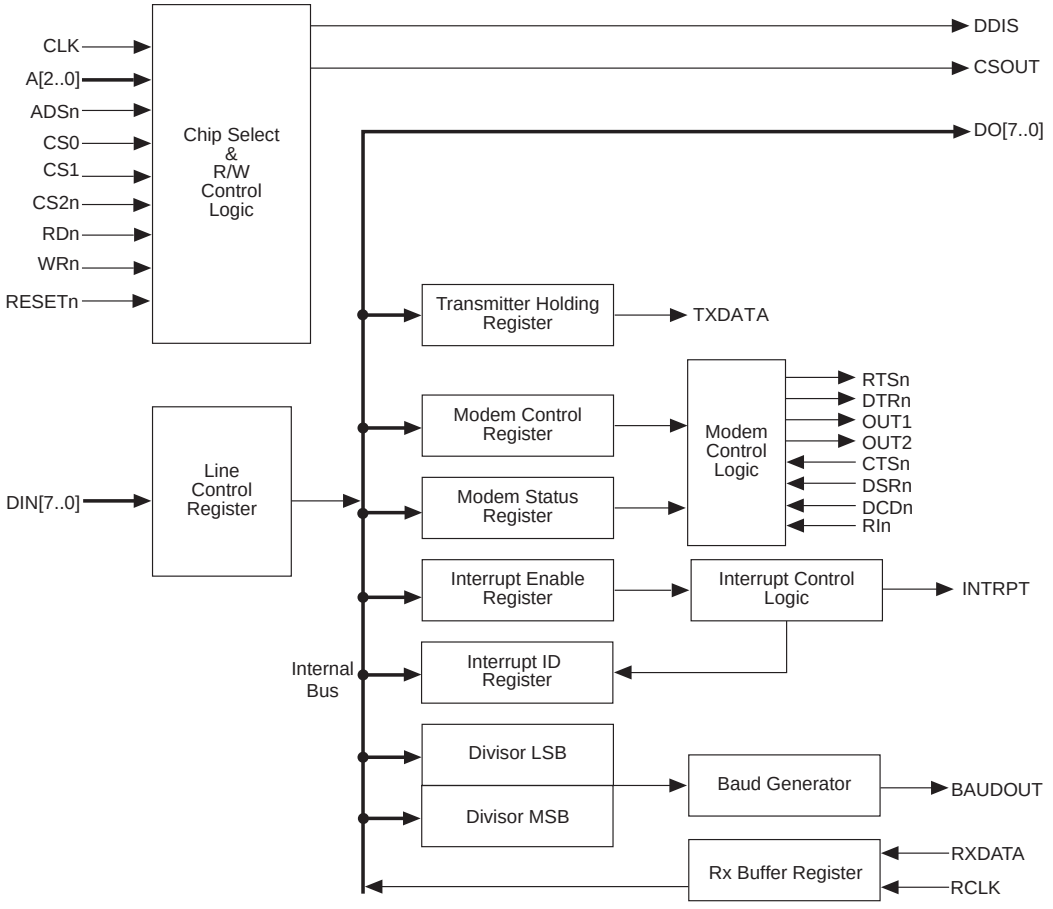
Modifiable Parameters

The C16450 megafunction can be customized to include a different CPU interface and to remove the internal baud rate generator.

Block Diagram

Figure 20 shows the block diagram for the C16450 UART megafunction.

Figure 20. C16450 UART Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance *Note (1)*	Parameter Setting
		Logic Cells	EABs		
EPF10K10A	-1	358	0	TX: 55 MHz RX: 52 MHz	Contact CAST

Note:
(1) TX is the transmit clock frequency and RX is the received clock frequency.

C16550 UART

Vendor: CAST
Target Application:
Serial data communications, modem interface
Additional Deliverables:
VHDL testbench, VHDL model
ID Code: 2AA5-C010

- In FIFO mode, the transmitter and receiver are each buffered with 16-byte FIFO buffers to reduce the number of CPU interrupts
- Programmable data word length (5 to 8 bits), parity, and stop bits
- Parity, overrun, and framing error checking
- Increased transmission rates up to 1.5 Mbps
- Programmable baud rate generator allows division of any reference clock by 1 to ($2^{16} - 1$) and generates an internal 16× clock
- False start bit detection
- Automatic break generation and detection
- Internal diagnostic capabilities
- Peripheral modem control functions
- Functionally based on the 16450 and 16550A devices
- C16550 megafunction is licensed from MOXSYN S.R.L.

General Description

The C16550 UART megafunction provides asynchronous serial communication for the ISA bus and the Intel 80*x*86 processor.

The megafunction has select, read/write, interrupt, and bus interface logic features that allow data transfers over an 8-bit bidirectional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data, supporting asynchronous operation.

Modifiable Parameters

The C16550 megafunction can be customized to include:

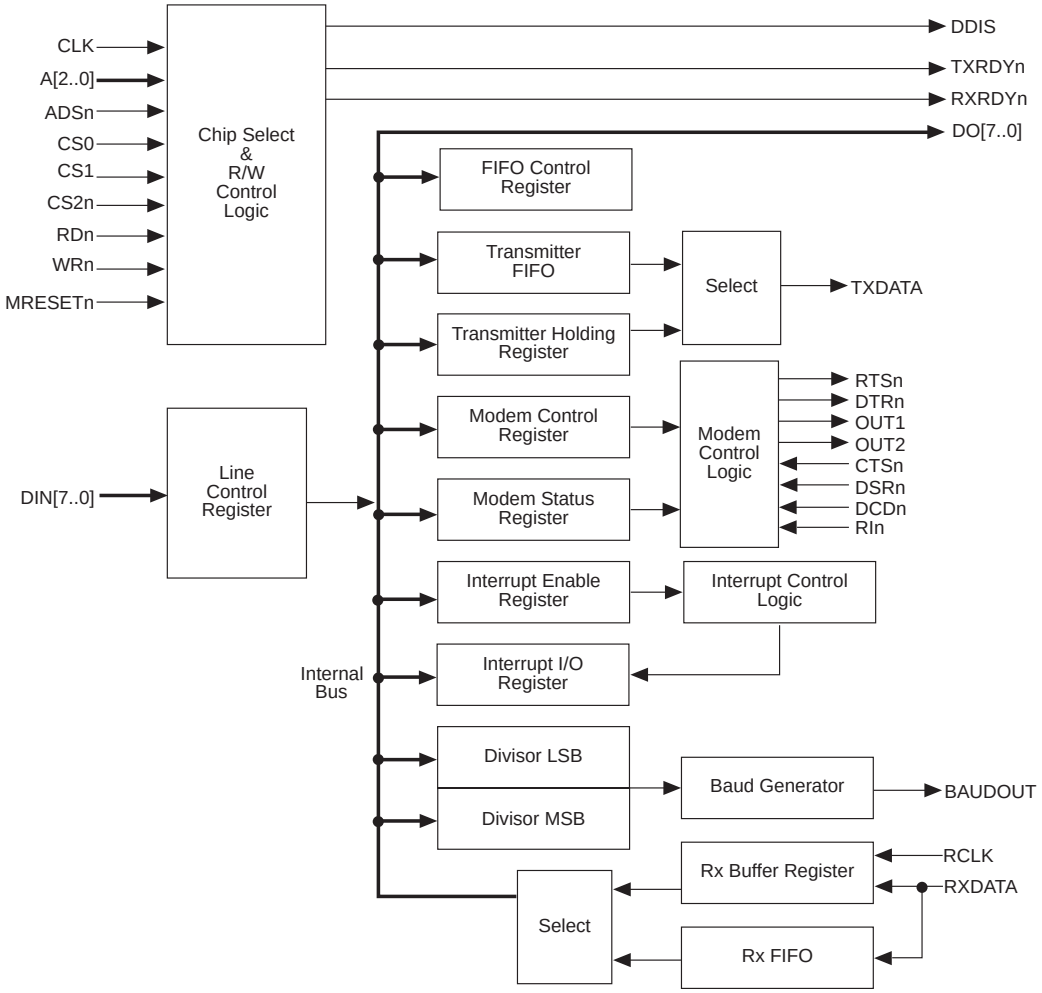
- Different FIFO sizes (separately for transmitter and receiver)
- Removal of internal baud rate generator
- Different CPU interface

Contact CAST directly for any required modifications.

Block Diagrams

Figure 21 shows the block diagram for the C16550 UART megafunction.

Figure 21. C16550 UART Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance *Note (1)*	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	1,099	0	TX: 27 MHz RX: 32 MHz	Contact CAST

Note:
(1) TX is the transmit clock frequency and RX is the received clock frequency.

C_UART

Vendor: CAST
Target Application:
Serial data communications applications
Additional Deliverables:
VHDL testbench
ID Code: 2AA5-C004

- 8-bit characters
- (T × C)/(R × C) 16 times the desired output baud rate
- One start bit and one stop bit
- Polling and interrupt modes
- Flexibility for adding other features
- Developed in VHDL
- C16550 megafunction is licensed from MOXSYN S.R.L.

General Description

The C_UART megafunction is a generic UART that can be used to implement a peripheral data communication device. The designer can program the megafunction with an 8-bit CPU.

A single clock input is provided for transmitting and receiving data. This clock frequency should be 16 times the data rate. The receive data line is receives input data in serial format. Synchronization with a clock for detection of data is accomplished internally. The transmit data output line transfers serial data to other peripherals.

The RxReady signal can be used as a receive interrupt (active low). A low level on this line indicates that the data has been received and the status register bit 0 is low. This interrupt can be cleared by reading data or by resetting the megafunction. The TxREADY signal can be used as a transmit interrupt (active low). A low level on this line indicates that the data has been transmitted, the transmit buffer is empty, and the status register bit 1 is low. This interrupt can be cleared by writing data or by resetting the megafunction.

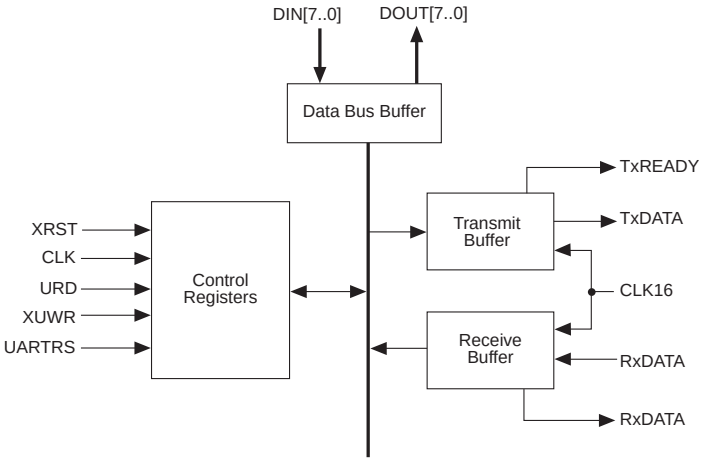
Modifiable Parameters

CAST can modify the megafunction's transmit buffer size, receive buffer size, character length, parity, and number of start and stop bits to meet user specifications.

Block Diagram

Figure 22 shows the block diagram for the C_UART megafunction.

Figure 22. C_UART Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10A	-1	87	0	169 MHz	Character length = 8, Number of start and stop bits = 2, Parity = On
EPF6016	-2	87	–	56 MHz	
EPM7160	-10	58	–	63 MHz	

eXtended MIDI (XMidi)

Vendor: Digital Design & Development
Target Application: Musical instruments
Additional Deliverables: Source code, evaluation board (XM-PC development kit)
ID Code: 1A91-B2F4

- Fully compatible with any musical instrument digital interface (MIDI) device
- 324 channels
- 510 linear resolution values (e.g., level and velocity)
- Automatic high-speed mode
- 4,374 non-linear values (e.g., control number and program change)
- 2,611 different instructions (i.e., opcodes)
- Bidirectional within TX line alone
- XMidi and MIDI files are cross compatible

General Description

Xmidi, also referred to as XM or Extended MIDI, is a proposed hardware-chip/software system that is designed to significantly enhance the capabilities of MIDI without losing or changing the current specification.

The XMidi megafunction is a combination of hardware and software to overcome the limitations of the current MIDI system. Cabling is done with ordinary MIDI cables and needs no interface or adapter of any kind. The XMidi megafunction uses ternary instead of binary logic to pack more data into the same message framing structure as used by the current MIDI. The main advantage of the XMidi megafunction is to bring denser data transmission and new message capabilities without losing compatibility. Channels now have extension subchannels, giving a total of 324 addressable devices per line.

Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	260	0	71 MHz	Contact Digital Design & Development

Telecom & Datacom

June 1998

Overview

Telecommunication and data communication (telecom and datacom) megafunctions provide networking building blocks to improve system performance. These megafunctions are ideal for a wide variety of networking applications, ranging from switches and routers to bridges and integrated services digital network (ISDN) terminal adapters. Typically, networking systems require high performance and the flexibility to scale a design to fit different speed rates. Using Altera® programmable logic devices (PLDs) and these Altera Megafunction Partners Program (AMPP℠) megafunctions, designers can meet the speed, density, and flexibility demands of their networking applications.

Contents

The telecom and datacom section contains the following functions:

HDLC Controller with M6800 Interface

Vendor: CAST
Target Application:
Data link controllers and protocol generators, digital sets, private branch exchanges (PBXs) and private packet networks, D-channel controller for ISDN basic access
Additional Deliverables:
VHDL testbench
ID Code: 2AA5-C015

- Motorola M6800 microprocessor interface
- Formats data as per X.25 (CCITT) level-2 standards
- Single-byte address recognition
- Microprocessor port and directly accessible registers for flexible operation and control
- Parameterizable first-in first-out (FIFO) buffer in both send and receive paths
- Handshake signals for multiplexing data links
- High-speed serially clocked output
- Facility to disable protocol functions
- Licensed from Hantro Products Oy

General Description

The high-level data link controller (HDLC) controller megafunction handles bit-oriented protocol structures, and formats the data as per the packet switching protocol defined in the X.25 (level 2) recommendations of the CCITT. The megafunction transmits and receives packed data (i.e., information or control data) serially in the format shown below, while providing the data transparency by zero insertion and deletion.

Flag	Address Field	Data Field	FCS	FLAG
One Byte	Optional	*N* Bytes ($N \geq 2$)	Two Bytes	One Byte

The HDLC controller megafunction generates and detects flags, various link channel states, and the abort sequence. Further, it provides a cyclic redundancy code check on the data packets using the CCITT-defined polynomial. In addition, the megafunction recognizes a single-byte address in the received frame. The megafunction includes a provision to disable the protocol functions and provide transparent access to the serial bus through the parallel port.

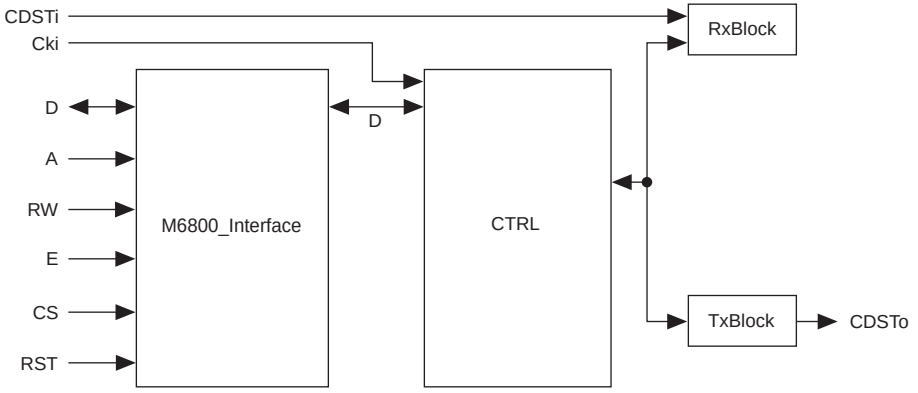
Modifiable Parameters

CAST can modify the size of the megafunction's transmit and receive FIFO buffers. The bit rate can be programmed to be equal to the clock or to be divided by two.

Block Diagram

Figure 1 shows the block diagram for the HDLC controller megafunction.

Figure 1. HDLC Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	1,447	0	21 MHz	Phase accumulator width = 24 bits Output data width = 8 bits

HDLC Controller

Vendor: Integrated Silicon Systems
Target Application: X.25, frame-relay, ISDN B-channel and D-channel
Additional Deliverables: Behavioral VHDL testbench
ID Code: C38B-1119

- Single- and double-byte address recognition
- 16-bit (CRC-16) and 32-bit (CRC-32) frame check sequence
- Asynchronous 8-bit input data interface, suitable for a wide range of FIFO buffers
- Compatible with International Telegraphy Union (ITU) recommendation Q.921
- Serial interface with external clocking for interfacing to the PCM-highway
- Transmission is synchronous to network interface with back pressure mechanism. Buffering at the network interface not required
- Supports transparent mode
- Supports modular scaling of multiple HDLC channels through parallel cores or core multiplexing
- Supports data rates up to 20 Mbits/second

General Description

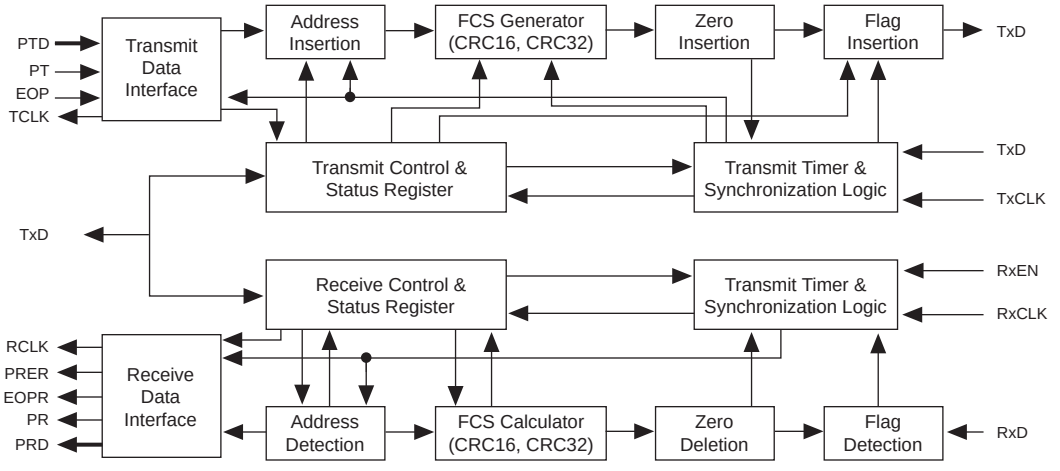
The ISS HDLC controller megafunction is a high-performance, third-level, soft-core module for the bit-oriented packet transmission mode. The megafunction is suitable for frame-relay, X.25, ISDN B-channel (64 Kbits/second), and D-channel (16 Kbits/second). The megafunction fulfills the specification according to the ITU Q.921, X.25 level 2 recommendation.

The data stream and transmission rate are controlled from the network node (PCM highway clock) with a back-pressure mechanism. This function eliminates additional synchronization and buffering of the data at the network interface. The data interface is 8-bits wide and asynchronous, and includes an 8-bit synchronization buffer. The megafunction provides basic adaptation for a wide range of FIFO buffers. It can be used as a single-channel HDLC protocol controller or as a switched parallel core used to implement an *N*-multiple channel controller. The high throughput and modular structure also enables multiplexing of the megafunction between channels for low data rate applications.

Block Diagram

Figure 2 shows the block diagram for the HDLC controller megafunction.

Figure 2. HDLC Controller Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance *Note (1)*	Parameter Setting
		Logic Cells	EABs		
EPF10K10A	-1	405	0	72 MHz	Contact ISS

Note:
(1) Contact ISS for design optimization and highest performance results.

Multi-Standard ADPCM

Vendor: Integrated Silicon Systems
Target Application: Overload voice channels in digital circuit multiplication equipment (DCME), data modems for DCME, packetized voice protocol (PVP) systems
Additional Deliverables: Simulation file, constraint file, user guide
ID Code: C38B-AD4E

- Compliant with G.721, G.723, G.726, G.726a, G.727, and G.727a ITU standards
- Coding 64 Kbits/second to and from 40, 32, 24, and 16 kbits/second
- Support for both A-and Mu-law pulse-code modulation (PCM) coding
- Support for up to 20 full duplex channels, and 40 encode or decode channels

General Description

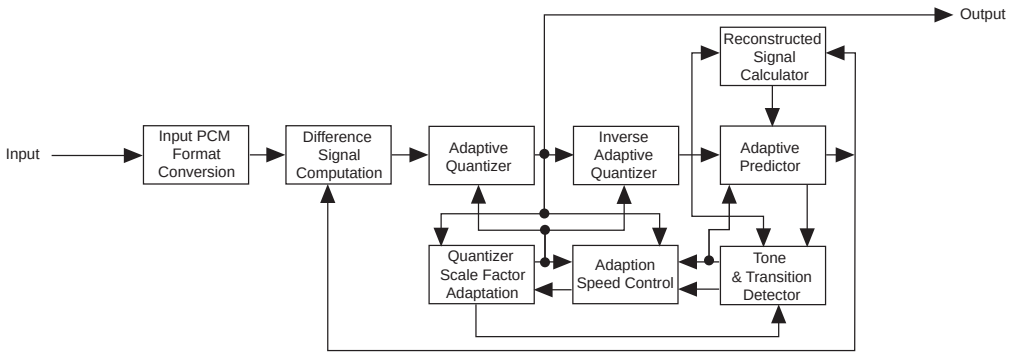
The multi-standard adaptive pulse code modulation (ADPCM) megafunction performs multi-channel duplex ADPCM coding in telecommunications applications. If the designer requires only a subset of the megafunction's capabilities, the Altera MAX+PLUS® II software will remove unused logic during logic synthesis. This feature improves device utilization and facilitates system development and prototyping on a FLEX® 10K device.

The multi-standard ADPCM megafunction's functionality and timing are verified using ITU standard test sequences. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Block Diagram

Figure 3 shows the block diagram for the multi-standard ADPCM megafunction.

Figure 3. Multi-Standard ADPCM Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100A	-1	3,942	9	9 MHz	16 channels, full duplex coding with all standards and coding rates, and PCM laws

Speedbridge

Vendor: SIS Microelectronics
Target Application:
Network communication, interface
Additional Deliverables:
Documentation, Verilog HDL register transfer language (RTL) sources
ID Code: 7D0E-5BA1

- Elastic FIFO buffer for bridging data between various speed domains
- User-parameterizable width and depth
- Provides full/empty status flags
- Independently clocked input and output interfaces
- Register based
- Full/empty status flags

General Description

The speedbridge megafunction is a speed-matching FIFO buffer that transfers data across an asynchronous interface. The read and write ports have independent clocks and synchronous enables for accessing their respective functions. These features allow the clocks to run without read or write operations occurring.

The speedbridge megafunction eliminates the need for an external asynchronous FIFO buffer, which minimizes system development and debugging time and reduces development cost and risk in design.

Modifiable Parameters

The following megafunction parameters can be modified:

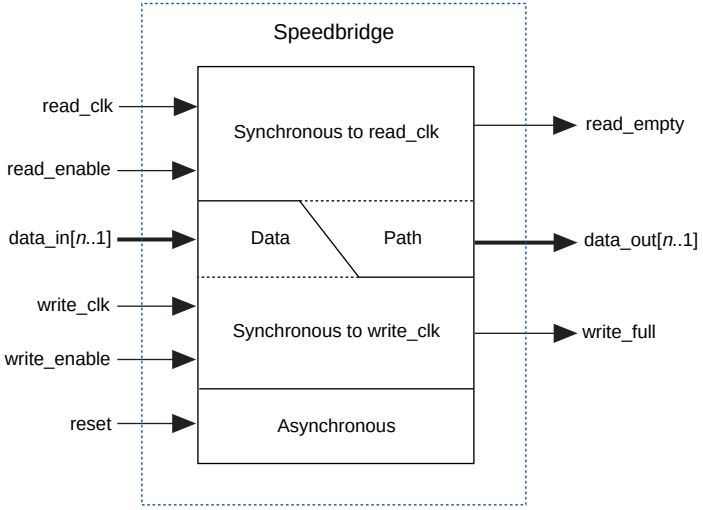
Modifiable Parameters

Parameter	Description
DEPTH	Number of words
WIDTH	Width of data bus

Block Diagram

Figure 4 shows the block diagram for the speedbridge megafunction.

Figure 4. Speedbridge Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance *Note (1)*	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	424	0	R: 108 MHz W: 126 MHz	Contact SIS Microelectronics

Note:
(1) R = Read clock frequency; W = Write clock frequency.

Telephony Tone Generation (ToneGen)

Vendor: NComm, Inc.
Target Application:
PBX, T-1 trunk signaling, SS7 path verification, DTMF tones
Additional Deliverables:
Test vectors
ID Code: 423E-7212

- Generates single- and dual-frequency tones used in telephony applications
- Outputs ST-Bus, IOM-2, IDL, and other standard-compatible serial streams containing from 1 to 32 tones
- Supports both Mu-Law and A-Law encoding algorithms
- Provides fully configurable gain control for individual tones and for each frequency component that makes up a tone
- Parameterization via the MegaWizard™ Plug-In features tone creating, tone editing, and tone testing using a sound-capable computer

General Description

The tone generation (ToneGen) megafunction is a Mitel ST-Bus-compatible device providing from 1 to 32 user-programmable tones used in telephony applications. The ToneGen megafunction can generate any combination of single- and/or dual-frequency tone sequences, such as dialtone, ringback, busy, DTMF, SS7 path validation, MF, and any other custom tone sequence. The ToneGen megafunction supports gain control, Mu-law or A-law encoding, and other parameters on a tone-by-tone basis, providing complete control over the tones being generated. Because the megafunction is parameterized with the MegaWizard Plug-In, the ToneGen megafunction allows users to configure new tones, edit existing tones, listen to generated tones on a sound-capable computer, and minimize the ROM storage required to contain the tones. The Altera MegaWizard Plug-In provides a simple and powerful way to add tone generation to telephony or other applications.

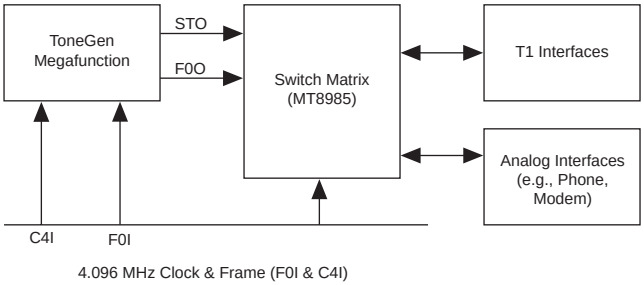
Modifiable Parameters

The ToneGen megafunction can be customized to create different tones. With the associated MegaWizard Plug-In, users can create virtually any set of tones required by the target application. In addition, the MegaWizard Plug-In allows users to minimize the number of embedded array blocks (EABs) required to synthesize a set of tones by calculating the least number of PCM samples required to generate the desired tone sequences.

Block Diagram

Figure 5 shows the block diagram for the ToneGen megafunction.

Figure 5. Telephony Tone Generation Megafunction Block Diagram



Device Utilization Examples

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100	-4	445	6	23.14 MHz	MF tones 0 - 9, ST, and KP
		136	6	26.24 MHz	Dialtone, busy tone, and ringback
EPF10K50	-4	50	4	30.48 MHz	Dialtone
EPF10K20	-3	445	4	30.86 MHz	MF tones 0 - 9, ST, and KP
		136	6	26.24 MHz	Dialtone, busy tone, and ringback

UTOPIA Level 1: ATM Cell-Based Interface

Vendor: PLD Applications
Target Application: Local-area network (LAN) applications, wide-area network (WAN) ATM networks
Additional Deliverables: Simulation file, constraint files, development board, user guide, reference design
ID Code: 73 E2-F1F3

- Low complexity enables users to increase function integration and reduce the number of interoperability problems
- High-performance physical layer (PHY) was specifically developed for asynchronous transfer mode (ATM)
- Flexibility—Due to its aperiodic structure, the megafunction can operate at several bits
- Cell-based physical layer enables the megafunction to map ATM VPs on optical sections without using the SONET/SDH layer (WDM)

General Description

The UTOPIA level 1 ATM cell-based interface megafunction contains the functions listed below.

Transmitter

The transmit function performs the following actions:

- *Cell rate decoupling*. This function adapts the transfer capability to the interface rate (idle cells insertion/extraction).
- *Insertion of F1 and F3 OAM cells.* These cells are specific to the cell-based physical layer; they are used to carry the operation and maintenance (OAM) information, which includes maintenance signals S-RDI, P-RDI and P-AIS, performance information (BIP-8 computation), and reports of the number of errored blocks. This OAM information is compliant with ITU-T Recommendations G.826 and I.610, which define the maintenance and performance mechanisms for various transmission systems (PDH, SDH, and cell-based). F1 OAM cells apply to the section regenerator level, whereas F3 OAM cells apply to the transmission path.
- *Scrambling*. This function uses the distributed sample scrambler (DSS), which avoids imitation of the cell header pattern in the cell payload and helps randomize the transmitted data for improved transmission performance.
- *Header error control (HEC) computation.* The value of the HEC field is computed on the scrambled header before the cell is transmitted.

Receiver

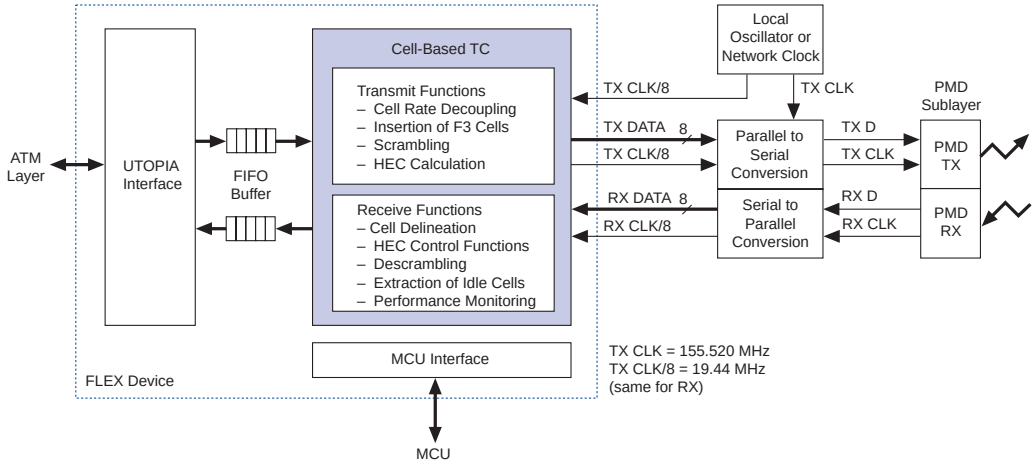
The receive function performs the following actions:

- *Cell delineation.* This function recovers the cell boundaries in the data flow by using the HEC syndrome in the cell header.
- *Descrambling*. Cells are descrambled by using the DSS.
- *Extraction of F1 and F3 OAM cells.* These cells are used for operation and performance monitoring functions.

Block Diagram

Figure 6 shows the block diagram for the UTOPIA level 1 ATM cell-based interface megafunction.

Figure 6. UTOPIA Level 1 ATM Cell-Based Interface Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100A	-1	2,160	0	20 MHz	Contact PLD Applications

UTOPIA Level 2: Master Receiver

Vendor: CoreEl MicroSystems
Target Application: ATM, router controller, switch interface
Additional Deliverables: Behavioral VHDL testbench, complete RTL
ID Code: C08E-20A1

CoreEl MicroSystems

- Cell-based interface
- 16-bit data bus
- 155 Mbits/second
- 25-, 33-, and 50-MHz UTOPIA level 2
- Supports as many as 32 ports
- Supports physical to logical address mapping
- Compliant with ATM Forum UTOPIA level 2, version 1.0

General Description

The UTOPIA level 2 master receiver megafunction receives ATM cells from receive UTOPIA slaves on the UTOPIA bus. The megafunction conforms to UTOPIA level 2 specifications and is configurable to work with a maximum of 31 ports. During cell transfers, the megafunction reads 16 bits of data every clock cycle. Then, it assembles the data into a 32-bit word and writes the word to the cell FIFO buffer corresponding to the PHY port.

The megafunction's ports are polled in round-robin fashion. The port ready status is generated from the `RxClav` signal. If the PHY is ready and the corresponding cell FIFO buffer is not full, the PHY is chosen for data transfer. Then, the PHY sends data to the cell FIFO buffer.

During data transfers, other ports are polled. Ports are polled every alternate cycle, and the address 1F appears between two port addresses so that the tri-stated signals have enough turnaround time. When a cell transfer is almost finished, the block checks if other ports are available for transfer. If other ports are available, the next port is chosen in round-robin fashion. Otherwise, the current port is kept selected for one more cycle and then deselected. If the current port has one more cell, it responds with a `RxSOC` signal in the next cycle. Then, the current port must be selected again and the next cell transfer must be completed. This transfer sequence is called an unexpected back-to-back situation.

If no other ports are available or the current port's FIFO buffer is full, the port is deselected immediately. This action prevents an unexpected back-to-back transfer.

The port ID used throughout the megafunction is the logical port ID, which is translated to the physical PHY device ID before being clocked on the `RxAddr` bus.

Modifiable Parameters

The following megafunction parameters can be modified:

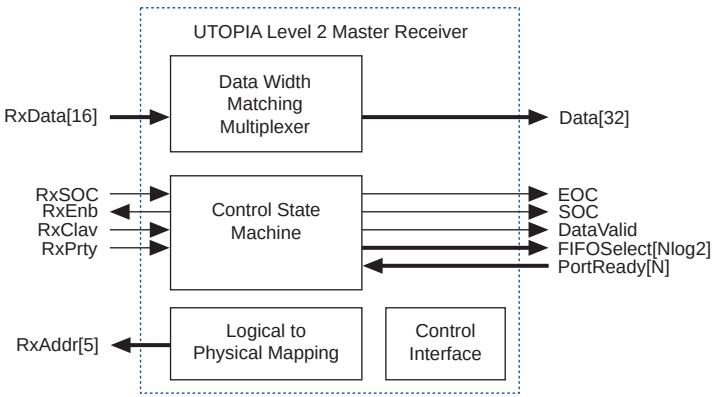
Modifiable Parameters

Parameter	Description
P	Number of data cell ports the block will handle
PB	Number of bits needed to encode P (log base 2 of P)

Block Diagram

Figure 7 shows the block diagram for the UTOPIA level 2 master receiver megafunction.

Figure 7. UTOPIA Level 2 Master Receiver Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	528	0	65 MHz	P = 4, PB = 2

UTOPIA Level 2: Master Transmitter

Vendor: CoreEl MicroSystems
Target Application: ATM, router controller, switch interface
Additional Deliverables: Behavioral VHDL testbench, complete RTL documentation
ID Code: C08E-40A1

CoreEl MicroSystems

- Conforms to UTOPIA level 2 specifications
- Provides access to internal registers via the controller interface
- Provides a mapping mechanism for assigning any logical port number to a physical port
- Provides a 32-bit data bus for data transfer from the ATM layer
- Polls the logical ports according to round-robin discipline
- Generates parity for the data going to the PHY device
- Inserts dummy HECs in the cell going to the PHY device

General Description

The state machine polls the available PHY ports serially and stores the polling status. On the cell FIFO side, each FIFO buffer sends one bit of information indicating that it is ready to transmit one cell. Then, a port is chosen for cell transmission from those ports ready to accept a cell and have the corresponding cell FIFO buffer ready. When the cell transfer is almost finished, the state machine looks for next port transmission in round-robin fashion. If no other port is available and the current port's FIFO buffer has one more cell to transmit, the next cell's transmission starts immediately after the current cell transmission is over.

Each cell FIFO buffer sends data to the megafunction via the 32-bit data bus. The data width matching multiplexer module accepts data from all FIFO buffers and chooses the appropriate data. This data is sent on the `TxData` bus to the PHY device, 16-bits at a time. The logical to physical mapping module has a look-up table (LUT) that can be programmed through the control interface. After choosing a port for selection or polling, the port address is converted to the corresponding physical address and then placed on the `TxAddr` bus. This sequence allows flexibility in allocating an arbitrary physical address to a set of logical addresses.

Modifiable Parameters

The following megafunction parameters can be modified:

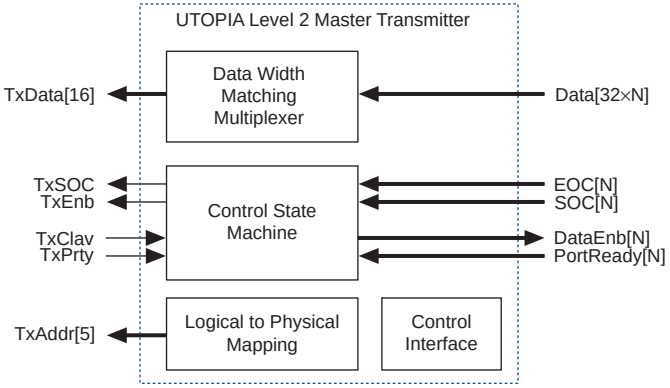
Modifiable Parameters

Parameter	Description
P	Number of data cell ports the block will handle
PB	Number of bits needed to encode P (log base 2 of P)

Block Diagram

Figure 8 shows the block diagram for the transmit UTOPIA level 2 master transmitter megafunction.

Figure 8. UTOPIA Level 2 Master Transmitter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	449	0	82.64 MHz	P = 4, PB = 2

UTOPIA Level 2: Slave Receiver

Vendor: CoreEl MicroSystems
Target Application: ATM, router controller, switch interface
Additional Deliverables: Behavioral VHDL testbench, RTL documentation
ID Code: C08E-30A1

CoreEl MicroSystems

- Cell-based interface
- 16-bit data bus
- 622 Mbits/second
- 25-, 33-, and 50-MHz UTOPIA level 2
- Supports as many as 32 ports
- Supports physical to logical address mapping
- Compliant with ATM Forum UTOPIA level 2, version 1.0

General Description

The UTOPIA level 2 slave receiver megafunction supports multiple PHY operation and transmits data on the UTOPIA bus. The cell FIFO buffer receives data in a 32-bit double-word format, and then sends it to the UTOPIA bus in a 16-bit word format.

The UTOPIA level 2 slave receiver megafunction has a cell-based interface, and it can support as many as 32 ports. A UTOPIA level 2 master receiver megafunction polls the slave megafunction for the availability of cells in various ports through the polling interface. The master receiver megafunction presents the PHY address to check if any cells are available for that PHY port. Cell availability is solely dependent on the cell FIFO interface, which gives the port ready status. A port ready status indicates that the port has an outgoing cell. The `RxClav` signal is asserted when the cell FIFO interface asserts the port ready status. The cell FIFO buffer stores the outgoing cells on a per port basis.

The UTOPIA level 2 slave receiver megafunction works in a 54-byte mode and transfers take place on a 16-bit wide UTOPIA data bus. Twenty-six transfers occur for each cell. The HEC word, which is the third word in the transfer, is a dummy byte. The physical layer places the appropriate HEC byte in the cell.

Data is packed according to the standard transmission convention. The upper byte of the word is the first one on the line.

Physical to logical address mapping is supported through a set of configuration registers, which are programmed through a standard microprocessor interface.

Modifiable Parameters

The following megafunction parameters can be modified:

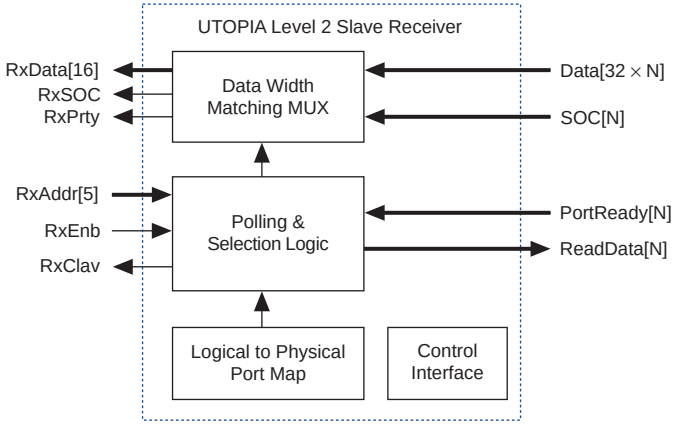
Modifiable Parameters

Parameter	Description
P	Number of data cell ports the block will handle
PB	Number of bits needed to encode P (log base 2 of P)

Block Diagram

Figure 9 shows the block diagram for the receive UTOPIA level 2 slave receiver megafunction.

Figure 9. UTOPIA Level 2 Slave Receiver Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	449	0	54 MHz	P = 4, PB = 2

UTOPIA Level 2: Slave Transmitter

Vendor: CoreEl MicroSystems
Target Application: ATM, router controller, switch interface
Additional Deliverables: Behavioral VHDL testbench, complete RTL documentation
ID Code: C08E-50A1

CoreEl MicroSystems

- Cell-based interface
- 16-bit data bus
- 622-Mbits/second
- 25-, 33-, and 50-MHz UTOPIA level 2
- Supports as many as 32 ports
- Supports physical to logical address mapping
- Compliant with ATM Forum UTOPIA level 2, version 1.0

General Description

The UTOPIA level 2 slave transmitter megafunction operates in a multi-PHY environment. It receives cells from the UTOPIA bus and assembles the data into 32-bit double words. Thereafter, the megafunction passes the data to the cell FIFO interface controller along with the appropriate port number. The `TxClav` signal generation is dependent on the cell FIFO interface controller. If the cell FIFO interface can accept a new cell when the master polls the megafunction, the `TxClav` signal is asserted.

The UTOPIA level 2 slave transmitter megafunction accepts 16-bit words on the UTOPIA bus and assembles them into double words before transferring them to the cell FIFO buffer. When a port is selected, the megafunction sends the assembled 32-bit data to the cell FIFO buffer and validates that data with a data enable signal.

The megafunction operates in a 16-bit UTOPIA data bus mode. There are 26 transfers for each cell transfer. The third word is masked because it is the HEC byte. The HEC check is performed by the physical layer device and data is packed in the standard way.

Physical to logical address mapping is supported through configuration registers that are programmable via the microprocessor interface.

Modifiable Parameters

The following megafunction parameters can be modified:

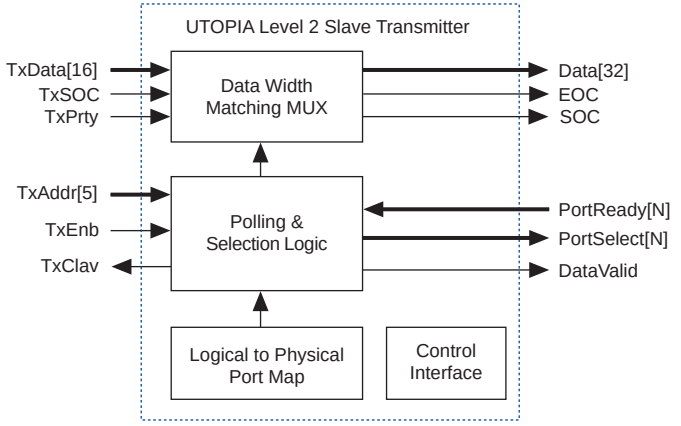
Modifiable Parameters

Parameter	Description
P	Number of data cell ports the block will handle
PB	Number of bits needed to encode P (log base 2 of P)

Block Diagram

Figure 10 shows the block diagram for the UTOPIA level 2 slave transmitter megafunction.

Figure 10. UTOPIA Level 2 Slave Transmitter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	323	0	88 MHz	P = 4, PB = 2

Notes:

June 1998

Overview

Historically, digital signal processing (DSP) applications have used only DSP processors, DSP-specific application-specific integrated circuits (ASICs), and application-specific standard products (ASSPs). Although DSP processors are flexible, they offer limited real-time performance. ASICs and ASSP devices are capable of real-time processing, but are limited in their adaptability and flexibility. On the other hand, DSP designs implemented in Altera® programmable logic devices (PLDs) combine the flexibility critical for product differentiation with the speed needed for high-performance applications, such as video convolution, radio frequency systems for cable networks, and spread-spectrum filtering. Because Altera FLEX® devices can be reconfigured, the entire DSP implementation flow can be rearranged. Further, algorithms that were traditionally regarded as a sequence of single instructions can be analyzed to determine possible parallelism. Additional deliverables—such as MATLAB simulation files, standard hardware description languages (HDLs), or development boards—further reduce time-to-market.

Contents

The DSP section contains the following functions:

Imaging

Error Correction

Filtering

Filtering *(Continued)*

Arithmetic

Framer

Standard Blocks

Discrete Cosine Transform

Vendor: Integrated Silicon Systems
Target Application: Multimedia systems, set-top boxes, video telephony systems, broadcast systems
Additional Deliverables: Simulation file, constraint file, user guide
ID Code: C38B-A263

- Fully parameterized megafunction
- Discrete cosine transform (DCT), inverse discrete cosine transform (IDCT), and combined DCT/IDCT variants available
- High performance
- Implements an 8 × 8 two-dimensional (2-D) DCT conforming to many image compression standards

General Description

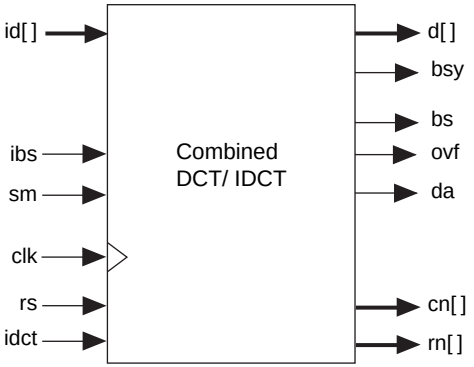
The DCT megafunction operates at sample rates of up to 50 MHz, and are fundamental building blocks for many image and video compression systems. Additional functionality ensures that the megafunctions are easy to use and reduces the need for extra circuitry in systems development. Parameter selection enables the megafunctions to comply with the following standards: H.261, H.263, Joint Photographic Experts Group (JPEG), Motion Pictures Expert Group (MPEG)-1, MPEG-2, and MPEG-4.

ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Block Diagram

Figure 1 shows the block diagram for the DCT megafunction.

Figure 1. DCT Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100	-3	4,386	0	17.45 MHz	8 × 8, 2-D DCT with 8-bit inputs, 8-bit outputs, 8-bit coefficient word lengths, and 12-bit internal precision

Laplacian Edge Detector

Vendor: Integrated Silicon Systems
Target Application: Video, broadcast systems
Additional Deliverables: Simulation files, VHDL template
ID Code: C38B-A264

- Bit parallel input and output data
- Unsigned binary input data format
- Parameterizable input data word lengths, which must be specified by the customer before delivery
- Two output data formats are available (two's complement or signed binary)
- Variants of the megafunction, which can handle input sample rates of up to 90 MHz, are available
- Asynchronous clear input signal

General Description

The Laplacian edge detector megafunction is a two-dimensional (2-D) filter targeted towards real-time front-end image processing applications. The input data words are bit-parallel unsigned binary format to suit the output of most video analog-to-digital converters (ADCs). To use the laplacien edge detector megafunction, the input data must be made available three vertically adjacent pixels at a time.

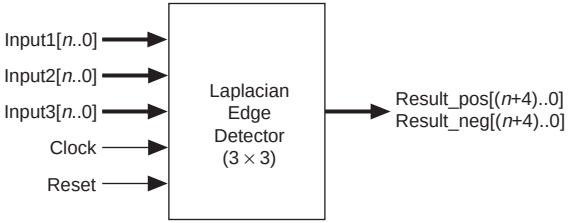
Modifiable Parameters

ISS can customize the input data word length (W) to meet user specifications.

Block Diagram

Figure 2 shows the block diagram for the Laplacian edge detector megafunction.

Figure 2. Laplacian Edge Detector Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	260	0	56 MHz	W = 8, 12

Convolutional Encoder

Vendor: Integrated Silicon Systems
Target Application: Cable modem, wireless communications, satellite communications
Additional Deliverables: Simulation file, constraint file, user guide
ID Code: C38B-D479

- High performance
- Highly parameterized
- Bit serial or symbol serial data input
- Complements other forward error correction (FEC) megafunctions from ISS

General Description

The convolutional encoder megafunction complements ISS's other FEC megafunctions (Reed-Solomon encoders and decoders, scramblers, descramblers, interleavers and deinterleavers, synchronous insertion and synchronous detection, and Viterbi decoders).

Modifiable Parameters

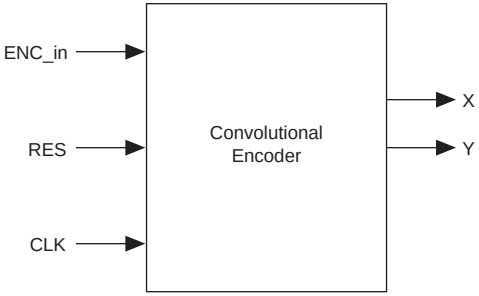
The convolutional encoder megafunction can be configured to use bit rate or symbol rate clocks, to accept the data in bit serial or symbol serial format, and to support a range of international standards. The following megafunction parameters can be modified:

- Performance
- Constraint length
- Code rate
- Generator polynomial
- Puncturing scheme
- Standards compliance

Block Diagram

Figure 3 shows the block diagram for the convolutional encoder megafunction.

Figure 3. Convolutional Encoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50	-3	39	0	120 MHz	K = 7, R = 1/3, 3/4 (punctured)

Convolutional Interleaver

Vendor: KTech Telecommunications
Target Application: Personal computer systems (PCS), cable modems
Additional Deliverables: Constraint file
ID Code: 52A2-4B52

- Convolutional interleaver function
- Bit byte is accepted at each clock cycle
- Interleaved 8-bit byte produced at each clock cycle

General Description

The convolution interleaver megafunction implements a convolutional interleaver that is optimized for personal communications systems (PCS) and cable modem applications. For small interleaving depth, the megafunction uses FLEX 10K embedded array blocks (EABs). For large interleaving depth, the megafunction requires an external dual-port RAM and ROM.

The megafunction accepts input signal 8 bits at a time. At each byte clock cycle, the input and output selector arms shift to the next set of data. When the final index *N* is reached, the selector arms go back to the initial index 1 arm, and the selector arms continue with each byte cycle. After the latency introduced by the interleaver, the output produces 8 bits at a time.

Modifiable Parameters

The following megafunction parameters can be modified:

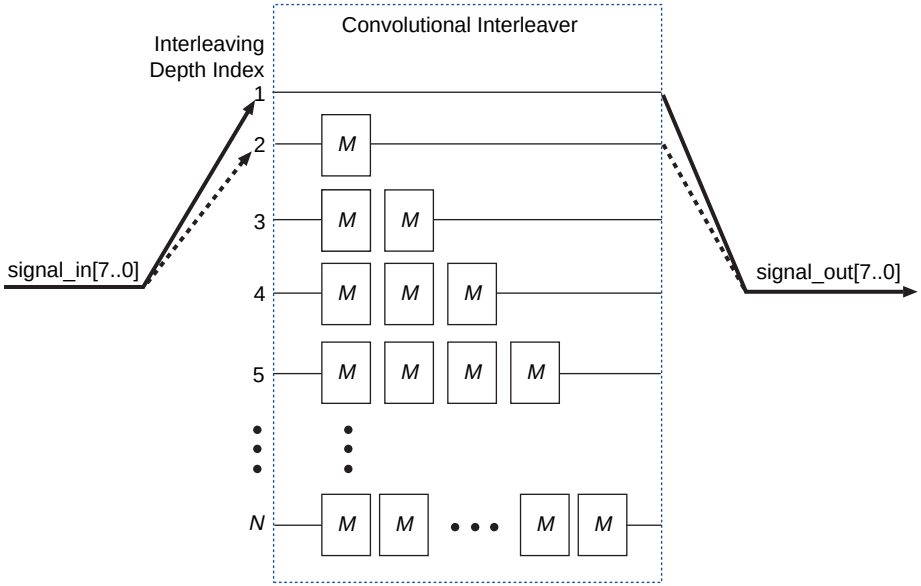
Modifiable Parameters

Parameter	Description
SI	Signal data input size
SO	Signal data output size

Block Diagram

Figure 4 shows the block diagram for the convolutional interleaver megafunction, in which *M* is the bit memory stage FIFO shift register size.

Figure 4. Convolutional Interleaver Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30	-3	252	0	52 MHz	SI = 8, S0 = 8

Reed-Solomon Decoder

Vendor: Hammer Cores
Target Application: Data communication, digital video broadcast
Additional Deliverables: DECRSV3 (an executable that automatically generates test vectors based on parameters)
ID Code: C4D5-FDEC

- High-speed decoder—typically 320 Mbytes per second (Mbps)
- Fully user parameterized

General Description

The Hammer Cores Reed-Solomon decoder megafunctions are high-performance, fully parameterized Reed-Solomon functions for programmable logic. The user can select any combination of parameters that define a Reed-Solomon code, and have a synthesized and routed function within minutes. Data throughput is typically in the range of 320 Mbps.

The megafunction processes codewords in a stream format, where it receives codewords and writes corrected codewords continuously. Utilities are included to generate the function description and to create test vectors based on a parameter list.

The megafunctions are optimized for Altera FLEX 10K devices. Overall resource requirements will vary widely with parameter specification, but are essentially linearly dependent on both the field size and number of check symbols.

Modifiable Parameters

The following megafunction parameters can be modified:

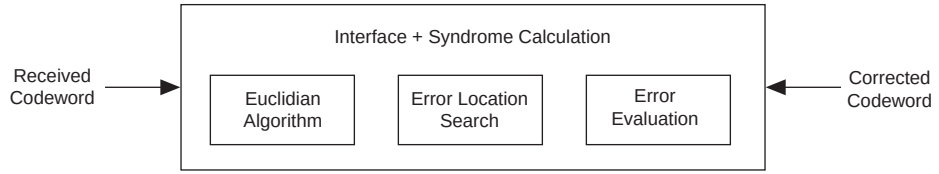
Modifiable Parameters

Parameter	Description
N	The total number of symbols in a message can range from 3 (minimum of R + 1) to $(2^M - 1)$.
K	The number of information symbols per message (N – R).
R	The number of check symbols in a message of N symbols can range from 4 to (N – 1) with a maximum of 40
T	The number of correctable errors per message (floor(R/2)).
M	The number of bits per symbol can range from 4 to 8.
FIELD	The polynomial defining the Galois field for the Reed-Solomon code. The selection of a valid field polynomial is rather complex. Valid field polynomials can be found by using the **FIELD.EXE** utility supplied with the Hammer Cores Reed-Solomon Codec Design Kit.
GENSTART	The first root of the generator polynomial.

Block Diagram

Figure 5 shows the block diagram for the Reed-Solomon decoder megafunction.

Figure 5. Reed-Solomon Decoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50	-1	2,296	2	102 Mbps	Discrete mode: N = 204, R = 16, M = 8, FIELD = 285, GENSTART = 0 (DVB)
		2,720	5	223 Mbps	Streaming mode: N = 204, R = 16, M = 8, FIELD = 285, GENSTART = 0 (DVB)
		1,628	2	119 Mbps	Discrete mode: N = 255, R = 10, M = 8, FIELD = 391, GENSTART = 0 (IntelSat)
EPF10K30A	-1	1,942	5	291 Mbps	Streaming mode: N = 255, R = 10, M = 8, FIELD = 391, GENSTART = 0 (IntelSat)

Reed-Solomon Decoder

Vendor: Integrated Silicon Systems
Target Application: Digital video and audio broadcast, digital satellite broadcast, data storage and retrieval systems
Additional Deliverables: Simulation file, constraint file, user guide
ID Code: C38B-E479

- Configurable solution for high data rate Reed-Solomon decoding
- Supports a range of standards, including European Telecommunication Standards (ETS) 300-421 and ETS 300-429
- Single implementation supports any valid block length
- Processes both burst and continuous data
- Supports high-speed applications (up to 400 Mbps)
- Symbol wide input and output, clock by single symbol rate clock (higher rate clock, if available, can be used to reduce gate count)
- Simple function interface allows easy integration into larger systems

General Description

The ISS Reed-Solomon decoder megafunction provides compact, high-performance solutions for a wide range of applications, and is consistent with the requirements of the European digital video broadcast (DVB) standards.

The European DVB standards provide system requirements for the broadcast of MPEG2 transport packets via, for example, cable or satellite channels. Reed-Solomon error correction coding techniques are employed on the 188-byte MTS packets, with the capability to correct 8 errors per transport packet being required. This process requires 16 parity symbols per MTS packet resulting in a shortened Reed-Solomon codeword of N = 204, K= 188.

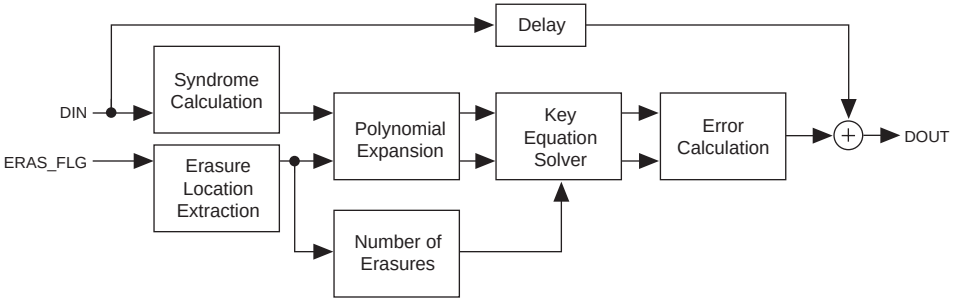
ISS has developed a range of Reed-Solomon decoder megafunctions, capable of operation up to 100 Mbps in Altera CPLDs. This Reed-Solomon decoder megafunction is designed specifically for the requirements of DVB standards.

The megafunction assumes only the availability of a symbol rate clock and all operations in the decoder are timed with this clock. If a higher rate clock, for example a bit rate clock, is available, the clock can be used to reduce the gate count of the decoder.

Block Diagram

Figure 6 shows the block diagram for the Reed-Solomon decoder megafunction.

Figure 6. Reed-Solomon Decoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	1,605	6	320 Mbps	N = 204, K = 188, 8-bit symbols

Reed-Solomon Encoder

Vendor: Hammer Cores
Target Application: Data communication, digital video broadcast
Additional Deliverables: ENCRS automatically generates test vectors based on parameters
ID Code: C4D5-FEC5

- High speed (typically 500 Mbps)
- Fully user parameterized
- Supports multiple telecommunication standards

General Description

The Reed-Solomon encoder megafunction is a compact, high-performance core that can be completely parameterized by the user. The encoder generates systematic codewords, and uses the generator polynomial shown below.

$$g(x) = \prod_{i = \mathrm{GENSTART}}^{\mathrm{GENSTART} + R - 1} (x - \alpha^{i})$$

The roots of the generator polynomial are the elements of the Galois field described by the field polynomial at location *i*. The first root is defined by the GENSTART parameter. The check symbols are generated by dividing the information stream by the generator polynomial. The remainder of this operation is a polynomial containing the check symbols.

Codewords are generated with no latency at the symbol clock rate. The interface to the encoder is very simple, with only four input and output signals required. Utilities are provided to generate the core description, as well as test vectors based on the parameter list.

The Reed-Solomon encoder is optimized for Altera FLEX 6000 and FLEX 10K devices.

Modifiable Parameters

The following megafunction parameters can be modified:

Modifiable Parameters (Part 1 of 2)

Parameter	Description
N	The total number of symbols in a message can range from 3 (minimum of R + 1) to 2^M – 1.
K	The number of information symbols per message is (N – R).
R	The number of check symbols in a message of N symbols, can range from 4 to (N – 1), with a maximum of 40.
T	The number of correctable errors per message (floor(R/2)).
M	The number of bits per symbol can range from 4 to 8.

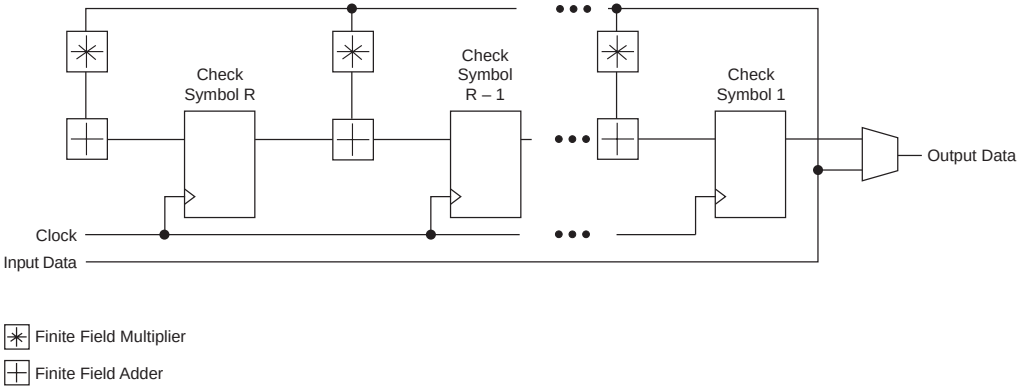
Modifiable Parameters (Part 2 of 2)

Parameter	Description
FIELD	The polynomial defining the Galois field for the Reed-Solomon code. The selection of a valid field polynomial is rather complex. The field polynomial may be defined by a standard for the system being implemented. Valid field polynomials can be found by using the **FIELD.EXE** utility supplied with the Hammer Cores Reed-Solomon Codec Design Kit.
GENSTART	The first root of the generator polynomial.

Block Diagram

Figure 7 shows the block diagram for the Reed-Solomon encoder megafunction.

Figure 7. Reed-Solomon Encoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10A	-1	256	0	512 Mbps	N = 204, R = 16, M = 8, FIELD = 285, GENSTART = 0 (DVB)
		201	0	560 Mbps	N = 255, R = 10, M = 8, FIELD = 391, GENSTART = 0 (DVB)

Reed-Solomon Encoder

Vendor: Integrated Silicon Systems
Target Application: Digital video and audio broadcast, digital satellite broadcast, data storage and retrieval systems
Additional Deliverables: Simulation file, constraint file, user guide
ID Code: C38B-E479

- Configurable solution for high data rate Reed-Solomon encoding
- Supports a range of standards, including European Telecommunication Standards ETS 300-421 and ETS 300-429.
- Single implementation supports any valid block length
- Processes both burst and continuous data
- Supports high-speed applications (up to 400 Mbps)
- Symbol wide input and output, clocked by single symbol rate clock (higher rate clocks, if available, can be used to reduce gate count)
- Low latency implementation: 2 symbol clock cycles
- Simple core interface allows easy integration into larger systems

General Description

The ISS Reed-Solomon encoder megafunction provides compact, high-performance solutions for a wide range of applications.

The European DVB standards provide system requirements for the broadcast of MPEG2 transport packets via, for example, cable or satellite channels. Reed-Solomon error correction coding techniques are employed on the 188-byte MTS packets, with the capability to correct 8 errors per transport packet. This requires the use of 16 parity symbols per MTS packet, resulting in a shortened Reed-Solomon codeword of N = 204, K= 188.

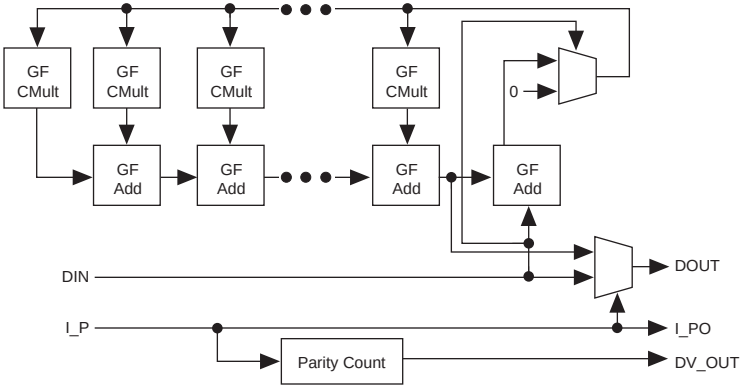
ISS offers a range of Reed-Solomon encoder megafunctions, capable of operating up to 400 Mbps on Altera CPLDs. This megafunction is aimed specifically at the requirements of the DVB standards.

The Reed-Solomon encoder megafunction assumes only the availability of a symbol rate clock and all operations in the encoder are timed with this clock. If a higher rate clock, for example a bit rate clock, is available, the clock can be used to reduce the gate count of the encoder.

Block Diagram

Figure 8 shows the block diagram for the Reed-Solomon encoder megafunction.

Figure 8. Reed-Solomon Encoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	199	0	88 MHz	N = 204, K = 188, 8-bit symbols

Viterbi Decoder

Vendor: CAST
Target Application:
Forward error correction, wireless telecommunications, consumer electronics
Additional Deliverables:
VHDL test bench
ID Code: 2AA5-C014

- Hard decision decoder
- Trace-back method for survivor memory
- Branch metric computations can be added for different applications

General Description

The Viterbi decoder megafunction decodes convolutional codes. The megafunction can also be used to produce the best estimate of a transmitted sequence over a channel with inter-symbol interference (ISI).

The megafunction finds the most likely path of the incoming data. The path is calculated so that the data is compared to the data in the branch metric table (this table shows the allowed data symbols, which are dependent on the encoder), and the error between received symbol and the symbol in table is calculated. The path with the smallest error is selected.

Viterbi_AcsUnit Module

The Viterbi_AcsUnit module calculates the path metrics to find the minimum path. The number of add-compare-select (ACS) units is parameterizable.

Viterbi_SmuCtrl Module

The Viterbi_SmuCtrl module manages the survivor memory. The state machine controls the alternate reading of new branch metrics and the trace-back. During trace-back, the megafunction reads the decision values from memory and outputs the decoded bits. The megafunction reconstructs the encoder's actions in reverse order by updating the state register with a decision value pointed by the former state value. As a result, the decoded bits are also output in reverse order.

Viterbi_Memory Module

The Viterbi_Memory module is an optional RAM memory that stores the trace-back values during calculation.

Modifiable Parameters

The following megafunction parameters can be modified:

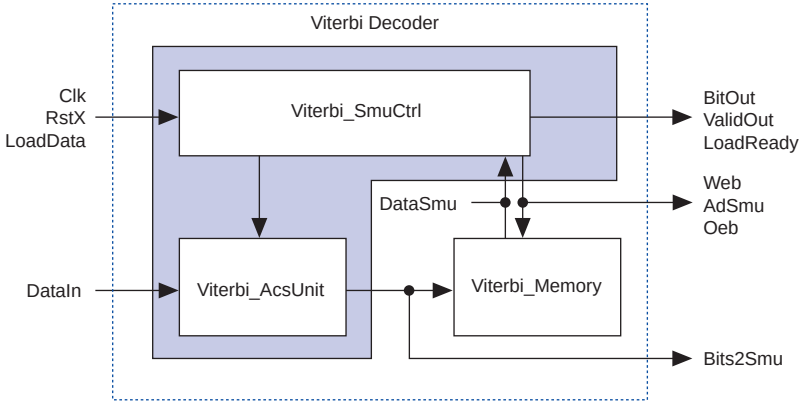
Modifiable Parameters

Parameter	Description
N	Number of states in the trellis
NB	Number of bits to represent transition values
ACS	ACS cells
LTB	Length of the trace-back
LRB	Length of the received burst
IP	Initial path metric for state 0
MWL	Survivor memory (RAM) word length

Block Diagram

Figure 9 shows a block diagram of the Viterbi decoder megafunction.

Figure 9. Viterbi Decoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	960	0	31 MHz	N = 16, NB = 8, ACS = 4, LTB = 30, LRB = 5, IP = –4, MWL = 8
EPF6016	-2	954	–	17 MHz	

Viterbi Decoder

Vendor: Integrated Silicon Systems
Target Application: Digital video broadcast, digital satellite broadcast, data storage and retrieval systems
Additional Deliverables: Behavioral VHDL testbench, complete RTL document
ID Code: C38B-DC41

- Soft decision decoder
- High-speed applications, typically 45 millions of samples per second (MSPS) on continuous data stream
- Optimized for the Altera FLEX 10K architecture
- Compatible with other ISS FEC megafunctions
- Supports a range of standards, including European Telecommunications Standard (ETS) 300-421 for DVB transmission over satellite channels
- Dynamic support of R = 1/2 and R = 3/4
- May be configured in terms of constraint length K, rate R, soft or hard decision
- Simple interface allows easy integration into larger systems

General Description

The ISS Viterbi decoder megafunction is a high-performance implementation suitable for a range of forward error correction (FEC) applications. The megafunction may be used in conjunction with other FEC-related megafunctions available from ISS to rapidly construct complete FEC solutions.

The megafunction has been developed in HDL and have been tailored specifically for Altera FLEX architectures to obtain compact, high-performance implementations.

The basic megafunction assumes only the provision of a symbol rate clock. If a higher rate clock is available in the system, some of the hardware may be reused multiple times per data symbol period, reducing the overall hardware requirements. If the latency of the first sample is approximately 960 `Clk` × 4 cycles, a continuous data stream could be processed at 47 MSPS typically.

The ISS Viterbi decoder megafunction can be rapidly configured for a wide range of specifications. The megafunctions have been developed using HDLs, in a modular and parameterizable fashion. This design gives ISS the capability to quickly configure a specific implementation to a user's specification by adding specific modules, such as the interleaver/deinterleaver and scrambler/descrambler.

Modifiable Parameters

The following megafunction parameters can be modified:

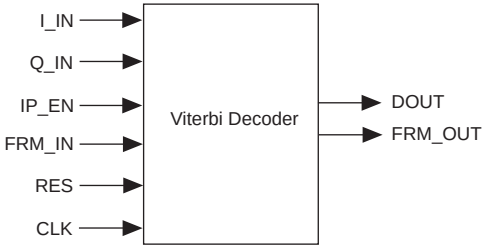
Modifiable Parameters

Parameter	Description
K	Constraint length
R	Decoder rate
P	Puncturing scheme
D	Soft or hard decision decoder

Block Diagram

Figure 10 shows a block diagram of the Viterbi decoder megafunction.

Figure 10. Viterbi Decoder Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	2,633	10	47 MSPS	K = 7, R = 1/2, soft decision decoder

Biorthogonal Wavelet Filter

Vendor: FASTMAN
Target Application: Fingerprint compression, advanced image compression
Additional Deliverables: Simulation file
ID Code: C3D0-AAA1

- Low-pass/high-pass filter integration
- Pipelined design
- Parallel vector multipliers
- Very fast implementation
- Biorthogonal symmetric filters

General Description

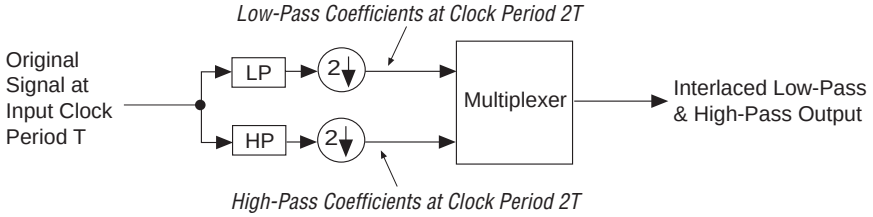
The biorthogonal wavelet filter megafunction operates on an incoming data stream and produces an output stream that consists of alternating low-pass and high-pass filtered outputs, each decimated by a factor of two from the input. The megafunction has a simple interface consisting of data input and output registers and a single global clock, and it employs fast pipelined parallel vector multipliers. The internal clock runs at one-half of the input data clock speed.

The megafunction is symmetrical, which makes it ideal for image processing applications. Other types of wavelet filter megafunctions are available through FASTMAN's custom design program.

Block Diagram

Figure 11 shows the block diagram for the biorthogonal wavelet filter megafunction.

Figure 11. Biorthogonal Wavelet Filter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K40	-4	1,776	0	68 MHz	16-bit data size, 12-bit coefficient precision

Cascadable Adaptive FIR Filter

Vendor: Integrated Silicon Systems
Target Application: 1-D and 2-D adaptive filtering, image and video processing, pulse shaping correlation and equalization
Additional Deliverables: Behavioral VHDL testbench, complete RTL documentation
ID Code: C38B-1126

- Ultra-fast "on-the-fly" coefficient programmability
- High-level specification up to 75 MSPS
- Optimized for the Altera FLEX architecture
- One-dimensional (1-D) and two-dimensional (2-D) versions available

General Description

The 7-tap, 9-bit data and coefficient finite impulse response (FIR) megafunction with "on-the-fly" coefficient programmability performs the following operation:

$$\texttt{Result[19..0]}_n = \sum_{K=1}^{7} \texttt{DataIn[8.0]}_{(n-K)} \times \texttt{W}_{(K)}\texttt{In[8.0]}$$

The variable $\texttt{DataIn[8..0]}_n$ refers to the nth input sample. The variable $\texttt{W}_{(K)}\texttt{In[8..0]}$ refers to the Kth coefficient of the FIR filter.

Data Input Interface

The 9- bit input data word, `DataIn[8..0]`, can be represented by either two's complement or straight binary format. The input data format is defined by the `Sel` signal. When the `Sel` signal is tied to logic 0 during the operation of the 7-tap FIR filter, the data is assumed to be in two's complement format. When the `Sel` signal is tied to logic 1, the data is assumed to be in straight binary format. The data is latched into the filter on the falling edge of the `ClkInput` signal.

Coefficient Loading

The coefficients are in sign plus absolute value representation and are latched into the filter on the falling edge of the `Clk_Load` signal when the `En_Load` signal is asserted high.

Tapped Delay Outputs

The data-tap outputs, `D1Out[8..0]` to `D7Out[8..0]`, are in two's complement format, regardless of the format used by `DataIn[8..0]`. The data-tap outputs are clocked out on the falling edge of the `ClkInput`.

Cascade Data Output

The input data delayed output, `DataOut[8..0]`, is in the same representation as the input data. The input data delayed output is clocked out on the falling edge of the `ClkInput` signal.

Result Output

The two's complement result, `Result[19..0]`, from the filter is clocked out on the falling edge of the `ClkInput` signal.

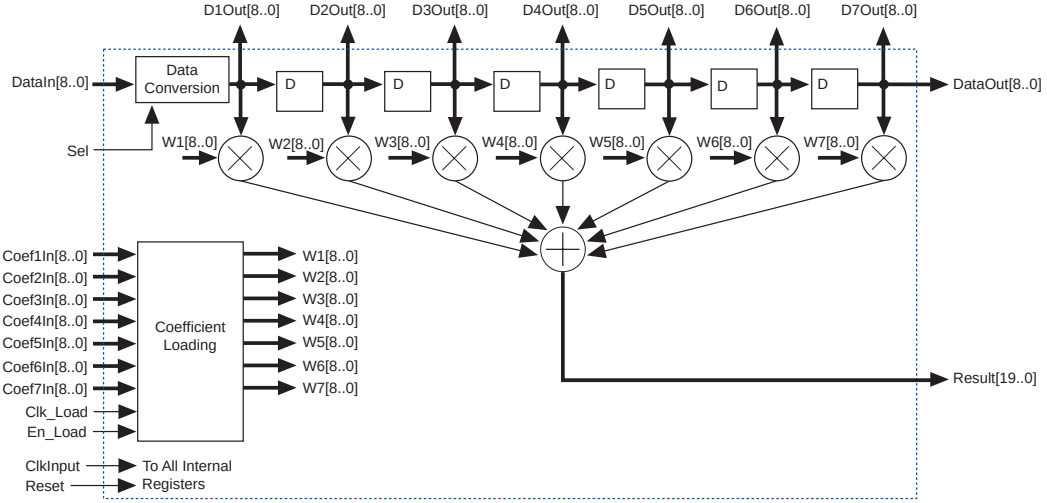
Latency

From the perspective of data entering the megafunction (`DataIn[8..0]`) the latency of the 7 tap FIR filter function is 11 `ClkInput` cycles. `D1Out[8..0]` has a latency of 3 `ClkInput` cycles, `D4Out[8..0]` has a latency of 4 `ClkInput` cycles, `D7Out[8..0]` has a latency of 9 `ClkInput` cycles, and `DataOut[8..0]` has a latency of 9 `ClkInput` cycles.

Block Diagram

Figure 12 shows the block diagram for the cascadable adaptive FIR filter megafunction.

Figure 12. Cascadable Adaptive FIR Filter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance *Note (1)*	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	2,070	0	75 MSPS	T = 7, W = 9, P = 0

Note:
(1) Contact ISS for design optimization and highest performance results.

Decimating Filter

Vendor: FASTMAN
Target Application:
MPEG audio, band-pass filtering
Additional Deliverables:
Simulation file
ID Code: C3D0-77A7

- Uses parallel vector multipliers
- Pipelined design
- Symmetrical or asymmetrical
- Even or odd number of taps
- Fast parallel implementation
- Customizable number of taps, data word size, and internal precision

General Description

The decimating filter megafunction implements biorthogonal wavelet filters for signal processing or compression. The megafunction operates on an incoming data stream, and it produces a filtered output stream that is decimated by a factor of two.

The designer can select the number of taps, the data word size, and the internal precision for the megafunction. In addition, the designer can select any set of filter coefficients and input them into the design through a data file. The megafunction can implement a filter with an even or odd number of taps in a symmetrical or asymmetrical manner. When the number of taps is odd, the filter is symmetrical to the center tap. The filter employs pipelined parallel vector multipliers. The internal clock of the filter runs at the output clock speed (i.e., one half of the input clock speed).

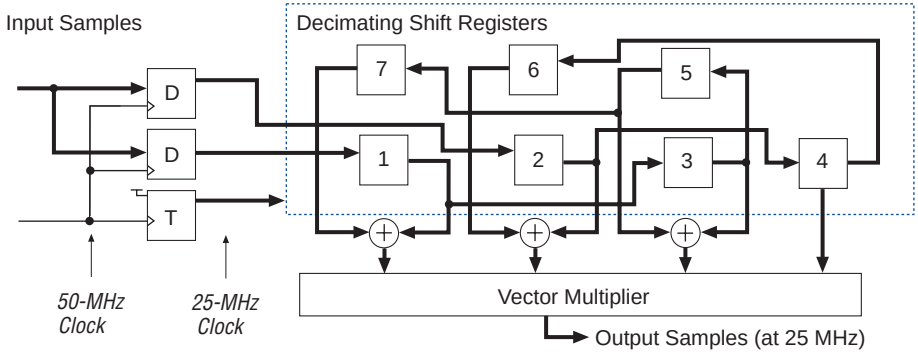
Modifiable Parameters

FASTMAN can customize a wide variety of filters (including non-decimating filters) to meet user specifications.

Block Diagram

Figure 13 shows the block diagram for the decimating filter megafunction.

Figure 13. Decimating Filter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K20	-3	1,040	0	65 MHz	9-tap filter, 16-bit data word size
		921	0	62.5 MHz	5-tap filter, 16-bit data word size
EPF8820A	-3	185	–	77.5 MHz	8-tap filter, 8-bit data word size
EPF81500A	-3	920	–	55 MHz	5-tap filter, 16-bit data word size

IIR Filter Library

Vendor: Integrated Silicon Systems
Target Application: Digital audio processing, digital video processing, signal conditioning, channel selection filtering
Additional Deliverables: User guide
ID Code: C38B-704E

- Cascadable
- High performance
- "On-the-fly" coefficient adaptation available

General Description

The megafunctions in the infinite impulse response (IIR) filter library are used in a broad spectrum of signal bandwidths. The megafunctions are basic building blocks for many IIR filter implementations. A second-order IIR filter, such as a biquad IIR filter, can be used to construct higher orders of filters by cascading the required number of biquad sections. A complete range of high-performance IIR filters can be constructed from a single IIR filter megafunction, which is covered under the same IIR filter library license. The megafunctions can process data at rates in excess of 50 MSPS.

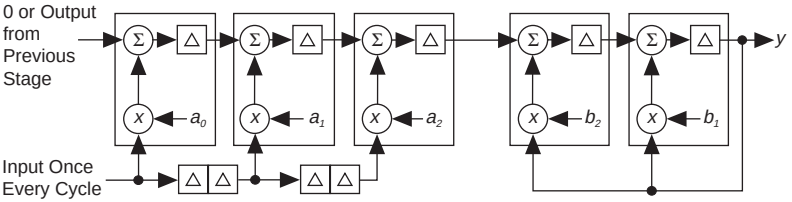
Modifiable Parameters

ISS can customize the data sample rate, coefficient loading strategy, filter order, and data word lengths and formats. Contact ISS for the best parameter settings to meet specific application requirements. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Block Diagram

Figure 14 shows the block diagram for the IIR filter library.

Figure 14. IIR Filter Library Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K20	-3	430	6	17 MHz	Biquad IIR filter with 8-bit input data, 8-bit coefficients, and 11-bit internal accuracy

LMS & Zero-Forcing Equalizers

Vendor: Hammer Cores
Target Application:
Data communication, image compression
Additional Deliverables:
MATLAB utility (linvec, lintst), reference design quadrature phase shift keying (QPSK) slicer/quantizer
ID Code: C4D5-E015

- Fully user parameterized equalizers
- LMS or zero forcing algorithms
- High performance—100 MSPS

General Description

The least-mean square (LMS) and zero-forcing equalizer megafunctions are fully parameterized, high-performance functions that are optimized for Altera devices. All parameters are fully user-definable. These megafunctions can achieve sample rates of 100 MSPS. Coefficients are updated at a rate up to the sample rate (selectable by the user), and may be initialized to any value, at any time.

High-performance levels are achieved through pipelining. Any level of pipelining can be specified, including no pipelining, which results in a standard LMS or zero-forcing equalizer. All algorithmic modifications and the architectural design are automatically handled by the megafunction. Any number of taps can be specified. Almost all precisions, internal and external to the equalizer, can be defined. An equalizer can optionally contain both LMS and zero-forcing algorithms, which is switched by an external control input.

The megafunction builds one real rail of the equalizer per instance. A complex equalizer can be constructed out of four rails. Because memory is not required, these equalizers can be targeted for both FLEX 10K and FLEX 6000 devices. A performance/size trade off parameter is given to meet the system design objectives.

Modifiable Parameters

The following megafunctions parameters can be modified:

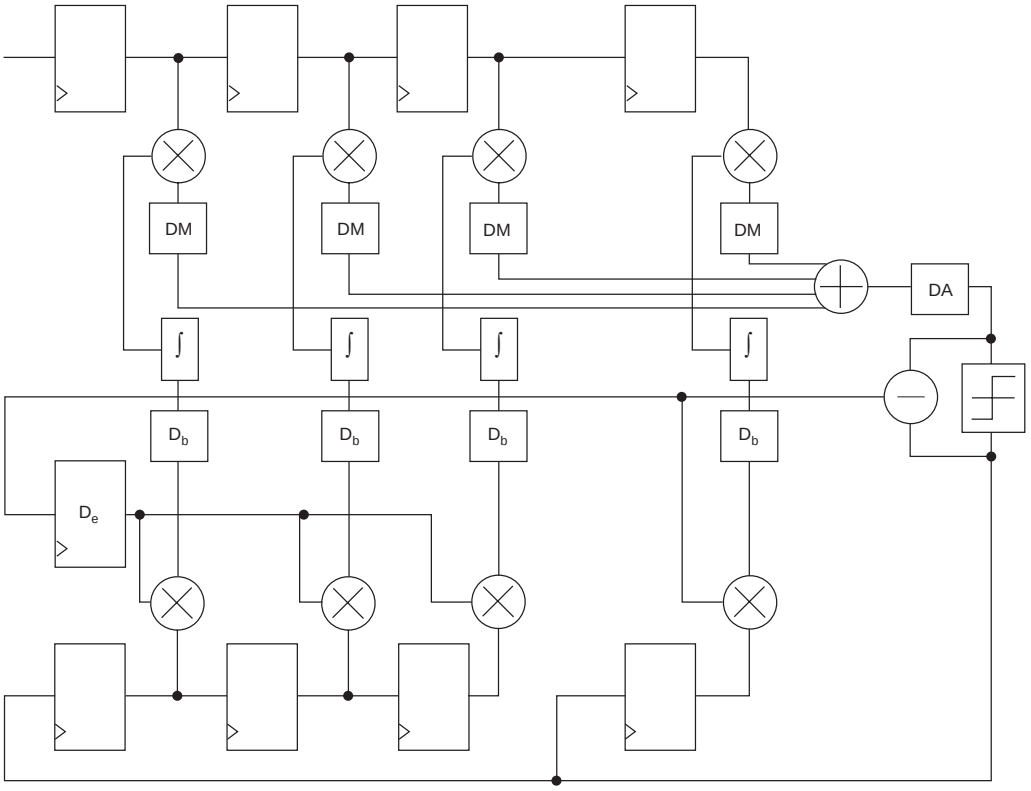
Modifiable Parameters

Parameter	Description
TAPS	Number of feedforward taps
CENTER	A: Adaptive center tap; F: Fixed at unity; Z: Zero
TYPE	LMS: LMS algorithm; ZP: Zero-forcing algorithm; BOTH: Both LMS and zero-forcing algorithms
SHARE	Number of taps per multiplier (size/speed trade off)
SIGIN	Sample input precision
COEFF	Feedforward weight precision
PREC	Feedforward multiplier output precision
ERRW	Error between estimate and nearest symbol
SIGCOR	Correlation precision: LMS
SYMCOR	Correlation precision: ZF
WIDTHO	Output of system (precision of estimate)
CONV	Inverse of convergence constant
DELAY	Latency of external error calculation, e.g., quadrature amplitude modulation (QAM) slicer
RELAX	Sum relaxation of weight update
PIPELINE	Latency of feedforward section
BACKPIPE	Latency of feedback section

Block Diagram

Figure 15 shows the block diagram for the megafunctions.

Figure 15. LMS & Zero-Forcing Equalizer Megafunctions Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	2,019	0	104 MHz	TAPS = 9, CENTER = F, TYPE = LMS, SIGIN = 10, COEFF = 8, PREC = 12, ERRW = 3, SIGCOR = 3, WIDTHO = 12, CONV = 6, PIPELINE = MAX

QPSK Equalizer

Vendor: Integrated Silicon Systems
Target Application: Satellite communications
Additional Deliverables: VHDL testbench, Matlab files
ID Code: C38B-1123

- Fast speed 61 MHz
- Easy to use
- Parameterizable

General Description

The QPSK equalizer megafunction is composed of two channels (I and Q), with one channel per device. Each channel has been implemented as a 7-tap FIR filter, where the coefficients are updated using the LMS algorithm. All operations perform at the symbol rate, except the coefficient update, which is performed every 12 clock cycles.

All the input and output words for the 7-tap LMS FIR filter megafunction are bit-parallel and all the signals are active high.

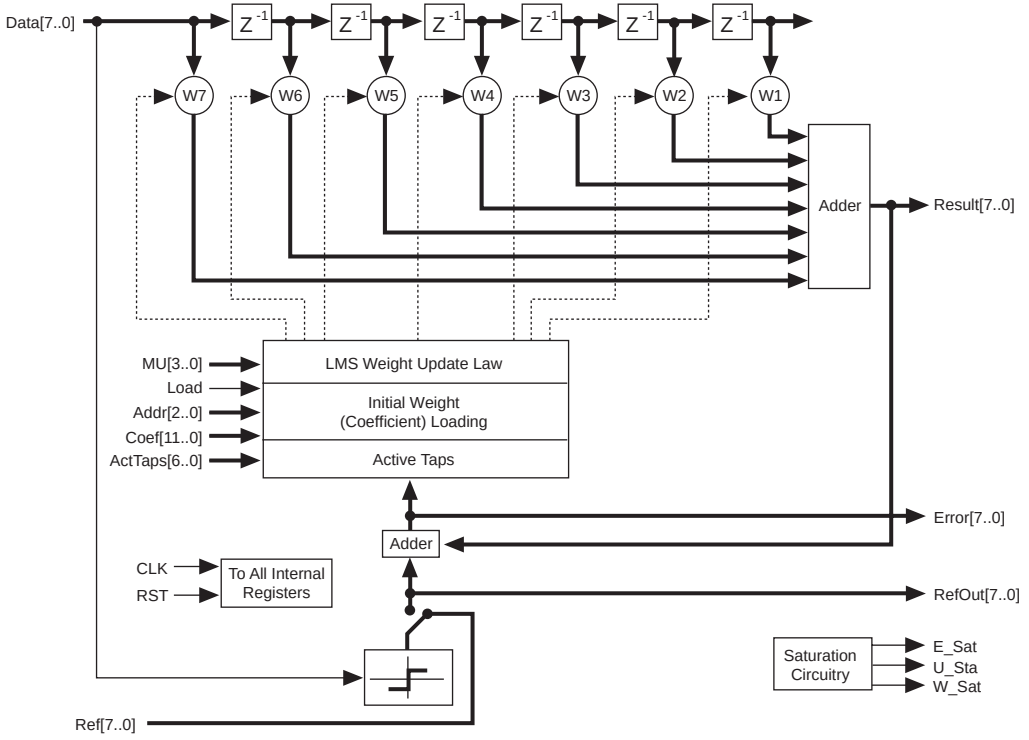
The update operation is based on the LMS algorithm shown below:

$$W_{k+1} = W_k + \mu e_k x_k$$

Block Diagram

Figure 16 shows the block diagram for one 7-tap LMS filter megafunction.

Figure 16. QPSK Equalizer Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	2,500	0	61 MHz	Contact ISS

Rank Order Filter

Vendor: Integrated Silicon Systems
Target Application: Signal processing systems
Additional Deliverables: Simulation files, testbench
ID Code: C38B-1115

- User-defined filter length
- Two-dimensional (2-D) operation available (e.g., 1 × 3, 3 × 3)
- 12-bit two's complement data word length
- 20 MSPS operation

General Description

The rank order filter megafunction enables any rank from a user-defined input data sequence to be selected. Designers can choose both 1-D and 2-D data windows and the length of the window.

Data Configuration Registers

Data is clocked to the function on the rising edge of the clock signal, `clk`. For 1-D operation, only the `data1` input is used, and the `data2` and `data3` inputs are tied low by the user. For 2-D operation, all three data inputs are used.

A range of further configurations are possible, including 1-D filters from 3 to 15 bits, as well as 1 × 3, 3 × 3 2-D filters. The `length` and `D1_D2` inputs configures the filter. The `length` input determines the data length, and it is used with the `D1_D2` input to configure the filter for 2-D operation. The data configuration register block formats the input data for sorting by the next stage in the filter, the shuffle array.

Shuffle Array

The shuffle array processes the data elements of each "window" in parallel. When the data emerges from the shuffle network, it is fully sorted.

Rank Selection

The desired rank value output is selected by input rank under user control.

Latency

A new data sample, or samples in 2-D operation, is loaded into the megafunction on every clock cycle. After the filter is completely filled with data, a result is produced every clock cycle.

The latency in clock cycles from a data series being loaded into the filter to getting the result is 12 clock cycles (i.e., as a new data sample is loaded into the filter, the first result is output 12 clock cycles later). Because the megafunction operates as a sliding window, each data sample contributes to several consecutive results (e.g., 15 results for a 15 × 1 filter). The filter was designed so the latency for all modes of operation are equivalent. A delay is also associated with the loading of the first set of data series (e.g., 15 clock cycles for a 15 × 1 filter).

Modifiable Parameters

The following megafunction parameters can be modified:

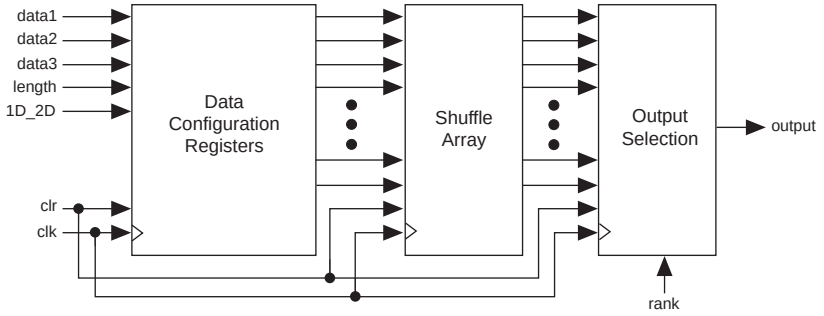
Modifiable Parameters

Parameter	Description
W	Window size
L	Data word length (bits)

Block Diagram

Figure 17 shows the block diagram for the rank order filter megafunction.

Figure 17. Rank Order Filter Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100A	-1	3,852	0	30 MHz	W = 15 × 1, L = 12

Complex Multiplier/Mixer

Vendor: Nova Engineering
Target Application: Digital mixers, modulators/demodulators, discrete Fourier transforms (DFT), complex arithmetic, wireless communications systems
Additional Deliverables: Prototype board, simulation files
ID Code: 66A3-101

- Multiplies/mixes two complex numbers/signals
- Fully synchronous design
- Parameterized data width
- Parallel implementation for maximum speed

General Description

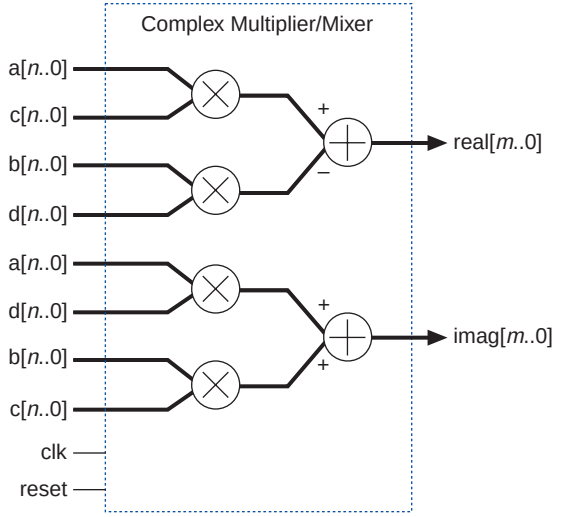
The complex multiplier/mixer megafunction multiplies two complex numbers or mixes two complex signals. It has a parallel, pipelined architecture that maximizes speed. The megafunction's internal and external operations are synchronized to the rising clock edge, and an asynchronous reset input is provided for initializing all internal registers.

The megafunction can be used for vector cross products, vector dot products, up/down frequency conversion, differential phase detection, digital amplitude modulation (AM), QAM, and DFT. The megafunction does not require FLEX 10K EABs; therefore, it can be combined with sine/cosine look-up tables (LUTs) for frequency down conversion or DFT functions within a single device.

Block Diagram

Figure 18 shows the block diagram for the complex multiplier/mixer megafunction.

Figure 18. Complex Multiplier/Mixer Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	604	0	83 MHz	8 × 8 complex multiplier with a three-clock latency
EPF6016	-1	608	–	47 MHz	

Cordpol Cordic Function

Vendor: Hammer Cores
Target Application:
Scientific computation
Additional Deliverables:
User guide
ID Code: C4D5-COD0

- High speed (50-MHz operation)
- User parameterized

General Description

The Cordpol Cordic megafunction uses the Cordic algorithm to convert rectangular coordinates to polar coordinates. This algorithm is also known as the backward-rotation Cordic algorithm. The Cordic algorithm is an iterative process, which is often more efficient to implement in hardware than calculating the hypotenuse and angle using multiplies, divides, and square roots.

The accuracy of the Cordic algorithm can be quite good, depending on the precision of the inputs. The number of iterations is the same as the precision of the input.

The Cordpol Cordic megafunction is a parallel implementation of the Cordic algorithm, and can be purely combinatorial or pipelined at every iteration.

The Cordpol Cordic megafunction accepts two unsigned numbers, giving the (*x*,*y*) coordinates of the vector endpoint. If the point's location is not in the first quadrant, the absolute values of the endpoint must be input. This operation will not affect the magnitude output, because the length of the vector is always a positive number.

Modifiable Parameters

The following megafunction parameters can be modified:

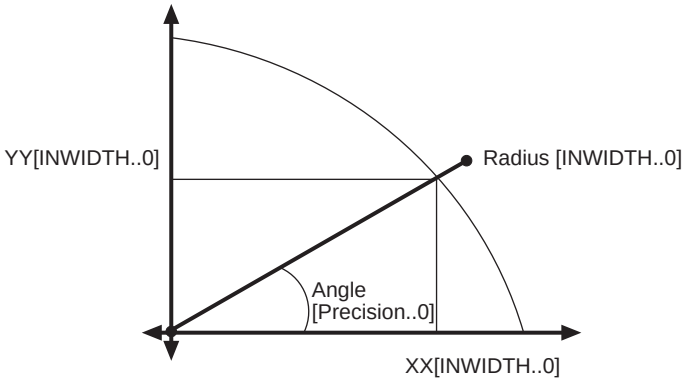
Modifiable Parameters

Parameter	Description
`INWIDTH`	Precision of the input Cartesian coordinates (*x*, *y*). The valid range is from 6 to 24.
`PIPELINED`	When yes, `INWIDTH` pipeline stages are generated.

Block Diagram

Figure 19 shows the block diagram for the Cordpol Cordic megafunction.

Figure 19. Cordpol Cordic Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	528	0	61 MHz	INWIDTH = 10, PIPELINED = NO

Floating-Point Operator Library

Vendor: Integrated Silicon Systems
Target Application: Adaptive systems, safety-critical systems, flight control, flight guidance, scientific processing, overflow indicator
Additional Deliverables: VHDL testbench, OpenCore feature, VHDL RTL source code
ID Code: C38B-1112, C38B-1122, C38B-1121

- Programmable register length and initial value
- Automatic resizing and feedback selection (2 to 32 bits)
- Feedback architecture designed for maximum speed
- Multiple user-selectable configurations

General Description

Floating-point operation implementation in programmable logic is now easy with the ISS floating-point operator library, which consists of the following:

- *Floating-point adder*—Registrable output and optional pipeline cuts, both addends have the same exponent size.
- *Floating-point divider*—Using radix-2 SR 0 array. Default quotient value when in operation = 0/0.
- *Floating-point multiplier*—BooWtMult is used to achieve the fastest possible speed without introducing pipelining in mantissa processing.

Modifiable Parameters

The following megafunction parameters can be modified:

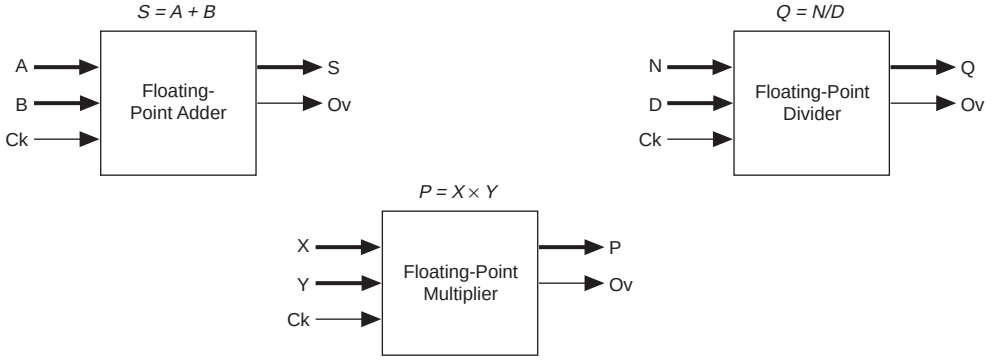
Parameter	Description
M	Mantissa size
E	Exponent size
P	Number of pipeline levels

Contact ISS directly for any required modifications.

Block Diagram

Figure 20 shows the block diagram for the floating-point operator library.

Figure 20. Floating-Point Operator Library Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K30A	-1	618	0	35 MHz	Floating-point adder (M = 16, E = 6, P = 3)
		785	0	37 MHz	Floating-point multiplier (M = 16, E = 6, P = 2)
		2,051	0	41 MHz	Floating-point divider (M = 16, E = 6, P = 6)

Linear Feedback Shift Register

Vendor: Nova Engineering
Target Application: Direct sequence spread spectrum (DSSS), pseudo-random number (PN) generation, built-in self-test (BIST), encryption and decryption, error detection
Additional Deliverables: Prototype board, simulation file
ID Code: 66A3-6101

- Programmable register length and initial value
- Automatic resizing and feedback selection (2 to 32 bits)
- Feedback architecture designed for maximum speed
- Multiple user-selectable configurations

General Description

The linear feedback shift register (LFSR) megafunction is based on linear XOR or XNOR feedback logic in which the initial value of the shift register, shift register taps, and feedback logic determines the output sequence.

The megafunction can be resized to any length between 2 and 32 bits, and the feedback logic automatically adapts to the shift register length to produce a maximum length sequence. The LFSR megafunction is designed to provide feedback delays that are independently reconfigured. This architecture maximizes speed and provides uniform performance for all configurations.

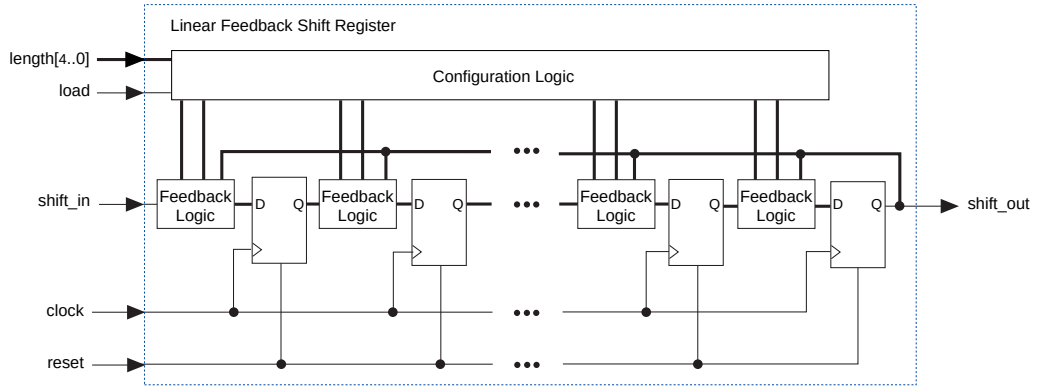
Modifiable Parameters

Nova Engineering will customize the LFSR megafunction's shift register size and the feedback configuration to meet user specifications at no additional cost. This customization reduces logic usage and optimizes area and performance.

Block Diagram

Figure 21 shows the block diagram for the LFSR megafunction.

Figure 21. Linear Feedback Shift Register Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	338	0	103 MHz	Contact Nova Engineering
EPF6016	-2	318	–	95 MHz	Contact Nova Engineering
EPM7128E	-7	103	–	113 MHz	Contact Nova Engineering

Binary Pattern Correlator

Vendor: Nova Engineering
Target Application: Spread spectrum communications, pattern recognition, error correction, frame synchronization
Additional Deliverables: Prototype board, simulation file
ID Code: 66A3-501

- Detects a reference pattern within a data stream
- Programmable threshold register
- Parameterized reference pattern length and width
- Pipelined architecture for maximum speed

General Description

The binary pattern correlator megafunction is designed to search a serial data stream for the presence of a user-programmed reference pattern. The reference pattern is detected when the number of matches between the reference pattern and the input data exceeds the threshold value. Threshold values allow the user to program the acceptable tolerance for a pattern match.

The megafunction uses a parallel and pipelined architecture that provides maximum speed. The megafunction's internal and external operations are synchronized to the rising clock edge, and an asynchronous reset input is provided for initializing all internal registers.

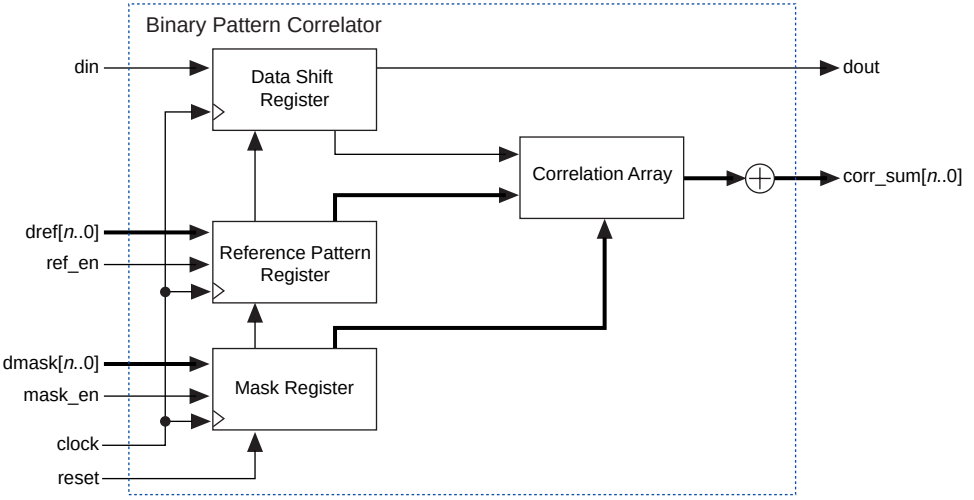
Modifiable Parameters

Nova Engineering will customize the megafunction's reference pattern length and width at no additional cost. Customizing the data widths optimizes the megafunction for specific applications.

Block Diagram

Figure 22 shows the block diagram for the binary pattern correlator megafunction.

Figure 22. Binary Pattern Correlator Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	206	0	68 MHz	Contact Nova Engineering
EPF6016	-2	236	–	32 MHz	Contact Nova Engineering

DES-Core

Vendor: CAST
Target Application:
Secured communications, electronic commerce, wide-area network (WAN) and local-area network (LAN) routers
Additional Deliverables:
VHDL testbench, user guide
ID Code: 2AA5-C019

- Loads the commands, which define the operation of CDESC, from the external host controller through the system data bus into the internal command register
- Loads the 64-bit encoded/decoded data from the host controller through the system data bus into the internal working data register
- Executes the data encoding/decoding in accordance with DES specification
- EBC and CBC modes supported
- Outputs 64-bit encoded/decoded data from the internal working data register onto the system data bus
- Generates 64-bit random numbers and outputs these on the system data bus on host request
- Loads and stores the secret keys in special key memory (internal or external)
- Loads the address of a current secret key into the internal key address register, which controls the key memory
- Transfers the current secret key from the key memory into the working key register
- Generates a session key by DES-processing of generated random number and transfers the calculated key from the working data register into the working key register
- Self tested
- Status register provides information on the current state of the CDESC (e.g., busy, command successfully completed, and self test passes)
- The simple external bus interface allows CDESC to work as a coprocessor with almost any microprocessor/microcontroller, including such devices as i8051, Z-80, Mc6805, i80x86, and others

General Description

The Extended DES Cryptoprocessor (CDESC) is designed for data protection in computers, computer networks, communication hardware, and business computing systems (including bank systems and electronics payments).

Due to export restrictions, this megafunction may not be available to customers located outside the United States and Canada, or to certain foreign nationals located in the United States. Customers should contact CAST directly for further information regarding export restrictions.

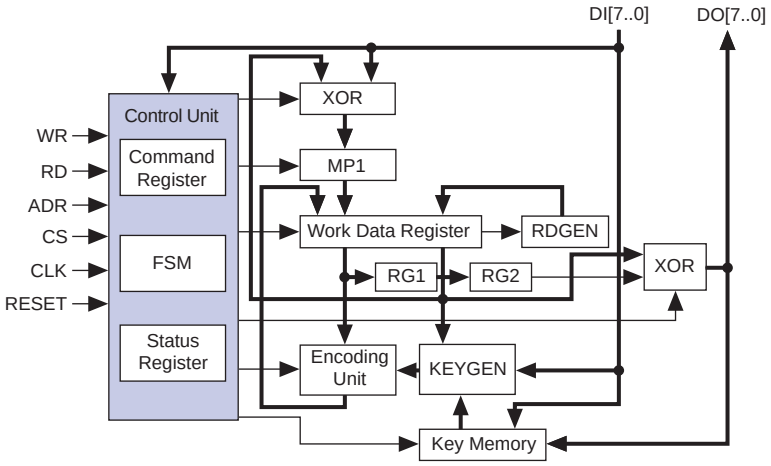
Modifiable Parameters

CAST, Inc. can customize the DES-Core megafunction to include additional DES modes, triple DES, and implementation of key-memory into RAM or ROM.

Block Diagram

Figure 23 shows the block diagram of the DES-Core megafunction.

Figure 23. DES-Core Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K30	-3	1,330	1	15 MHz	Contact CAST
EPF10K30A	-1	1,331	1	24 MHz	Contact CAST

DES-Core

Vendor: SICAN
Target Application:
Secured communications, electronic commerce, WAN/LAN routers
Additional Deliverables:
Documentation
ID Code: 18CD-4A76

- Fast data encryption/decryption using the DES algorithm
- Triple-DES support
- 56-bit or 112-bit key length (using triple-DES)
- 64 Mbits/second encryption speed
- Key change within one clock cycle
- ECB mode

General Description

The SICAN DES-Core megafunction provides high-speed data encryption/decryption using the industry-standard DES algorithm. With its high throughput of 64 Mbits/second, the DES-Core megafunction is a perfect choice for a variety of applications requiring secured communications. It accepts 64-bit parallel data input and processes one DES operation in 16 clock cycles. The output is 64 bits wide.

The DES-Core megafunction can be configured for either encryption or decryption operation and is switchable between normal DES mode and triple DES mode. It accepts a 56-bit key in DES mode or a 112-bit key in triple DES mode.

Due to export restrictions, this megafunction may not be available to customers located outside the United States and Canada, or to certain foreign nationals located in the United States. Customers should contact SICAN directly for further information regarding export restrictions.

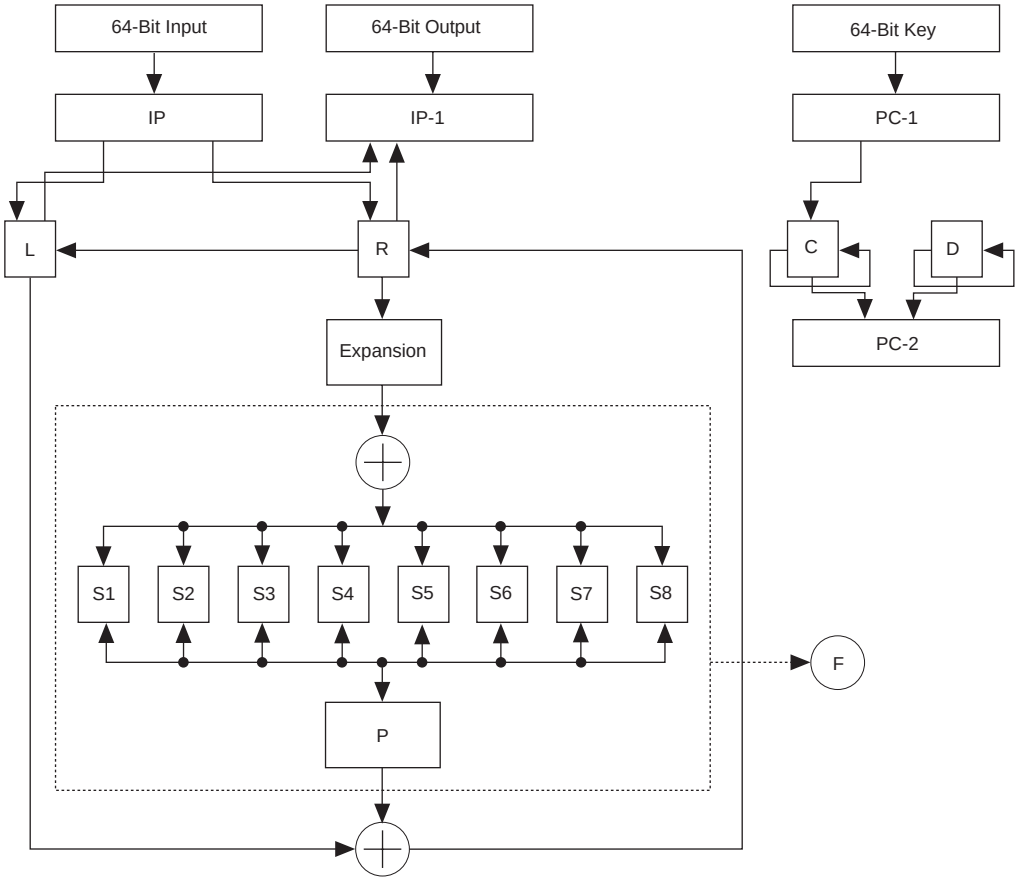
Modifiable Parameters

SICAN can modify the key length (`L`) and mode type (`M`) to meet user requirements.

Block Diagram

Figure 24 shows the block diagram of the DES-Core megafunction.

Figure 24. DES-Core Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Settings
		Logic Cells	EABs		
EPF10K50V	-1	574	0	27 MHz	L = 56 bits

IDR Framer/Deframer

Vendor: Integrated Silicon Systems
Target Application: Satellite communications, DVB
Additional Deliverables: Testbench, simulation files, constraint files
ID Code: C38B-1123

- Frame and multiframe synchronization signals
- Four backward alarm signals
- Single voice channel of 8 Mbits/second
- Two voice channels of 32 Mbits/second
- Compatible IESS-308

General Description

The ISS IDR framer/deframer megafunction performs engineering service circuit (ESC) channel data, voice, and alarm extraction, along with frame synchronization signal detection. The recovered data streams are buffered and then clocked out at different rates. Clock signals for the slower data rate signals are generated. Four clock rate combinations are supported. Both input data rate and composite data rate clocks must be supplied at the exact frequency ratios defined by IESS-308.

Synchronous Detection

The incoming data stream is sampled one bit at a time, over a succession of frames. If no synchronization pattern is detected within 16 frames at that bit position, a bit is skipped and synchronization detection moves on to the next bit position. Once a valid synchronization is detected, frame data extraction begins on the next superframe. The `InSync` signal will be asserted when the initial data appears on the `DataOut` pin. In the absence of transmission bit errors, synchronization will be achieved within a time specified by the following formula.

$$\text{SyncTime} = \texttt{CrClk}\ \text{period} \times 16 \times (\text{TotalBitsPerFrame})^2$$

Data FIFO Buffer

Input data is loaded into an asynchronous FIFO buffer for data rate conversion. No data is loaded when frame overhead bits are being received. Data bits are extracted from the FIFO buffer at the intermediate rate, and output to the `DataOut` pin.

ESC Data Clocks and Buffers

The composite rate clock, `CrClk`, derives the clock signals for the ESC voice channels, ESC data channels, and ESC alarm signals. These signals have defined frequencies. Data for the relevant channel is loaded into small buffers on receipt from the composite stream. Data is removed from the buffers a maximum of two frames later, on the rising edge of the relevant clock signal, and driven onto the appropriate output pin.

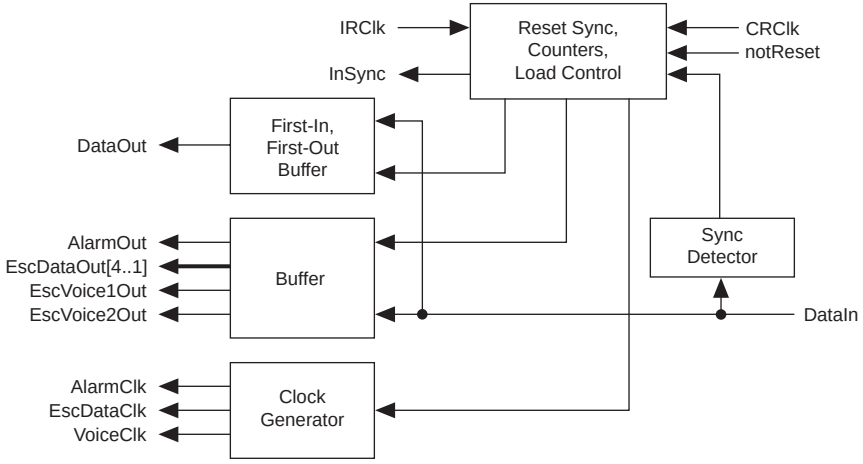
Counters & Buffer Load Control

A number of counters keep track of the frame, subframe, and bit number, and control the input stream disassembly. Note that IESS-308 specifies no relationship between the content of the data streams and the framing signals. The equipment connected to the data streams is responsible for synchronizing to the data carried in those streams.

Block Diagram

Figure 25 shows the block diagram for the IDR framer/deframer megafunction.

Figure 25. IDR Framer/Deframer Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K10A	-1	171	0	60 MHz	Framer
		205	0	83 MHz	Deframer

Digital Modulator

Vendor: Nova Engineering
Target Application: Amplitude modulators, frequency modulators, phase modulators, and up/down frequency conversion
Additional Deliverables: Simulation files
ID Code: 66A3-0301

- Implements a wide variety of modulation formats
- Uses phase-continuous direct digital synthesis (DDS)
- Parameterized input and output data widths for specific applications
- Optimized for the FLEX 10K device architecture

General Description

The digital modulator megafunction combines a quadrature numerically controlled oscillator (NCO) with a complex multiplier/mixer to provide a wide tuning range, excellent frequency resolution, and a fast settling time. The megafunction's parallel and pipelined architecture maximizes speed.

The megafunction generates a wide variety of modulation formats, including: AM, frequency modulation (FM), amplitude shift keying (ASK), frequency shift keying (FSK), continuous phase modulation (CPM), and phase shift keying (PSK).

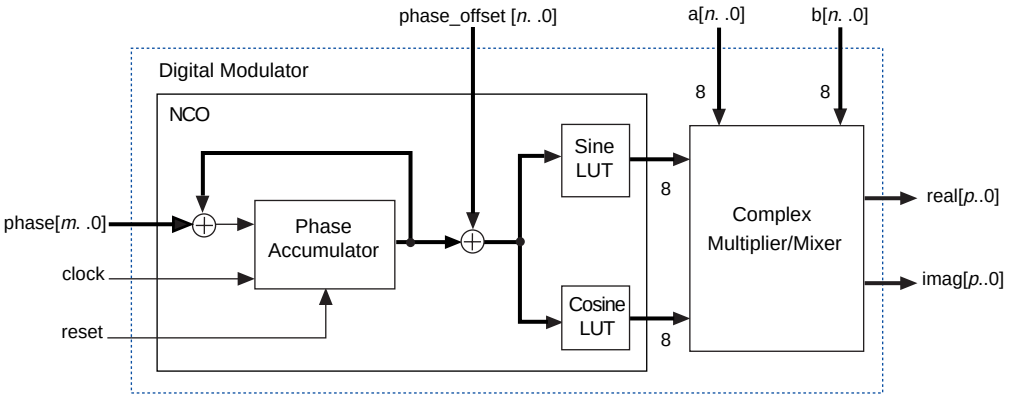
Modifiable Parameters

Nova Engineering will customize the phase accumulator width, multiplier width, phase offset input width, and the output data width at no additional charge.

Block Diagram

Figure 26 shows the block diagram for the digital modulator megafunction.

Figure 26. Digital Modulator Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	674	2	71 MHz	24-bit accumulator, 10-bit phase offset, 8-bit complex multiplier, and 8-bit quadrature outputs

Early/Late-Gate Symbol Synchronizer

Vendor: Nova Engineering
Target Application:
Digital receivers,
synchronous data interfaces
Additional Deliverables:
Simulation files
ID Code: 66A3-601

- Aligns local clock phase to incoming binary data transitions
- Supports a wide range of sample clock rates
- Includes programmable loop filter
- Supports acquisition and tracking modes

General Description

The early/late-gate symbol synchronizer megafunction is a closed-loop binary data synchronizer that performs two separate integrations for each symbol interval. The integrators accumulate the value of the symbol detected at the sample clock rising edge for each half of the symbol period. The difference between the integration is a measure of the local clock timing error. When the first-half symbol integration matches the second-half symbol integration, the local data clock is aligned to the incoming data.

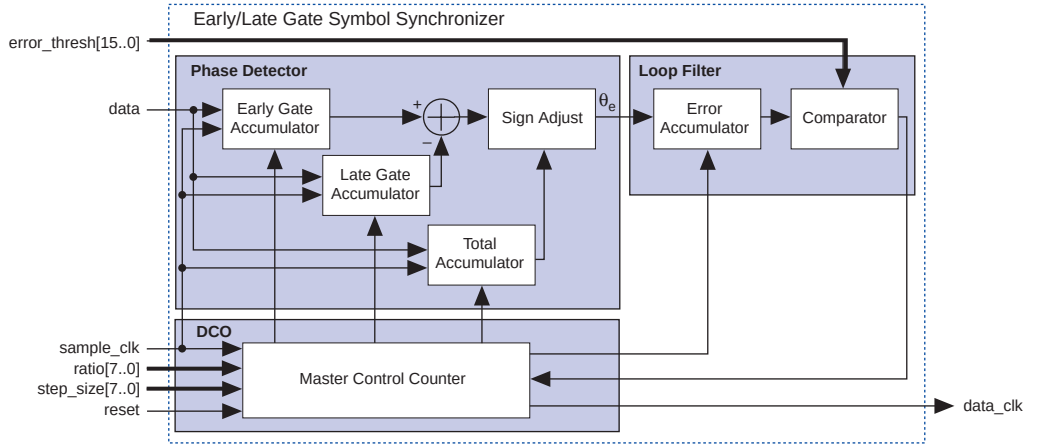
The megafunction includes a filter for controlling the timing loop response. The filter can be programmed to increase the loop bandwidth, which provides a faster transient response during acquisition mode. The loop bandwidth can also be reduced to provide better performance during tracking mode.

A programmable clock divider allows the megafunction to support a wide range of sample clock rates. Increasing the sample clock rate provides finer timing resolution and subsequently, less timing jitter. Decreasing the sample clock rate reduces power consumption, particularly in applications where timing jitter requirements are less stringent.

Block Diagram

Figure 27 shows the block diagram for the early/late-gate symbol synchronizer megafunction.

Figure 27. Early/Late-Gate Symbol Synchronizer Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	260	0	71 MHz	Contact Nova Engineering

FFT/IFFT

Vendor: Integrated Silicon Systems
Target Application: Signal processing systems
Additional Deliverables: VHDL testbench, test vector generation files, functional VHDL simulation model
ID Code: C38B-1114

- Fast speed
- No external memory required
- Easy to use
- Fully parameterizable

General Description

The ISS 64-, 128-, and 256-point FFT megafunction performs forward or inverse fast Fourier transform (FFT) functions on complex data containing 64, 128 or 256 points. Data and twiddle factor wordlengths, pipeline degree, and memory latency are parameterized, with block-floating-point arithmetic used internally for improved computation accuracy and increased dynamic range.

The ISS FFT megafunction is based on the radix-4 decimation in frequency (DIF) algorithm. The megafunction performs the computation in two phases. The main radix-4 processor performs two-stage radix-4 operations (three for 256-point) while the post-processor performs the final stage radix-4 (for 64- or 256-point) or radix-8 (for 128-point) operation. The post-processing is in parallel with the data I/O process so that the main-processor can continuously process data without waiting for the data I/O to complete. The megafunction contains all the necessary circuits to support this continuous processing.

Modifiable Parameters

The following megafunction parameters can be modified:

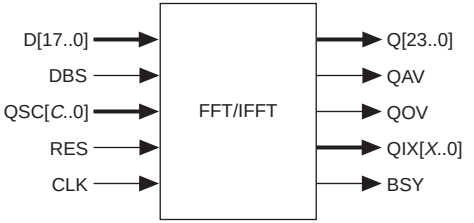
Modifiable Parameters

Parameter	Description
N	Number of points
IL	Input word length

Block Diagram

Figure 28 shows the block diagram for the FFT/IFFT megafunction.

Figure 28. FFT/IFFT Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K100A	-1	4,063	12	2.5 µs	N = 128, IL = 9

Numerically Controlled Oscillator

Vendor: Nova Engineering
Target Application:
DDS for up/down frequency conversion, frequency hopping systems, DFTs, polar to rectangular conversion, digital modulation/ demodulation
Additional Deliverables:
Simulation files
ID Code: 66A3-201

- Optimized for FLEX 10K EABs
- Generates digital sine and cosine waveforms
- Simultaneous quadrature outputs
- Parameterized phase accumulator width and output width

General Description

The numerically controlled oscillator megafunction generates digital sine and cosine waveforms at a programmable periodic rate. The sine and cosine outputs can be adjusted over a wide range of frequencies, with a high degree of resolution. The frequency resolution and tuning range are determined by the phase accumulator width and system clock. The megafunction's simultaneous quadrature outputs are ideal for quadrature modulation formats such as QPSK and QAM.

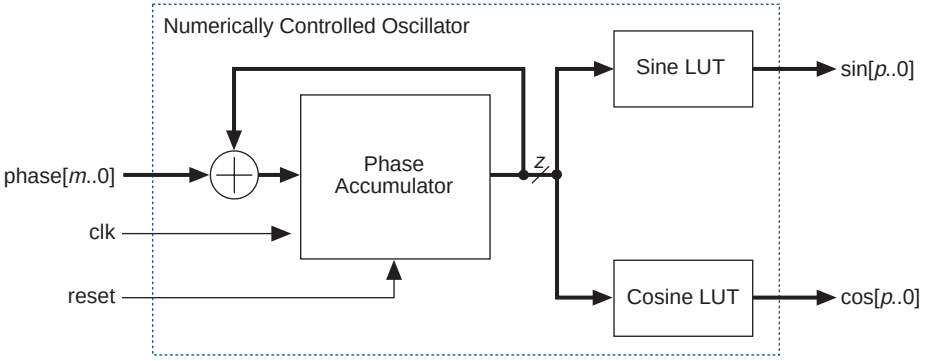
Modifiable Parameters

Nova Engineering will customize the phase accumulator and output data widths to user specifications at no additional charge. Customizing the width optimizes the megafunction for specific applications.

Block Diagram

Figure 29 shows the block diagram for the NCO megafunction.

Figure 29. NCO Megafunction Block Diagram



Device Utilization Example

Device	Speed Grade	Utilization		Performance	Parameter Setting
		Logic Cells	EABs		
EPF10K50V	-1	206	0	68 MHz	Phase accumulator width = 24 bits, output data width of 8 bits

Prototype Boards

June 1998

Table 1 lists the prototype boards offered by Altera Megafunction Partners Program (AMPP℠) partners.

Table 1. Prototype Boards Available from AMPP Partners

Partner	Board Name	Target Device Family	Application
Digital Design & Development	XM-PC	MAX 7000	MIDI
Nova Engineering	Constellation	FLEX 10K	DSP
PLD Applications	CB Lite	FLEX 10K	ATM
	PCI_GEN02	FLEX 10K	PCI
	PCI_GEN6K	FLEX 6000	PCI
Richard Watts Associates	RAW8052	FLEX 10K	8051
Sapien Design	USB	FLEX 10K	USB

Notes:

AMPP Partner Profiles

June 1998

CAST, Inc.

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http://www.cast-inc.com

Overview

CAST focuses on maximizing the success of programmable logic device (PLD) designs by supplying high-quality, high-value megafunctions for simulation and synthesis. CAST provides a total modeling solution for PLD design by delivering and supporting hardware description language (HDL) libraries with thousands of accurate, reliable, and affordable functions ready for use by designers world wide. CAST delivers the best available combination of up-front economy, long-term value, and personalized support.

The V-Custom Series library provides affordable HDL megafunctions such as processors, complex functions, and specialized devices. The series currently includes a variety of universal asynchronous receiver/transmitters (UARTs), direct memory access (DMA) controllers, microcontrollers, and digital signal processing (DSP) functions.

Products

CAST provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Processor and peripheral	C49410 microprogram controller	57	–	Now
	C8051 microcontroller unit	59	–	Now
	C2910A microprogram controller	63	–	Now
	C6850 asynchronous communication interface adapter (ACIA)	90	–	Now
	C8251 programmable communication interface	92	–	Now
	C8254 programmable interval timer/counter	76	–	Now
	C8255A programmable peripheral interface	78	–	Now
	C8259A programmable interrupt controller	80	–	Now

Target Application	Function	Catalog Page	Additional Documents	Availability
Processor and peripheral *(Continued)*	C16450 UART	94	–	Now
	C16550 UART	96	–	Now
	C_UART	98	–	Now
	DMA controller	86	–	Now
Telecom and datacom	High-level data link controller (HDLC)	102	–	Now
DSP	DES-Core	169	–	Now
	Viterbi decoder	141	Solution Brief 33	Now

Additional Services & Features

CAST provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore™ evaluation available
- Prototype/evaluation board

CoreEl MicroSystems Inc.

46750 Fremont Boulevard
Suite 208
Fremont, CA 94538

alterasales@coreel.com
http://www.coreel.com

Overview

CoreEl MicroSystems, Inc. is a leading provider of intellectual property (IP) in the areas of networking and telecommunications. The company has operations in Fremont, California and Pune, India, with over 80 employees. CoreEl provides feature-rich implementations that reduce overall system cost and greatly reduce time-to-market. CoreEl can provide a building block's register transfer language (RTL) code, along with its respective testbenches and synthesis scripts. Low-cost support for CoreCell customization, integration, integrated system validation and turnkey solutions are also available. CoreEl takes pride in quality of its design process, which includes RTL documentation, strict adherence of internal coding standards, bug tracking, and version control.

Products

CoreEl MicroSystems provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Telecom and datacom	UTOPIA level 2 master receiver	114	–	Now
	UTOPIA level 2 master transmitter	116	–	Now
	UTOPIA level 2 slave receiver	118	–	Now
	UTOPIA level 2 slave transmitter	120	–	Now
	10/100 Mbps fast ethernet MAC transmitter	–	–	Now
	10/100 Mbps fast ethernet MAC receiver	–	–	Now

Additional Services & Features

CoreEl MicroSystems provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

Digital Design & Development

18A Godshuis Street, 1861
Meise, Belgium
Tel. (32) 2-270-2797
Fax (32) 2-270-1905

73261.530@compuserve.com
http://ourworld.
compuserve.com/homepage
s/eric_lukac_kuruc/ddd.htm

Overview

Digital Design & Development (DDD) produces the eXtended MIDI (XMidi) megafunction, an improved version of the MIDI communication system. The XMidi megafunction uses both hardware and software to overcome the limitations of traditional MIDI systems, while remaining completely compatible with existing MIDI systems.

XMidi upgrades conventional MIDI in two ways:

- Expanding traditional MIDI functions and capabilities
- Adding numerous new functions

DDD provides the expertise to assist designers in understanding XMidi and integrating the system's functions in custom products.

Products

DDD provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Processor and peripheral	eXtended MIDI (XMidi)	100	–	Now

Additional Services & Features

DDD provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

Eureka Technology, Inc.

4962 El Camino Real
Suite 108
Los Altos, CA 94022
Tel. (650) 960-3800
Fax (650) 960-3805

info@eurekatech.com

Overview

Eureka Technology provides sophisticated design capabilities to assist logic designers. By offering reusable megafunctions, custom design services, and simulation models for PLD designs, Eureka Technology can help designers reduce costs and shorten design times to meet time-to-market demands. Eureka Technology supplies products for the computer, communications, and semiconductor industries.

Products

Eureka Technology provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Bus and interface	32-bit peripheral component interconnect (PCI) target	10	Solution Brief 6	Now
	32-bit PCI master/target	14	Solution Brief 19	Now
	64-bit PCI target	18	Solution Brief 6	Now
	64-bit PCI master/target	22	Solution Brief 19	Now
	PCI host bridge	29	–	Now
	PowerPC bus master	31	–	Now
	PowerPC bus slave	33	–	Now
Processor and peripheral	DMA controller	86	–	Now
	PowerPC bus arbiter	88	–	Now

Additional Services & Features

Eureka Technology provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

FASTMAN, Inc.

1613 Capitol of TX Hwy S.
Suite 222
Austin, TX 78746
Tel. (512) 328-9088
Fax (512) 328-9317

mrt@fastman.com
http://www.fastman.com

Overview

FASTMAN, Inc. develops data compression products featuring high compression rates that still maintain data quality and integrity. FASTMAN's megafunctions are based on the proprietary adaptive wavelet transform (AWT) techniques, which exceed the data-compression and quality performance of current-generation compression methods. The megafunctions are used in high-data-fidelity, high-speed data compression applications with low-bandwidth communications channels.

FASTMAN also holds several patents in data compression. RapidTransit, a software-only version of the AWT technique, delivers high-quality audio products within the evolving internet standards for communication and application interfaces.

Products

FASTMAN provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
DSP	Biorthogonal wavelet filter	145	Solution Brief 15	Now
	Decimating filter	148	Solution Brief 14	Now

Additional Services & Features

FASTMAN provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

Hammer Cores

http://www.hammercores.com

Overview

Hammer Cores offers standard megafunctions designed and optimized for Altera® programmable logic devices (PLDs). These functions are available from Hammer Cores.

Products

Hammer Cores provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Processor and peripheral	FLEXCore	67	–	Now
	RISC processor	69	–	Now
DSP	Reed-Solomon decoder	133	–	Now
	Reed-Solomon encoder	137	–	Now
	LMS & zero-forcing equalizers	152	–	Now
	Cordpol cordic function	161	–	Now

Additional Services & Features

Hammer Cores provides the following services and features:

- Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

Integrated Silicon Systems, Ltd.

29 Chlorine Gardens
Belfast, BT9 5DL,
Northern Ireland
Tel. (44) 1232-664-664
Fax (44) 1232-669-664
Sales:
Tel. (408) 727-3441
Fax (408) 727-3441

doug@iss-dsp.com
http://www.isp-dsp.com

Overview

Integrated Silicon Systems (ISS) is a DSP intellectual property company specializing in synthesizable DSP products. ISS supplies highly optimized DSP circuit functions for CPLD implementations.

Advantages

- Highly efficient silicon implementations after synthesis
- Very high performance—orders of magnitude greater than programmable DSP functions
- All blocks are fully parameterized, allowing the ultimate in design flexibility and design reuse
- ISS optimizes its functions and library blocks for Altera CPLDs and provides full technical support

Products

ISS provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
DSP	Adaptive equalizer	–	–	Now
	Cascadable adaptive finite impulse response (FIR) filter	146		
	Convolutional encoder	129	–	Now
	Discrete cosine transform (DCT/IDCT)	125	Solution Brief 9	Now
	Fast Fourier transform/ inverse fast Fourier transform (FFT/IFFT)	179	–	Now
	Floating-point operator library	163	–	Now
	IDR framer/deframer	173	Solution Brief 34	Now
	Infinite impulse response (IIR) filter library	150	Solution Brief 3	Now
	Laplacian edge detector	127	–	Now
	Numerically controlled oscillator	–	–	Now
	QPSK equalizer	155	–	Now

Target Application	Function	Catalog Page	Additional Documents	Availability
DSP *(Continued)*	Rank order filter	157	–	Now
	Reed-Solomon decoder	135	–	Now
	Reed-Solomon encoder	139	–	Now
	Viterbi decoder	141	–	Now
Telecom and datacom	HDLC controller	104	–	Now
	Multi-standard adaptive differential pulse code modulation (ADPCM)	106	Solution Brief 8	Now

Additional Services & Features

ISS provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

KTech Telecommunications, Inc.

15501 SF Mission Blvd.
Suite 100
Mission Hills, CA 91345
Tel. (818) 361-2248
Fax (818) 270-2010

skuh@ktechtelecom.com
http://www.ktechtelecom.com

Overview

KTech Telecommunications, Inc. is a design service company with experience in DSP functions designed for use in PLDs.

Products

KTech Telecommunications provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
DSP	Convolutional interleaver	131	Solution Brief 16	Now

Additional Services & Features

KTech Telecommunications provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

NComm, Inc.

401 Main Street
Suite 204
Salem, NH 03079
Tel. (603) 893-6186
Fax (603) 893-6534

info@ncomm.com

Overview

NComm, Inc. (NCI) specializes in product development for telecommunications equipment. In addition to software technology, NCI offers a growing family of telecommunications products, including megafunctions optimized for Altera PLDs. NCI's PLD solutions provide high-quality telecommunication building blocks that accelerate product development and reduce overall system costs. NCI supplies maintenance and support programs as well as consulting services.

NCI's staff has developed telecommunication functions used in switching systems, transmission equipment, private branch exchanges (PBXs), intelligent peripherals, and video equipment.

If a telecom megafunction is not currently available, NCI can create custom megafunctions upon request. The experts at NCI can work closely with the design engineers to produce the exact megafunctions required.

Products

NComm provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Telecom and datacom	Telephony tone generation	110	Solution Brief 32	Now

Additional Services & Features

NComm provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

Nova Engineering, Inc.

5 Circle Freeway Drive
Cincinnati, OH 45246-1105
Tel. (513) 860-3456
Fax (513) 860-3535

Info@nova-eng.com
http://www.nova-eng.com

Overview

Nova Engineering, Inc. specializes in the design and development of leading-edge communications and signal processing systems. Nova has comprehensive experience in military, government, and commercial electronics, with an emphasis on state-of-the-art digital communications systems. Nova's innovative solutions have resulted in numerous patents and a series of successfully deployed communications and signal processing systems.

Embedded real-time signal processing in PLDs plays a major role in virtually every Nova product. The signal processing techniques are as diverse as forward error correction (e.g., binary coded hexadecimal (BCH), Reed-Solomon, and Nadler functions), Kalman filters, digital modulation/demodulation, and low-rate, toll-quality vocoders. Nova's experience in communication product design has led to rapid prototyping using VHDL and PLDs to take advantage of the value provided by PLDs and module re-use.

Products

Nova Engineering provides the functions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
DSP	Binary pattern correlator	167	Solution Brief 18	Now
	Complex multiplier/mixer	159	Solution Brief 4	Now
	Digital modulator	175	Solution Brief 10	Now
	Early/late-gate symbol synchronizers	177	Solution Brief 17	Now
	Linear feedback shift register	165	Solution Brief 11	Now
	Numerically-controlled oscillator	181	Solution Brief 5	Now

Additional Services & Features

Nova Engineering provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

Phoenix Technologies. Ltd.

411 East Plumeria Drive
San Jose, CA 95134
Tel. (408) 570-1000
Fax (408) 570-1230

sales@vchips.com
http://www.phoenix.com

Overview

The Virtual Chips division of Phoenix Technologies, Ltd. develops and markets synthesizable functions and test environments for computer-industry standards including peripheral component interconnect (PCI), universal serial bus (USB) accelerated graphics port (AGP), CardBus, and pulse code modulation personal computer memory card international association (PCMCIA). Simulation models for specialty memories are also available.

The Virtual Chips product line is developed and maintained by experienced system designers. All products include the features, documentation, and support necessary to ensure a smooth integration into customer designs. Products are available in both Verilog HDL and VHDL.

The Virtual Chips application-optimized PCI functions are designed to ensure optimal system throughout and full PCI performance at 33 or 66 MHz. The functions are silicon-proven, and they have been verified in a wide range of applications by an installed base of over 100 customers. The Virtual Chips PCI bus test environment includes bus models, a PCI compliance test suite, and a set of macro commands to let designers create a realistic system simulation environment for PCI.

Additional Services & Features

Phoenix provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

PLD Applications

14, rue Soleillet
75971 Paris Cedex 20
France

plda@worlnet.fr
http://www.plda.com

Overview

PLD Applications is an engineering company specialized in EPLD/CPLD-based electronic systems. To provide fully competitive and highly efficient products, PLD Applications has acquired and developed competencies in high-technology domains and developed products for Altera. PLD Applications optimizes its functions for Altera FLEX® 10K and FLEX 6000 devices, and provides full technical support.

PLD Applications currently focuses on the PCI market. PLD Applications products are designed with:

- *Modularity*—Hierarchical designs, multi-blocks approach, simplified interfaces
- *Flexibility*—Zero device assignments, user-customizable function
- *Efficiency*—Knowledge of both the specifications and the target internal architecture

Products

PLD Applications provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Bus and interface	32-bit PCI target	12	Solution Brief 25	Now
	32-bit PCI master/target	16	Solution Brief 26	Now
	64-bit PCI target	20	Solution Brief 37	Now
	64-bit PCI master/target	24	–	Now
Telecom and datacom	UTOPIA level 1 ATM cell-based interface	112	Solution Brief 35	Now

Additional Services & Features

PLD Applications provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

Richard Watts Associates, Ltd.

8 Church Square
Leighton Buzzard,
Bedfordshire
LU7 7AE
England
Tel. (44) 0 1525 372621
Fax (44) 0 1525 383228

coreinfo@evolution.co.uk
http://www.evolution-uk.com/rwa

Overview

Richard Watts Associates (RWA) specializes in designing MegaCell functions for PLDs, which help designers meet the goals of high performance, lower cost, and faster time-to-market. RWA has ten years of design experience with real-time embedded system software for many different processors and DSP devices, including the 8052 device. The company can also support customers in any form of product development.

RWA's functions are designed in VHDL, which makes them independent of EDA tools and processes. Individual functions are available as behavioral VHDL, dataflow VHDL, dataflow Verilog HDL, and process-optimized blocks. MegaCell functions are supplied with high-fault coverage test vectors.

All of RWA's MegaCell functions are fully synchronous and static designs. Modern design techniques have been used to enhance performance and reduce area. Many functions are supported with extra models to aid system design, such as in hardware and software co-simulation debuggers. All MegaCell designs can be customized by RWA or the designer.

Products

Richard Watts Associates provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Processor and peripheral	BareCore 8052-A	65	–	Now
	RAW8051/8052	61	–	Now

Additional Services & Features

Richard Watts Associates provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

SAND Microelectronics, Inc.

3350 Scott Boulevard
Suite 24
Santa Clara, CA 95054
Tel. (408) 235-8600
Fax (408) 235-8601

sales@sandmicro.com
http://www.sandmicro.com

Overview

SAND Microelectronics, Inc. provides IP and related tools for industry-standard interfaces, such as PCI and USB. SAND's comprehensive IP solutions are compatible with the SANDesigner ADVantage Solutions, which include analysis, design, and verification (ADV) tools. These solutions allow designers to integrate projects quicker and more efficiently, which improves time-to-market and design integration.

SAND's analysis tools permit designers to optimize megafunction performance during simulation. With RapidScript, designers can configure the megafunctions to meet optimal requirements without changing the source code of the function.

Additional Services & Features

SAND Microelectronics provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

Sapien Design

45335 Potawatami Drive
Fremont, CA 94539
Tel. (510) 668-0200
Fax (510) 668-0200

dennis@sapiendesign.com
http://www.sapiendesign.com

Overview

Sapien Design offers standard IP products for PLDs, developed in partnership with Arasan Chip Systems of Madras, India. These products include USB synthesizable megafunctions for PLDs as well as a USB simulation test environment. The megafunctions include a USB function controller and a host controller for embedded systems.

Products

Sapien Design provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Bus and interface	USB function controller	42	Solution Brief 24	Now
	USB host controller	46	Solution Brief 28	Now

Additional Services & Features

Sapien Design provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

SICAN Microelectronics Corp.

400 Oyster Point Blvd.
Suite 512
S. San Francisco, CA 94080
Tel. (415) 871-1494
Fax (415) 871-1504

http://www.SICAN-micro.com

Overview

As a full-service design house, SICAN offers integrated circuit (IC) development services focused towards multimedia, ATM, and networking. SICAN has expertise in classical application-specific integrated circuit (ASIC) development using gate array and standard cell architectures. Its ASIC development group, called the "Design Factory," is involved in a variety of ASIC logic design projects and acts as an authorized design center for several world-class ASIC vendors, including LSI Logic and Fujitsu.

SICAN has developed special core expertise in Motion Pictures Expert Group (MPEG) video and audio encoding and decoding ICs. Its MPEG hardwired solutions enable low-cost MPEG solutions for multimedia IC and systems suppliers. SICAN licenses its multimedia IC building blocks to quickly customize projects tailored to specific customer requirements. Building blocks can be combined into functions called "DesignObjects."

SICAN has a flexible approach to development strategy. It will do a turnkey PLD design where all tasks from concept to final product are done by SICAN. The company also works on a modular sharing of tasks basis where SICAN is responsible for well-defined tasks that are part of the development project. One of the more successful models is the joint-development team where the customer and SICAN form a joint team.

Products

SICAN provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Bus and interface	CAN bus	35	Solution Brief 22	Now
	IIC master	40	Solution Brief 31	Now
	IIC slave	41	Solution Brief 31	Now
DSP	DES-Core	171	–	Now

Additional Services & Features

SICAN Microelectronics provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

Sierra Research and Technology, Inc.

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http://www.srti.com

Overview

Sierra Research and Technology, Inc. (Sierra) was incorporated in February 1993, and is headquartered in Mountain View, California. The three founders have more than 50 years of experience in engineering and management positions at some of Silicon Valley's largest and most successful companies. The technical staff at Sierra is a responsive, educated group of engineers that are well-suited to tackle advanced design projects. From concept to silicon, Sierra offers standard designs and custom design services for networking, data communications, CPU megafunctions, and storage devices.

Additional Services & Features

Sierra Research and Technology provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

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SILICON ENGINEERING, INC.

Overview

Silicon Engineering, Inc. (SEI) provides custom and semi-custom IC design capability and technology licenses for the systems, semiconductor, and consumer electronics industries.

For the past decade, SEI has applied system knowledge and design expertise to a variety of application areas, including disk drive controllers, memory controllers, networking chipsets, embedded controllers, and consumer game controllers. Designs range in complexity from 10,000 to 2 million gates.

SEI utilizes industry-standard methodologies and tools from Cadence, Synopsys, Viewlogic, and Mentor Graphics to match the designer's environment. A top-down and well-structured design methodology is followed throughout the design cycle in order to minimize design time and ensure first-pass success. Using industry-standard tools augmented with proprietary tools enables SEI to rapidly design ASICs and application-specific standard products (ASSPs) implemented in high-density PLDs.

Additional Services & Features

SEI provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

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Overview

Simple Silicon, Inc. is a provider of leading-edge digital connectivity solutions for consumer electronics, computing, audio, video, and mass storage applications. Simple Silicon's products can dramatically shorten the time-to-market and ensure first-time silicon success for your PLD-based designs.

Simple Silicon makes reusable building blocks based upon the emerging bus standards of IEEE Std. 1394 and USB for key market segments. PLD designers can use these functions as is inside their designs to create high-speed serial interfaces.

Products

Simple Silicon provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Bus and interface	IEEE 1394 link layer controller	38	–	Now
	USB function controller	44	–	Now
	USB host controller	48	–	Now
	USB hub controller	50	–	Now

Additional Services & Features

Simple Silicon provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

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Overview

SIS Microelectronics, Inc., a subsidiary of Aspec Technology, Inc., is a leader in chip integration and related professional services. Since 1982, SIS has developed the expertise in chip development that makes tomorrow's products a reality today. SIS excels when time-to-market, cost, and performance goals must all be met. The company's blend of technical expertise and program management, combined with a library of proven functional building blocks, forges strong partnerships with SIS customers and delivers consistent "first-time" working silicon.

SIS Microelectronics is founded on the principle that success in the electronics marketplace requires a partnership between the system designer and the chip manufacturer. SIS's proven team approach provides its partners with the equivalent of an "in-house" chip supplier, providing assistance for chip design and integration to companies requiring design support through the development process. SIS also works in partnerships to develop proprietary products for embedded applications in the laser printer, network, telecommunications, and mass storage markets.

Products

SIS Microelectronics provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Bus and interface	IEEE 1284 parallel slave interface	27	–	Now
	IEEE 1394-compatible LLC-I	37	Solution Brief 36	Now
Telecom and datacom	Speedbridge	108	Solution Brief 13	Now

Additional Services & Features

SIS Microelectronics provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

Synova, Inc.

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Overview

Synova is a commercial fabless semiconductor company that specializes in accelerated integrated circuit development cycles using megafunction-based design techniques. Synova's complex functions enable incorporation of digital video and embedded reduced instruction set computers (RISC) microprocessor designs into systems-on-a-chip. Synova's function-based design methodology provides decreased time-to-market solutions by providing sophisticated megafunctions for PLDs.

Additional Services & Features

Synova provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- Prototype/evaluation board

VAutomation

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Overview

VAutomation's synthesizable hardware description language (HDL) megafunctions provide designers with solid, stable, easy-to-use standard functions such as microprocessors or microperipherals. These functions allow the designer to concentrate on unique value-added features without re-inventing standard functions. Combining VAutomation megafunctions with other functional blocks and custom logic can produce systems-on-a-chip. VAutomation AMPP megafunctions are designed to allow prototyping in Altera PLDs and later migration to a custom device in a suitable target architecture.

VAutomation uses strictly synchronous HDL designs with D flipflops and logic gates that are reliable and easy to synthesize and analyze; feedback loops, multi-cycle paths, latches, and flipflop clear or set pins are not used. VAutomation megafunctions are available in both VHDL and Verilog HDL source codes. The cores come complete with verification and synthesis scripts.

Products

VAutomation provides the megafunctions shown in the following table.

Target Application	Function	Catalog Page	Additional Documents	Availability
Bus and interface	VUSB embedded host controller	52	–	Now
Processor and peripheral	V6502 microprocessor	70	–	Now
	V8-µRISC	72	–	Now
	VZ80 microprocessor	74	–	Now

Additional Services & Features

VAutomation provides the following services and features:

- ✓ Source code available
- ✓ Consulting services
- ✓ Simulation files
- ✓ Technical support
- ✓ Custom megafunctions
- ✓ OpenCore evaluation available
- ✓ Prototype/evaluation board

Notes:

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June 1998

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Abbreviations

June 1998

ACIA	Asynchronous communications interface adapter
ADC	Analog-to-digital converter
ADV	Analysis, design, and verification
ADPCM	Adaptive differential pulse code modulation
AGP	Accelerated graphics port
AHDL	Altera Hardware Description Language
ALU	Arithmetic logic unit
AM	Amplitude modulation
AMPP	Altera Megafunction Partners Program
ASIC	Application-specific integrated circuit
ASK	Amplitude shift keying
ASSP	Application-specific standard product
ATM	Asynchronous transfer mode
AWT	Adaptive wavelet transform
BAR	Base address register
BCD	Binary coded decimal
BCH	Binary coded hexadecimal
BCT	Binary coded ternary
BIST	Built-in self-test
CAD	Computer-aided design
CAN	Controller area network
CCITT	International Telegraph and Telephone Consultation Committee
CODEC	Coder/decoder
CPLD	Complex programmable logic device
CPM	Continuous phase modulation
CPU	Central processing unit
CRC	Cyclic redundancy code
DAB	Digital audio broadcast
DAC	Digital-to-analog converter
DCME	Digital circuit multiplication equipment
DCT	Discrete cosine transform
DDS	Direct digital synthesis
DFT	Discrete Fourier transform
DIF	Decimation in frequency
DMA	Direct-memory access
DRAM	Dynamic random access memory
DSP	Digital signal processing
DSS	Digital satellite system
DSSS	Direct sequence spread spectrum

DUT	Device under test
DVB	Digital video broadcast
EAB	Embedded array block
ECC	Error correction coding
ECL	Emitter-coupled logic
ECP	Extended capabilities port
EDA	Electronic design automation
EEPROM	Electrically erasable programmable read-only memory
EISA	Extended industry-standard architecture
ESC	Engineering service circuits
ETS	European Telecommunication Standards
DCME	Digital circuit multiplication equipment
DES	Data encryption standard
FEC	Forward error correction
FFT	Fast Fourier transform
FIFO	First-in first-out
FIR	Finite impulse response
FLEX	Flexible Logic Element MatriX
FM	Frequency modulation
FSK	Frequency shift keying
GUI	Graphical user interface
HDL	Hardware description language
HDLC	High-level data link controller
HEC	Header error control
IC	Integrated circuit
ICR	In-circuit reconfigurability
IDCT	Inverse discrete cosine transform
IIC	Inter integrated circuit
IP	Intellectual property
IEEE	Institute of Electrical and Electronic Engineers
IIR	Infinite impulse response
I/O	Input/output
ISA	Industry-standard architecture
ISI	Inter-symbol interference
ISP	In-system programmability
ITU	International Telegraphy Union
ISDN	Integrated services digital network
JPEG	Joint Photographic Experts Group
LAN	Local-area network
LFSR	Linear feedback shift register
LIFO	Last-in first-out
LMS	Least-mean square
LSB	Least significant bit
LUT	Look-up table
MAC	Multiplier-accumulator
MAX	Multiple Array MatriX
MCU	Microcontroller unit

MIDI	Musical instrument digital interface
MOR	Models on request
MPEG	Motion Pictures Expert Group
MSB	Most significant bit
NCO	Numerically controlled oscillator
NRZ	Non-return-to-zero
OAM	Operation and maintenance
OEM	Original equipment manufacturer
PBX	Private branch exchange
PCB	Printed circuit board
PCI	Peripheral component interconnect
PCI-SIG	Peripheral component interconnect Special Interest Group
PCM	Pulse-code modulation
PCMCIA	Personal computer memory card international association
PCS	Personal communications system
PHY	Physical layer
PID	Proportional-integral-derivative
PLD	Programmable logic device
PLL	Phase-locked loop
PN	Pseudo-random number
POTS	Plain old telephone service
PPI	Programmable peripheral interface
PSK	Phase shift keying
PVP	Packetized voice protocol
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
RAM	Random access memory
RAMDAC	Random access memory digital-to-analog converter
RF	Radio frequency
RISC	Reduced instruction set computing
RLE	Run, length encoding
ROM	Read-only memory
RTL	Register transfer level
SCVL	Standard component VHDL library
SIG	Special interest group
SRAM	Static random access memory
TCM	Trellis coded modulation
TTL	Transistor-to-transistor logic
UART	Universal asynchronous receiver/transmitter
USART	Universal synchronous/asynchronous receiver/transmitter
USB	Universal serial bus
UTOPIA	Universal xxx and operations physical interface for ATM
VME	Versa module eurocard
VLSI	Very large-scale integration
WAN	Wide-area network
XMIDI	Extended musical instrument digital interface

Notes:

I.S. EN ISO 9001