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Application Notes

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- AN 94 Understanding MAX 7000 Timing
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- AN 122 Using Jam STAPL for ISP & ICR via an Embedded Processor

Data Sheets

- BitBlaster Serial Download Cable Data Sheet
- ByteBlaster Parallel Port Download Cable Data Sheet
- ByteBlasterMV Parallel Port Download Cable Data Sheet
- MasterBlaster Serial/USB Communications Data Sheet
- MAX 9000 Programmable Logic Device Family Data Sheet
- MAX 7000 Programmable Logic Device Family Data Sheet
- MAX 7000A Programmable Logic Device Family Data Sheet
- MAX 7000B Programmable Logic Device Family Data Sheet
- MAX 3000A Programmable Logic Device Family Data Sheet

General Information

- In-Circuit Test Vendor Support
- Saving Board Space with MAX 7000S & MAX 7000A TQFP Packages

Jam Programming & Test Language

- Third-Party Programmer Support for the Jam Programming & Test Language
- Jam Programming & Test Language Specification

Product Information Bulletins

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PIB 26 Concurrent Programming through the JTAG Interface for MAX Devices

PIB 27 Jam Programming & Test Language Overview

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TB 28 Advantages of ISP-Based CPLDs

TB 32 ISP Programming Methods & Ordering Codes