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Brochures *Note (1)*

- APEX Devices Brochure
- FLEX 10K Brochure
- FLEX 6000 Brochure
- MegaCore Functions Brochure
- Quartus Brochure

Data Sheets *Note (1)*

Altera Device Package Information Data Sheet
Configuration Devices for FLEX & APEX Devices Data Sheet Version 10
fft Fast Fourier Transform Data Sheet
APEX 20K Programmable Logic Device Family Data Sheet
FLEX 10KE Embedded Programmable Logic Family Data Sheet
FLEX 10K Embedded Programmable Logic Family Data Sheet
FLEX 10K PCI Prototype Board Data Sheet
FLEX 6000 Programmable Logic Device Family Data Sheet
MAX 9000 Programmable Logic Device Family Data Sheet
MAX 7000 Programmable Logic Device Family Data Sheet
MAX 7000A Programmable Logic Device Family Data Sheet
MAX+PLUS II Programmable Logic Development System & Software Data Sheet
Operating Requirements for Altera Devices Data Sheet
PCI Master/Target MegaCore Function with DMA Data Sheet
pci_b PCI Master/Target MegaCore Function Data Sheet
pcit1 PCI Target MegaCore Function Data Sheet
Quartus Programmable Logic Development System & Software Data Sheet
SignalTap Embedded Logic Analyzer Megafunction Data Sheet

Selector Guides *Note (1)*

Component Selector Guide
Development Tools Selector Guide
Megafunctions Selector Guide

Solution Briefs *Note (1)*

SB 6 PCI Bus Target Megafunction
SB 17 Early/Late Gate Synchronizer Megafunction
SB 19 EC210 PCI Bus Master/Target Megafunction
SB 20 PCI Bus Master/Target MegaCore Function
SB 21 a8259 Programmable Interrupt Controller MegaCore Function
SB 22 CAN Bus Megafunction
SB 24 USB Function Controller Megafunction
SB 25 PCI Bus Target Interface Megafunction

SB 26	PCI Bus Master/Target Interface Megafunction
SB 28	USB Host Controller Megafunction
SB 30	crc MegaCore Function Parameterized CRC Generator/Checker
SB 32	Telephony Tone Generation Megafunction
SB 33	Viterbi Decoder Megafunction
SB 34	IDR Deframer Megafunction
SB 35	ATM Cell-Based UTOPIA Level 1 Interface Megafunction
SB 36	IEEE 1394-Compatible LLC-I Megafunction
SB 39	I2C Master Interface Megafunction
SB 40	I2C Slave Interface Megafunction
SB 41	FIR Compiler MegaCore Function
SB 42	Interleaver/Deinterleaver MegaCore Function
SB 44	64-Bit PCI Master/Target MegaCore Function

Technical Briefs *Note (1)*

TB 3	FLEX Devices as Alternatives to ASSPs & ASICs
TB 4	Using FLEX Devices as DSP Coprocessors
TB 15	Implementing a 100,000-Gate Gate Array Design in an EPF10K100 Device
TB 24	The Advantages of LPM
TB 25	Using the OpenCore Evaluation Feature
TB 26	FLEX 10K & pci_a: The Complete PCI Solution
TB 28	Advantages of ISP-Based CPLDs
TB 30	Authorization Codes Now Via the WWW
TB 32	ISP Programming Methods & Ordering Codes
TB 36	Timing-Driven Compilation Improvements in MAX+PLUS II Version 8.2
TB 38	FLEX 10KA-1 Devices: The Fastest High-Density Devices Available
TB 39	Using Synopsys Design Compiler & FPGA Compiler to Synthesize Designs for MAX+PLUS II Software
TB 41	Power Measurements: FLEX 10KA vs. XC4000 Devices
TB 42	Using Synopsys FPGA Express Software to Synthesize Designs for MAX+PLUS II Software
TB 44	Using Synplicity Synplify Software to Synthesize Designs for MAX+PLUS II Software
TB 45	Importing Synthesized Files from EDA Tools into the MAX+PLUS II Software for Place & Route
TB 48	Passing Hierarchical Timing Constraints from Synopsys Tools to MAX+PLUS II Version 9.0
TB 51	Advantages of Quartus Internet Integration

TB 60 Advantages of APEX PLLs over Virtex DLLs

White Papers *Note (1)*

Using Altera's 1.0-mm FineLine BGA Packages White Paper

Note:

- (1) To view Japanese text, you must be running the Japanese version of Acrobat Reader 3.0 and either the Windows 95-J or Windows NT 4.0J operating system. You can download the Japanese version of Acrobat Reader 3.0 from the <CD-ROM Drive>:\acroread\japan\ directory. For installation instructions, see the accompanying **readme.txt** or **readme_j.txt** file.