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November 2000

Application Briefs

AB 124 Prescaled Counters in FLEX 8000 Devices
AB 130 Parity Generators in FLEX 8000 Devices
AB 131 State Machine Encoding
AB 135 Ripple-Carry Gray Code Counters in FLEX 8000 Devices

Application Notes

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AN 71 Guidelines for Handling J-Lead, QFP & BGA Devices
AN 73 Implementing FIR Filters in FLEX Devices
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AN 82 Highly Optimized 2-D Convolvers in FLEX Devices
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AN 85 In-System Programming Times for MAX Devices
AN 86 Implementing the pci_a Master / Target in FLEX 10K Devices
AN 88 Using the Jam Language for ISP & ICR via an Embedded Processor
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AN 91 Understanding FLEX 10K Timing
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AN 94 Understanding MAX 7000 Timing
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AN 97 Comparing Performance of High-Density PLDs
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AN 101 Improving Performance in FLEX 10K Devices with the Synplify Software
AN 102 Improving Performance in FLEX 10K Devices with Leonardo Spectrum Software
AN 106 Designing with 2.5-V Devices
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AN 109 Using the HP 3070 Tester for In-System Programming
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AN 111 Embedded Programming using the 8051 & Jam Byte-Code
AN 112 Integrating Product-Term Logic in APEX 20K Devices
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AN 115 Using the ClockLock & ClockBoost Features in APEX Devices
AN 116 Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices
AN 117 Using Selectable I / O Standards in Altera Devices
AN 118 Scripting with Tcl in the Quartus Software
AN 119 Implementing High-Speed Search Applications with APEX CAM
AN 122 Using Jam STAPL for ISP & ICR via an Embedded Processor
AN 123 Using Timing Analysis in the Quartus Software
AN 125 Evaluating AMPP & MegaCore Functions
AN 128 Implementing Voice Over Internet Protocol

Brochures

APEX Devices Brochure
Quartus Brochure
Corporate Brochure
Excalibur Brochure

Customer Applications

Altera Delivers Speed for GigaNet ATM Protocol Engine Customer Application
Bailey Controls Uses Megafunctions to Solve the PCI Challenge Customer Application
FLEX 8000 Devices “Grab” Vitana’s Fancy Customer Application

Catalogs

Intellectual Property Catalog
LPM Quick Reference Guide

Data Sheets

a16450 Universal Asynchronous Receiver / Transmitter Data Sheet
a6402 Universal Asynchronous Receiver / Transmitter Data Sheet
a6850 Asynchronous Communications Interface Adapter Data Sheet
a8237 Programmable DMA Controller Data Sheet
a8251 Programmable Communications Interface Data Sheet
a8255 Programmable Peripheral Interface Adapter Data Sheet
a8259 Programmable Interrupt Controller Data Sheet
ACEX 1K Programmable Logic Family Data Sheet
Altera Device Package Information Data Sheet
Altera Programming Hardware Data Sheet
APEX 20K Programmable Logic Device Family Data Sheet
BitBlaster Serial Download Cable Data Sheet
ByteBlaster Parallel Port Download Cable Data Sheet
ByteBlasterMV Parallel Port Download Cable Data Sheet
Classic EPLD Family Data Sheet
Configuration Elements Data Sheet
Configuration Devices for APEX & FLEX Devices Data Sheet
crc MegaCore Function Parameterized CRC Generator / Checker Data Sheet

Excalibur Development Kit with the Nios Embedded Processor Data Sheet
fft Fast Fourier Transform Data Sheet
FLEX 10K Embedded Programmable Logic Family Data Sheet
FLEX 10KE Embedded Programmable Logic Family Data Sheet
FLEX 10K PCI Prototype Board Data Sheet
FLEX 10KE PCI Development Board Data Sheet
FLEX 8000 Programmable Logic Device Family Data Sheet
FLEX 6000 Programmable Logic Device Family Data Sheet
MasterBlaster Serial / USB Communications Data Sheet
MAX 9000 Programmable Logic Device Family Data Sheet
MAX 7000 Programmable Logic Device Family Data Sheet
MAX 7000A Programmable Logic Device Family Data Sheet
MAX 7000B Programmable Logic Device Family Data Sheet
MAX 3000A Programmable Logic Device Family Data Sheet
MAX+PLUS II Programmable Logic Development System & Software Data Sheet
Nios Soft Core Embedded Processor Data Sheet
Operating Requirements for Altera Devices Data Sheet
PCI Master / Target MegaCore Function with DMA Data Sheet
pci_b PCI Master / Target MegaCore Function Data Sheet
pcit1 PCI Target MegaCore Function Data Sheet
QFP Carrier & Development Socket Data Sheet
Quartus Programmable Logic Development System & Software Data Sheet
RGB2YCrCb & YCrCb2RGB Color Space Converters Data Sheet
SignalTap Embedded Logic Analyzer Megafunction Data Sheet

Functional Specifications

FS 1 FIR Filters
FS 2 fp_add_sub Floating-Point Adder / Subtractor
FS 4 fp_mult Floating-Point Multiplier
FS 5 round Data Word Rounder
FS 6 saturate Data Word Saturator
FS 7 fft_on_chip Fast Fourier Transform

General Information

Abbreviations
About this CD-ROM
BASELINE & E+MAX Installation Instructions
EDA Software Support
E+MAX Overview
In-Circuit Test Vendor Support
Glossary
How to Contact Altera
Introduction (to the Altera ***1999 Data Book***)
Jam Byte-Code Compiler Version 2.09 README File
Jam Byte-Code Player Version 2.09 README File
Jam Compiler & Player Installation Instructions
Jam Player Version 2.12 README File
Jam Programming & Test Language Specification
Legal Notice
MAX+PLUS II BASELINE Overview
MAX+PLUS II Version 10.0 READ.ME File
Ordering Information
Programming Hardware Manufacturers
Sales Offices, Distributors & Representatives
Saving Board Space with MAX 7000S & MAX 7000A TQFP Packages
Technical Support from Altera Applications
Third-Party Programmer Support for the Jam Programming & Test Language

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PIB 20 Benefits of Embedded RAM in FLEX 10K Devices
PIB 21 Implementing Logic with the Embedded Array in FLEX 10K Devices
PIB 22 Design Tools for 100,000 Gate Programmable Logic Devices
PIB 23 Digital Signal Processing in FLEX Devices
PIB 24 Advantages of ISP-Based PLDs over Traditional PLDs
PIB 26 Concurrent Programming through the JTAG Interface for MAX Devices
PIB 27 Jam Programming & Test Language Overview

PIB 29 LVDS Comparison APEX 20KE vs. Virtex-E Devices

Selector Guides

Component Selector Guide

Development Tools Selector Guide

Intellectual Property Selector Guide

Solution Briefs

SB 2 High-Speed Adaptive FIR Filter Megafunction

SB 3 Biquad IIR Filter Megafunction

SB 4 Complex Multiplier / Mixer Megafunction

SB 5 Numerically Controlled Oscillator Megafunction

SB 6 PCI Bus Target Megafunction

SB 8 ADPCM Megafunction

SB 9 Discrete Cosine Transform Megafunctions

SB 10 Digital Modulator Megafunction

SB 11 Linear Feedback Shift Register Megafunction

SB 12 Fast Fourier Transform MegaCore Function

SB 13 Speedbridge Megafunction

SB 16 Convolutional Interleaver Megafunction

SB 17 Early / Late Gate Synchronizer Megafunction

SB 18 Binary Pattern Correlator Megafunction

SB 19 EC210 PCI Bus Master / Target Megafunction

SB 20 PCI Bus Master / Target MegaCore Function

SB 21 a8259 Programmable Interrupt Controller MegaCore Function

SB 22 CAN Bus Megafunction

SB 23 Microperipheral MegaCore Library

SB 24 USB Function Controller Megafunction

SB 25 PCI Bus Target Interface Megafunction

SB 26 PCI Bus Master / Target Interface Megafunction

SB 27 RGB2YCrCb & YCrCb2RGB Color Space Converter MegaCore Functions

SB 28 USB Host Controller Megafunction

SB 30 crc MegaCore Function Parameterized CRC Generator / Checker

SB 32 Telephony Tone Generation Megafunction
SB 33 Viterbi Decoder Megafunction
SB 34 IDR Deframer Megafunction
SB 36 IEEE 1394-Compatible LLC-I Megafunction
SB 37 64-Bit PCI Bus Target Megafunction
SB 38 SDRAM Controller Megafunction
SB 39 I2C Master Interface Megafunction
SB 40 I2C Slave Interface Megafunction
SB 41 FIR Compiler MegaCore Function
SB 42 Interleaver / Deinterleaver MegaCore Function
SB 44 64-Bit PCI Master / Target MegaCore Function
SB 46 FLEX PCI Development Kit
SB 47 System-on-a-Programmable-Chip (SOPC) Development Board

Technical Briefs

TB 3 FLEX Devices as Alternatives to ASSPs & ASICs
TB 4 Using FLEX Devices as DSP Coprocessors
TB 5 Implementing Multipliers in FLEX 10K EABs
TB 8 Implementing Multirate Filters in FLEX Devices
TB 15 Implementing a 100,000-Gate Gate Array Design in an EPF10K100 Device
TB 24 The Advantages of LPM
TB 25 Using the OpenCore Evaluation Feature
TB 26 FLEX 10K & pci_a: The Complete PCI Solution
TB 28 Advantages of ISP-Based CPLDs
TB 29 Internal Tri-State Emulation
TB 30 Authorization Codes Now Via the WWW
TB 31 The Advantages of FLEX 10K Devices Versus Lucent ORCA Devices
TB 32 ISP Programming Methods & Ordering Codes
TB 33 Evaluating MAX 7000S Device Utilization & Fitting
TB 34 MAX 7000S Power Consumption
TB 38 FLEX 10KA-1 Devices: The Fastest High-Density Devices Available
TB 39 Using Synopsys Design Compiler & FPGA Compiler to Synthesize Designs for MAX+PLUS II Software
TB 40 Advantages of MAX+PLUS II Fitting
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TB 42 Using Synopsys FPGA Express Software to Synthesize Designs for MAX+PLUS II Software

TB 43 Using the MAX+PLUS II Software with Exemplar Logic Leonardo Software

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TB 45 Importing Synthesized Files from EDA Tools into the MAX+PLUS II Software for Place & Route

TB 48 Passing Hierarchical Timing Constraints from Synopsys Tools to MAX+PLUS II Version 9.0

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TB 51 Advantages of Quartus Internet Integration

TB 52 Increasing Performance Using ATOM Netlist Files

TB 53 Quartus Software Feature Comparison with Xilinx Alliance 2.1i

TB 54 Quartus Revision Control Software Support

TB 56 Using APEX 20KE CAM for Fast Search Applications

TB 57 Power Consumption Comparison: APEX 20K vs. Virtex Devices

TB 58 In-Circuit Test Support with MAX 7000 Devices

TB 59 Hierarchical Design Methodology with the Quartus Software

TB 60 Advantages of APEX PLLs Over Virtex DLLs

TB 61 CAM Comparison: APEX 20KE vs. Virtex-E Devices

TB 62 MAX 7000AE Performance Comparison

TB 63 Programming Time Comparison: MAX 7000AE vs. XC9500XL Devices

TB 64 New Features of the Quartus Software Version 2000.02

TB 65 Design Fitting: MAX 7000AE vs. ispLSI 2000VE Devices

TB 67 Advanced Synthesis with LeonardoSpectrum

TB 68 Advanced Synthesis with FPGA Express

TB 69 HDL Simulation with the Model*Sim*–Altera Software

User Guides & Software Manuals

FPGAExpress–Altera Software Installation Instructions

FIR Compiler MegaCore Function User Guide

Installing the Visual IP Software User Guide

LeonardoSpectrum–Altera Software Installation Instructions

MAX+PLUS II Getting Started Manual

pci_b & pcit1 MegaCore Function User Guide

pci_c MegaCore Function User Guide

PCI MegaCore Function User Guide
PCI-X MegaCore Function User Guide
Quartus Installation & Licensing for PCs
Quartus Installation & Licensing for UNIX Workstations
Reed-Solomon Compiler MegaCore Function User Guide
Reed-Solomon MegaCore Function User Guide
Simulating the a6402 Model with the Visual IP Software User Guide
Simulating the a8237 Model with the Visual IP Software User Guide
Simulating the a8251 Model with the Visual IP Software User Guide
Simulating the a8259 Model with the Visual IP Software User Guide
Symbol Interleaver / De-Interleaver MegaCore Function User Guide
System-on-a-Programmable-Chip Development Board User Guide
Turbo Encoder / Decoder MegaCore Function User Guide

White Papers

5.0-Volt Tolerance in APEX 20KE Devices
8b / 10b Encoders White Paper
Arctan Function White Paper
Area Optimized Soft Decision Viterbi Decoder Functions White Paper
ATF1500AS Analysis Report White Paper
CORDIC Functions CDPP & CDPS White Paper
DDR SDRAM Decoders White Paper
DES Cores White Paper
Implementing ATM Switch with APEX Embedded CAM White Paper
NCO Core White Paper
Reed-Solomon FEC Demonstration White Paper
Turbo Codec FEC Demonstration White Paper
u-Law Companders & A-Law Companders White Paper
Using APEX 20KE CAM with the Quartus Software Design Tool
Using LVDS in the Quartus Software
Viterbi Decoders White Paper