FLEX 10KE PCI Development Board

June 2000, ver. 1.01 Data Sheet

Features

- Universal 64-bit, 66-MHz peripheral component interconnect (PCI) expansion card
- Includes the FLEX® 10KE EPF10K100EFC-1 device
- On-board 144-pin small outline DIMM 32-Mbyte SDRAM module
- On-board standard PCI Mezzanine card (PMC) connector
- I/O prototype area
- RS-232 port
- On-board voltage regulator automatically generates 2.5 V and 3.3 V from a 5.0-V power supply
- Flexible clocking options for the local-side logic, including PCI clock, on-board crystal oscillator, or external clock input
- Supports in-circuit reconfigurability (ICR) with an EPC2 configuration device and a MasterBlaster™, ByteBlasterMV™, ByteBlaster™, or BitBlaster™ download cable. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable.)
- Designed to accept the following devices:
  - EPF10K30EFC484
  - EPF10K50EFC484
  - EPF10K50SFC484
  - EPF10K100EFC484
  - EPF10K130EFC484
  - EPF10K130EFC672
  - EPF10K200EFC672
  - EPF10K200SFC672

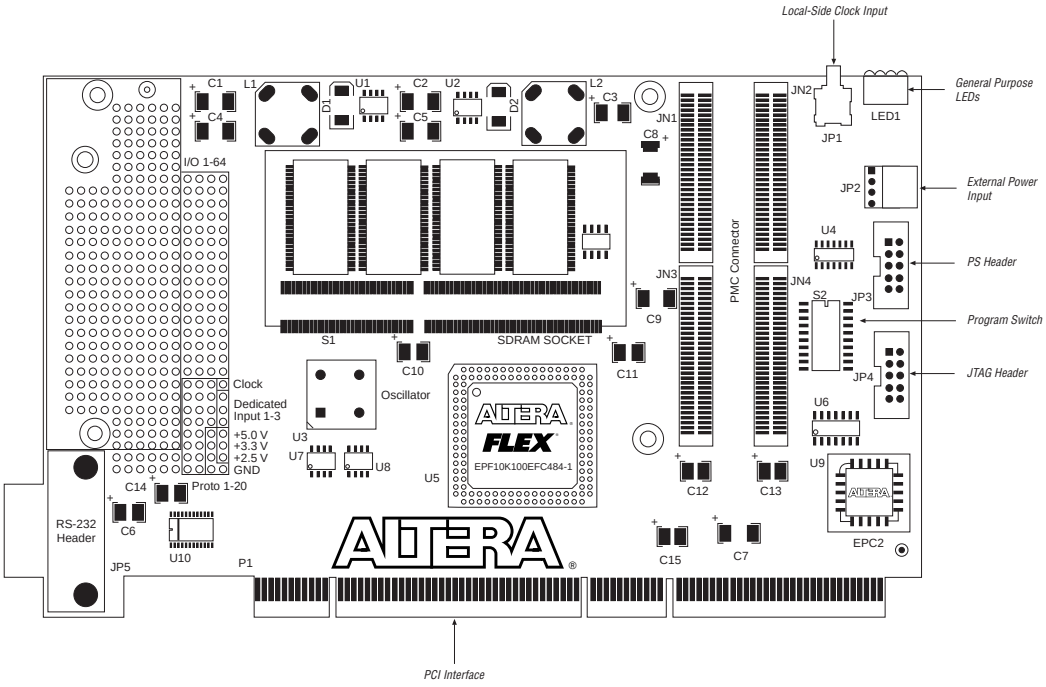
General Description

The PCI development board works with all Altera® PCI MegaCore™ functions, including `pci_a`, `pci_b`, `pci_c`, and `pcit1` (a back-end reference design for each megafunction is required). Users can implement custom local-side functions to interface the Altera PCI MegaCore function with the on-board SDRAM socket, the on-board PMC connector, the RS-232 port, or any custom logic implemented in the prototype area or PMC. The PCI development board provides a flexible clock network distribution and in-circuit configuration options. It supports a wide range of FLEX 10KE devices so users can tailor the development board to meet I/O pin and area requirements. This data sheet provides information on FLEX 10KE pin assignments, programming and configuration settings, clock network selection, supported components, board options, and schematics for the Altera FLEX 10KE PCI development board.

Functional Description

Figure 1 shows the FLEX 10KE PCI development board.

Figure 1. FLEX 10KE PCI Development Board



FLEX 10KE Pin Assignments

Pin assignments to FLEX 10KE devices ensure that its I/O pins are properly connected to the defined signals on the board. Table 1 shows the definitions for the pin assignments.

Table 1. Pin Assignment Reference Definitions

Pin Name	Board Components	Definition
e_<*pci_signal*>	JN1, JN2, JN3	Standard PMC connectors.
p4_io<*n*>	JN4	Additional PMC I/O pins.
p5_io<*n*>	I/O 1-64	User prototype area I/O pins.
p_<*pci_signal*>	P1	64-bit universal board PCI connector.
a_<*name*>	U5	Altera FLEX 10KE I/O.
s_<*name*>	S1	SDRAM module.
proto<*n*>	Proto 1-20	Prototype outputs from the FLEX 10KE device.
rs232_<*name*>	U10	RS-232 interface signals.
led<*n*>	LED1	Input signals to general-purpose LEDs.
sw<*n*>	S2	Switch connected to the FLEX 10KE I/O.

Before compiling the FLEX 10KE design for the PCI development board, pin assignments must be made to all defined pins. See Table 2.

Table 2. FLEX 10KE PCI Development Board Pin Assignments (Part 1 of 7)

Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA	Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA
e_ack64n	C18	E20	e_ad4	D3	F5
e_ad0	D1	F3	e_ad40	L17	N19
e_ad1	E2	G4	e_ad41	K21	M23
e_ad10	B9	D11	e_ad42	K22	M24
e_ad11	C10	E12	e_ad43	L18	N20
e_ad12	A11	C13	e_ad44	L22	N24
e_ad13	A12	C14	e_ad45	L20	N22
e_ad14	B12	D14	e_ad46	L21	N23
e_ad15	C12	E14	e_ad47	L19	N21
e_ad16	C13	E15	e_ad48	M22	P24
e_ad17	A14	C16	e_ad49	M21	P23
e_ad18	C14	E16	e_ad5	D2	F4
e_ad19	E20	G22	e_ad50	L16	N18
e_ad2	C1	E3	e_ad51	M19	P21
e_ad20	D21	F23	e_ad52	N22	R24

Table 2. FLEX 10KE PCI Development Board Pin Assignments (Part 2 of 7)

Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA	Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA
e_ad21	D22	F24	e_ad53	M18	P20
e_ad22	F20	H22	e_ad54	N21	R23
e_ad23	H16	K18	e_ad55	M17	P19
e_ad24	E22	G24	e_ad56	P21	T23
e_ad25	F21	H23	e_ad57	R21	U23
e_ad26	G20	J22	e_ad58	U22	W24
e_ad27	J16	L18	e_ad59	U21	W23
e_ad28	G22	J24	e_ad6	C6	E8
e_ad29	J18	L20	e_ad60	Y20	AB22
e_ad3	E3	G5	e_ad61	AB21	AD23
e_ad30	J17	L19	e_ad62	AB22	AD24
e_ad31	J19	L21	e_ad63	Y19	AB21
e_ad32	H22	K24	e_ad7	A7	C9
e_ad33	K15	M17	e_ad8	C9	E11
e_ad34	K16	M18	e_ad9	A9	C11
e_ad35	J21	L23	e_bm1	W2	AA4
e_ad36	K17	M19	e_bm2	V2	Y4
e_ad37	J22	L24	e_bm3	U2	W4
e_ad38	K18	M20	e_bm4	U3	W5
e_ad39	K19	M21	e_cben0	B19	D21
e_cben1	F17	H19	p4_io17	*(1)*	H26
e_cben2	A21	C23	p4_io18	*(1)*	J25
e_cben3	E17	G19	p4_io19	*(1)*	J26
e_cben4	B20	D22	p4_io2	*(1)*	B15
e_cben5	D18	F20	p4_io20	*(1)*	K25
e_cben6	C19	E21	p4_io21	*(1)*	K26
e_cben7	D19	F21	p4_io22	*(1)*	L25
e_devseln	B18	D20	p4_io23	*(1)*	L26
e_framen	D17	F19	p4_io24	*(1)*	M26
e_gntn	E15	G17	p4_io25	*(1)*	N25
e_idsel	AA21	AC23	p4_io26	*(1)*	N26
e_intan	W1	AA3	p4_io27	*(1)*	P25
e_intbn	T2	V4	p4_io28	*(1)*	P26
e_intcn	R2	U4	p4_io29	*(1)*	R26
e_intdn	P3	T5	p4_io3	*(1)*	B17
e_irdyn	C16	E18	p4_io30	*(1)*	R25

Table 2. FLEX 10KE PCI Development Board Pin Assignments (Part 3 of 7)

Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA	Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA
e_lockn	V20	Y22	p4_io31	P20	T22
e_par	D20	F22	p4_io32	P22	T24
e_par64	C20	E22	p4_io33	*(1)*	T26
e_perrn	G18	J20	p4_io34	*(1)*	U25
e_req64n	A20	C22	p4_io35	*(1)*	U26
e_reqn	A15	C17	p4_io36	T20	V22
e_rstn	U20	W22	p4_io37	T21	V23
e_sbo	N2	R4	p4_io38	*(1)*	V26
e_sdone	M3	P5	p4_io39	T22	V25
e_serrn	C22	E24	p4_io4	*(1)*	B18
e_stopn	A19	C21	p4_io40	*(1)*	W25
e_trdyn	A18	C20	p4_io41	*(1)*	W26
p4_io1	*(1)*	B14	p4_io42	*(1)*	Y25
p4_io10	*(1)*	D26	p4_io43	*(1)*	AA25
p4_io11	*(1)*	E25	p4_io44	*(1)*	Y26
p4_io12	*(1)*	E26	p4_io45	*(1)*	AB26
p4_io13	*(1)*	F25	p4_io46	W22	AA24
p4_io14	*(1)*	G25	p4_io47	*(1)*	AC25
p4_io15	*(1)*	F26	p4_io48	*(1)*	AB25
p4_io16	*(1)*	G26	p4_io49	*(1)*	AC26
p4_io5	C17	E19	p5_io24	*(1)*	J2
p4_io50	*(1)*	AD25	p5_io25	*(1)*	J1
p4_io51	*(1)*	AE24	p5_io26	*(1)*	K2
p4_io52	*(1)*	AF22	p5_io27	*(1)*	K1
p4_io53	*(1)*	AD26	p5_io28	*(1)*	L2
p4_io54	*(1)*	AE26	p5_io29	J3	L5
p4_io55	AB20	AD22	p5_io3	*(1)*	A8
p4_io56	AB19	AD21	p5_io30	J1	L3
p4_io57	AB18	AD20	p5_io31	J2	L4
p4_io58	*(1)*	AF19	p5_io32	*(1)*	L1
p4_io59	AB17	AD19	p5_io33	*(1)*	M1
p4_io6	*(1)*	B26	p5_io34	*(1)*	N2
p4_io60	Y16	AB18	p5_io35	*(1)*	N1
p4_io61	*(1)*	AE18	p5_io36	L1	N3
p4_io62	AA15	AC17	p5_io37	*(1)*	P2
p4_io63	*(1)*	AF17	p5_io38	*(1)*	P1

Table 2. FLEX 10KE PCI Development Board Pin Assignments (Part 4 of 7)

Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA	Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA
p4_io64	AB15	AD17	p5_io39	M2	P4
p4_io7	*(1)*	C26	p5_io4	*(1)*	A7
p4_io8	*(1)*	D25	p5_io40	*(1)*	R1
p4_io9	*(1)*	C25	p5_io41	*(1)*	R2
p5_io1	B10	D12	p5_io42	*(1)*	U1
p5_io10	B3	D5	p5_io43	*(1)*	U2
p5_io11	*(1)*	A3	p5_io44	*(1)*	V1
p5_io12	A4	C6	p5_io45	*(1)*	V2
p5_io13	*(1)*	C2	p5_io46	*(1)*	W1
p5_io14	*(1)*	B1	p5_io47	U1	W3
p5_io15	*(1)*	D2	p5_io48	*(1)*	W2
p5_io16	*(1)*	D1	p5_io49	*(1)*	Y1
p5_io17	*(1)*	E1	p5_io5	A5	C7
p5_io18	*(1)*	E2	p5_io50	*(1)*	AA2
p5_io19	*(1)*	F2	p5_io51	*(1)*	AA1
p5_io2	*(1)*	A9	p5_io52	*(1)*	AB2
p5_io20	*(1)*	F1	p5_io53	*(1)*	AB1
p5_io21	*(1)*	G2	p5_io54	R3	U5
p5_io22	*(1)*	G1	p5_io55	*(1)*	AC1
p5_io23	F2	H4	p5_io56	*(1)*	AC2
p5_io57	*(1)*	AD2	p_ad24	T4	V6
p5_io58	*(1)*	AD1	p_ad25	T6	V8
p5_io59	AB5	AD7	p_ad26	R6	U8
p5_io6	A3	C5	p_ad27	R5	U7
p5_io60	AB3	AD5	p_ad28	R7	U9
p5_io61	Y9	AB11	p_ad29	R4	U6
p5_io62	AA9	AC11	p_ad3	AA7	AC9
p5_io63	*(1)*	AF11	p_ad30	P4	T6
p5_io64	AB9	AD11	p_ad31	P6	T8
p5_io7	A2	C4	p_ad32	W16	AA18
p5_io8	B4	D6	p_ad33	AA18	AC20
p5_io9	*(1)*	B3	p_ad34	U16	W18
a_clk2	D12	F14	p_ad35	AA17	AC19
a_clkout	D15	F17	p_ad36	T16	V18
led1	E16	G18	p_ad37	W15	AA17
led2	D16	F18	p_ad38	AA16	AC18

Table 2. FLEX 10KE PCI Development Board Pin Assignments (Part 5 of 7)

Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA	Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA
led3	A17	C19	p_ad39	U15	W17
led4	A16	C18	p_ad4	W8	AA10
p_ack64n	Y10	AB12	p_ad40	V15	Y17
p_ad0	U9	W11	p_ad41	Y15	AB17
p_ad1	AA8	AC10	p_ad42	V14	Y16
p_ad10	V7	Y9	p_ad43	W14	AA16
p_ad11	Y7	AB9	p_ad44	U14	W16
p_ad12	AB6	AD8	p_ad45	T14	V16
p_ad13	U7	W9	p_ad46	R13	U15
p_ad14	U6	W8	p_ad47	Y14	AB16
p_ad15	AA5	AC7	p_ad48	T13	V15
p_ad16	V6	Y8	p_ad49	AA14	AC16
p_ad17	Y5	AB7	p_ad5	V8	Y10
p_ad18	W6	AA8	p_ad50	U13	W15
p_ad19	W5	AA7	p_ad51	AB14	AD16
p_ad2	T9	V11	p_ad52	W13	AA15
p_ad20	W4	AA6	p_ad53	V13	Y15
p_ad21	W3	AA5	p_ad54	T12	V14
p_ad22	U5	W7	p_ad55	U12	W14
p_ad23	T5	V7	p_ad56	V12	Y14
p_ad57	W12	AA14	p_stopn	U10	W12
p_ad58	U11	W13	p_stopn_in	H11	K13
p_ad59	Y11	AB13	p_trdyn	T10	V12
p_ad6	U8	W10	p_trdyn_in	R12	U14
p_ad60	T11	V13	Proto1	H13	K15
p_ad61	AB10	AD12	Proto10	R17	U19
p_ad62	R11	U13	Proto11	R19	U21
p_ad63	AA10	AC12	Proto12	R20	U22
p_ad7	Y6	AB8	Proto13	N19	R21
p_ad8	T8	V10	Proto14	G2	J4
p_ad9	W7	AA9	Proto15	Y4	AB6
p_cben0	Y17	AB19	Proto16	AB2	AD4
p_cben1	V16	Y18	Proto17	AA4	AC6
p_cben2	R16	U18	Proto18	AA3	AC5
p_cben3	AA19	AC21	Proto19	AA2	AC4
p_cben4	W17	AA19	Proto2	G13	J15

Table 2. FLEX 10KE PCI Development Board Pin Assignments (Part 6 of 7)

Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA	Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA
p_cben5	W18	AA20	Proto20	AB1	AD3
p_cben6	V17	Y19	Proto3	P16	T18
p_cben7	V18	Y20	Proto4	N15	R17
a_clk1	P11	T13	Proto5	P17	T19
p_devseln	V10	Y12	Proto6	N16	R18
p_framen	W9	AA11	Proto7	V1	Y3
p_gntn	W10	AA12	Proto8	T18	V20
p_idsel	N8	R10	Proto9	V21	Y23
p_intan	T17	V19	rs232_cd	L15	N17
p_irdyn	R10	U12	rs232_cts	N17	R19
p_irdyn_in	V11	Y13	rs232_DTR	P18	T20
p_lockn	R18	U20	rs232_ri	N18	R20
p_M66EN	N5	R7	rs232_RTS	M16	P18
p_par	Y18	AB20	rs232_rx	M15	P17
p_par64	AA20	AC22	rs232_tx	P19	T21
p_perrn	U19	W21	s_A0	G6	J8
p_req64n	V9	Y11	s_A1	F4	H6
p_reqn	T19	V21	s_A10	C7	E9
p_rstn	E12	G14	s_A11	D5	F7
p_serrn	U17	W19	s_A12	F6	H8
s_A13	E7	G9	s_dq29	D9	F11
s_A2	G4	J6	s_dq3	K6	M8
s_A3	G5	J7	s_dq30	H10	K12
s_A4	C3	E5	s_dq31	E9	G11
s_A5	H7	K9	s_dq32	F10	H12
s_A6	B6	D8	s_dq33	D10	F12
s_A7	F3	H5	s_dq34	E10	G12
s_A8	F8	H10	s_dq35	A10	C12
s_A9	E6	G8	s_dq36	F11	H13
s_ba0	P5	T7	s_dq37	G10	J12
s_ba1	P1	T3	s_dq38	E11	G13
s_casn	M5	P7	s_dq39	D11	F13
s_cke0	N7	R9	s_dq4	K7	M9
s_cke1	M4	P6	s_dq40	B11	D13
s_dq0	K4	M6	s_dq41	G11	J13
s_dq1	K1	M3	s_dq42	F12	H14

Table 2. FLEX 10KE PCI Development Board Pin Assignments (Part 7 of 7)

Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA	Signal Name	484-Pin FineLine BGA	672-Pin FineLine BGA
s_dq10	J6	L8	s_dq43	G12	J14
s_dq11	H3	K5	s_dq44	H12	K14
s_dq12	H5	K7	s_dq45	B13	D15
s_dq13	J7	L9	s_dq46	D13	F15
s_dq14	H6	K8	s_dq47	F13	H15
s_dq15	F7	H9	s_dq48	E13	G15
s_dq16	C5	E7	s_dq49	D14	F16
s_dq17	D6	F8	s_dq5	K8	M10
s_dq18	C4	E6	s_dq50	B14	D16
s_dq19	B7	D9	s_dq51	E14	G16
s_dq2	K5	M7	s_dq52	B15	D17
s_dq20	D7	F9	s_dq53	F14	H16
s_dq21	D8	F10	s_dq54	G19	J21
s_dq22	G7	J9	s_dq55	F16	H18
s_dq23	C8	E10	s_dq56	F22	H24
s_dq24	E8	G10	s_dq57	G17	J19
s_dq25	B8	D10	s_dq58	F15	H17
s_dq26	G9	J11	s_dq59	H19	K21
s_dq27	F9	H11	s_dq6	H1	K3
s_dq28	G8	J10	s_dq60	G16	J18
s_dq61	H18	K20	s_dqmb5	L3	N5
s_dq62	H21	K23	s_dqmb6	L7	N9
s_dq63	H17	K19	s_dqmb7	L8	N10
s_dq7	J5	L7	s_rasn	M6	P8
s_dq8	J4	L6	s_s0n	P7	T9
s_dq9	H4	K6	s_s1n	N6	R8
s_dqmb0	M1	P3	s_scl	P2	T4
s_dqmb1	M7	P9	s_sda	N4	R6
s_dqmb2	M8	P10	s_wen	L5	N7
s_dqmb3	L4	N6	sw9	G14	J16
s_dqmb4	L6	N8	–	–	–

Note:
(1) These pins are designated as no connect pins.

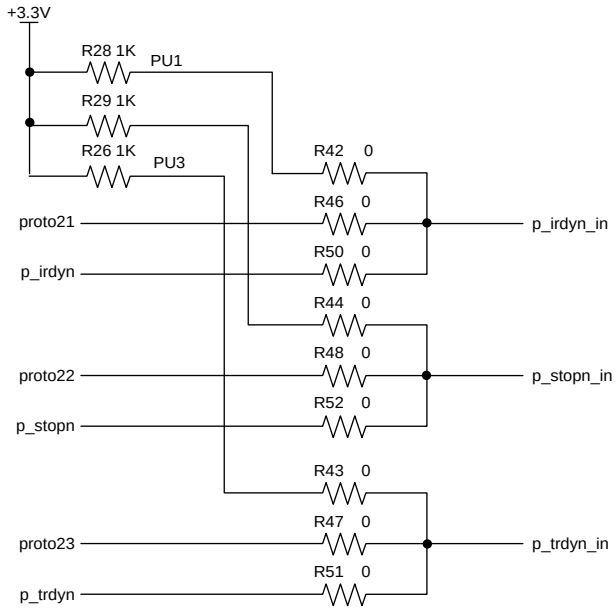
Dedicated Input Selection

The FLEX 10KE PCI development board provides a dedicated input selection circuitry, and performs the following functions:

- Sets split-pin configuration for high fan-out PCI signals (`trdyn`, `irdyn`, and `stopn`).
- Drives available dedicated inputs with external signals.
- Provides pull-up resistors to dedicated inputs.

Dedicated input configuration can be selected by installing or removing various 0 Ω resistors. Figure 2 shows a schematic of the board's dedicated input selectors.

Figure 2. Dedicated Input Selectors



The PCI development board is shipped with R42, R43, and R44 installed. This configuration provides a pull-up resistor for each of the three available dedicated inputs.

Programming & Configuration Settings/Defaults

The PCI development board supports on-board configuration device programming and in-circuit configuration for FLEX devices (via JP3) for Joint Test Action Group (JTAG) or passive serial (PS) mode (via JP4) with the MasterBlaster or ByteBlasterMV download cable. Table 3 shows the programming and configuration options available and their settings.

Table 3. Programming & Configuration Options

Mode/ Device(s)	MasterBlaster/ ByteBlaster/	DIP Switch Settings *(1)*	Description
JTAG EPC2	Connected to JTAG header	0000000001	Programs the EPC2 device in JTAG mode using the MAX+PLUS® II software. This setting is the default for the board.
JTAG EPC2, FLEX	Connected to JTAG header	0000000110	Places the EPC2 device and FLEX device in the JTAG chain (where the EPC2 device is device 0 and the FLEX device is device 1) and configures FLEX devices using the MAX+PLUS II software.
JTAG EPC2, FLEX, PMC	Connected to JTAG header	0001111010	Places the EPC2 device, FLEX device, and the PMC connector in the JTAG chain (where the EPC2 device is device 0, the FLEX device is device 1, and the PMC is device 2) and configures the device connected to the PMC connector using the MAX+PLUS II software.
PS	Connected to BitBlaster header	0000000000	Configures the FLEX device in PS mode using the MAX+PLUS II software.
Configuration with EPC2	Removed	1000000000	Configures the FLEX device with the programmed EPC2 device.

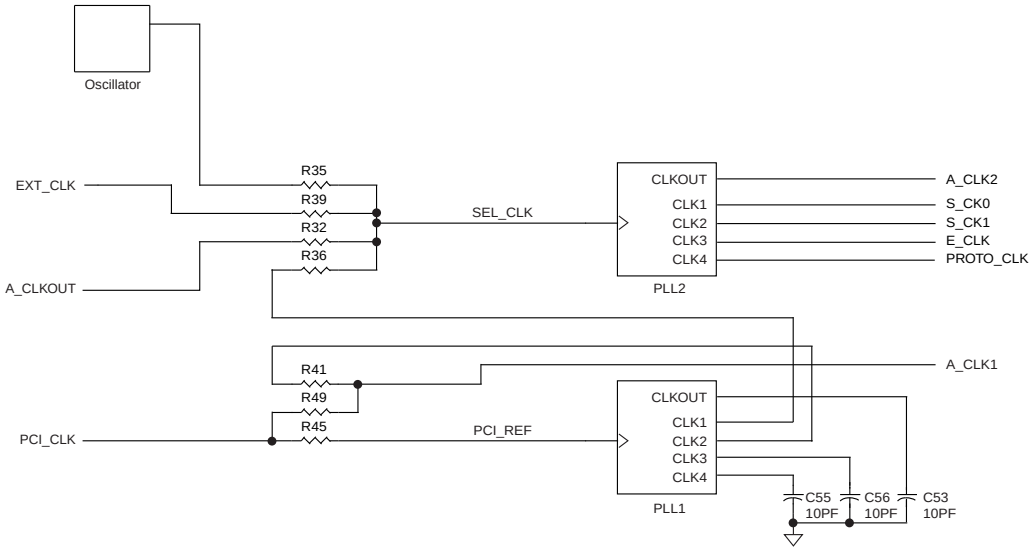
Note:

(1) The DIP switch setting is indicated with a 10-bit binary number where bit 0 refers to switch 1, and bit 9 refers to switch 10 on S2. A value of 1 indicates that the corresponding switch is in the on position, and a value of 0 indicates that the corresponding switch is in the off position. Switch 9 is not a part of the programming and configuration circuit. It is connected to an input of the FLEX 10KE device.

Clock Network Selection/Default

The clock signal on the PCI development board can arrive from various clocking sources including system clock, external clock, and on-board crystal oscillator. The zero-delay buffers provide zero-delay clock signal distribution throughout the board to minimize clock skew within the same clock network. Clocking options on the board can be selected by installing or removing various 0 Ω resistors. Figure 3 shows a schematic of the board's clock distribution circuit.

Figure 3. Clock Distribution Circuit



The SDRAM, PMC, prototype area, and FLEX 10KE local-side clock inputs can be connected from the system clock (PCI_CLK), external clock input, on-board crystal oscillator, or FLEX clock output by installing the appropriate resistors. The FLEX 10KE clock input (A_CLK1) can be driven directly from the system clock or the output of PLL1. For example, to select the system clock to drive the FLEX 10KE clock input directly, R49 is installed; to select the external clock as the clocking source for the SDRAM socket, PMC connector, and prototype area, R39 is installed.

The PCI development board is shipped with R41, R45, and R36 installed. These resistors select the system clock (PCI_CLK) as the clocking source for the FLEX 10KE device, the SDRAM socket, the prototype area, and the PMC connector.

Voltage Supply Circuit

The FLEX 10KE PCI development board has special voltage regulator circuitry, which allows the necessary 2.5-V and 3.3-V power supply to be generated from a 5.0-V input. The board can accept the 5.0-V input from either the PCI connector or an external power supply (via JP2).

Using the external power supply input while the board is plugged into the PCI connector slot may result in severe board damage and possibly system damage.

Supported Components

Table 4 lists all components supported by the PCI development board; however, not all components are shipped with the board. See "Board Options" on page 15 for more information.

Table 4. Supported Components (Part 1 of 2)

Component	Manufacturer Part Number	Quantity	Schematic Reference
CAPACITOR, 0.01UF, 0805	AVX:08055E104ZAT	46	C16, C18, C20, C21, C23, C24, C27, C28, C30, C31, C32, C33, C34,C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C54, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70
CAPACITOR, 10PF, 0805	AVX:08055A100KAT	3	C53, C55, C56
CAPACITOR, 330PF, 0805	AVX:08055A331KAT	2	C19, C25
CAPACITOR, 0.01UF, 0805	AVX:08055E103ZAT	2	C26, C29
CAPACITOR, 1.0UF, 1206	AVX:12063G105ZAT	2	C17, C22
CAPACITOR, 10UF, TAN, B-SIZE	AVX:TAJB107M016	7	C9, C10, C11, C12, C13, C14, C15
CAPACITOR, 47UF, TAN, D-SIZE	AVX:TAJC477M010	8	C1, C2, C3, C4, C5, C6, C7, C8
RESISTOR, 0 Ω, 0805	AVX:CR21-000	22	R8, R9, R10, R11, R16, R18, R32, R35, R36, R39, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52
RESISTOR, 150 Ω, 0805	AVX:CR21-151J	1	R40
RESISTOR, 510 Ω, 0805	AVX:CR21-511J	2	R3, R4
RESISTOR, 1 KΩ, 0805	AVX:CR21-102J	22	R12, R13, R14, R15, R17, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R33, R34, R37, R38
RESISTOR, 13.0 KΩ, 1%, 0805	AVX:CR21-1302F	2	R1, R6
RESISTOR, 22.1 KΩ, 1%, 0805	AVX:CR21-2212F	2	R2, R5
RESISTOR, 37.5 KΩ, 1%, 0805	AVX:CR21-3572F	1	R7
DIODE, SCHOTTKY, 30 V, 1.0 A, SMT	MOTOROLA:MBRS130LT3	2	D1, D2

Table 4. Supported Components (Part 2 of 2)

Component	Manufacturer Part Number	Quantity	Schematic Reference
LED, 4-DIODE_PACK, SMT	DIALIGHT:555-4003	1	LED1
INDUCTOR, 50 UH, 1.0 A	COILTRONICS:CTX50-2P	2	L1, L2
IC, PWM-VOLTAGE-REGULATOR, S08	MAXIM:MAX750ACSA	2	U1, U2
IC, RS232-INTERFACE, S024W	MAXIM:MAX208CWG	1	U10
IC, HEX-INVERTER, HCT, S014	TI:SN74HCT04D	1	U4
IC, QUAD3-STATE_BUF, HCT, S014	TI:SN74HCT125D	1	U6
IC, FLEX 10KE, 484/672-PIN_BGA	ALTERA	1	U5
IC, SERIAL_EPROM, PLCC20	ALTERA	1	U9
IC, ZERO-DELAY_BUFFER, S08	CYPRESS:CY2305-1H	2	U7, U8
SOCKET, 8-PIN_DIP	SAMTEC:ICO-308-SST	1	U3
SOCKET, 20-PIN, PLCC	SAMTEC:PLCC-020-F-N	1	Z2
CONNECTOR, DB-9, MALE	AMP:747250-4	1	JP5
CONNECTOR, 4-PIN, LOCK, RA	AMP:176153-4	1	JP2
SOCKET, 144-PIN, SO-DIMM, RA	AMP:390114-1	1	S1
CONNECTOR, PMC, RECEPTACLE	AMP:120521-1	4	Jn1, Jn2, Jn3, Jn4
CONNECTOR, SMB	AMP:414026-3	1	JP1
HEADER, 5 × 2-PIN, SHROUDED	SAMTEC:TST-105-07-S-D	2	JP3, JP4
SWITCH, DECADE, SMT	CTS:218-10LPST	1	S2

Board Options

Tables 5 through 7 show clock, SDRAM, and FLEX 10KE device options for the PCI development board.

Table 5. On-Board Oscillator Options

Options	Part Number	Description
User-defined clock device		Other frequency
Suggested clock device	EPSON SG-531PH-66.000MC	Suggested 66-MHz clock device

Table 6. SDRAM Options

Part Number	Configuration	Maximum Access Time (ns)	Maximum Operating Current (mA)
MT4LSDT464HG-662	4 Mbytes × 64	9	420
MT4LSDT864HG-662	8 Mbytes × 64	9	840

Table 7. FLEX 10KE Device Options

Part Number	Number of Pins	Package Type
EFP10K30EFC484-1	484	FineLine BGA™
EFP10K50EFC484-1	484	FineLine BGA
EFP10K50SFC484-1	484	FineLine BGA
EFP10K100EFC484-1	484	FineLine BGA
EFP10K130EFC484-1	484	FineLine BGA
EFP10K130EFC672-1	672	FineLine BGA
EFP10K200EFC672-1	672	FineLine BGA
EFP10K200SFC672-1	672	FineLine BGA

References

Refer to the following Altera documents for more information:

- *PCI Master/Target MegaCore Function with DMA Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)*
- *FLEX 10KE Embedded Programmable Logic Family Data Sheet*
- *MasterBlaster Serial/USB Communications Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*

Other references include:

- PCI-SIG. ***PCI Local Bus Specification, Revision 2.2***, Portland, Oregon: PCI Special Interest Group, December 1998.
- Micron Technology, inc. Small-Outline SDRAM Module MT4LSDT464H, MT4LSDT864H Data Sheet. **http://www.micron.com.**

Schematics

The following schematic foldouts are shown on sheets 1 through 9.

☞ `P5_IO[64:1]` signals on the schematics correspond to the I/O 1-64 on the board. `PROTO[23:21]` signals on the schematics correspond to the dedicated input 1-3 on the board.

Revision History

The information contained in the *FLEX 10KE PCI Development Board Data Sheet* version 1.01 supersedes information published in previous versions.

Version 1.01 Changes

- Updated information for `p4_io39` information in Table 2 on page 5.
- Updated no connect pins 484-pin packages in Table 2.

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