SignalTap Plus System Analyzer

June 2000, ver. 1 Data Sheet

Features

- Simultaneous internal programmable logic device (PLD) and external (board-level) logic analysis
- 32-channel external logic analyzer
  - 166 MHz maximum sample rate (synchronous and asynchronous)
  - 1M samples per channel
  - Four-level trigger sequence
  - Trigger on event count
  - Trigger on pattern duration
  - Selectable trigger time out
- SignalTap™ embedded logic analyzer
  - Up to 128 channels of internal (PLD) logic analysis
  - Up to 2k samples per channel
  - Non-intrusive probing of internal PLD nodes
  - Signals sampled synchronously to user-specified clock
  - No design file modifications required
  - Access via a Joint Test Action Group (JTAG) port
- Cross-triggering between internal and external analyzers
- Connects to PC via serial and USB ports
- Software support
  - Integrated into Quartus™ development environment
  - SignalTap Front Panel software provides stand-alone debugging capabilities

General Description

The Altera® SignalTap Plus system analyzer is a powerful system-level debugging tool that enhances the existing on-chip debugging capabilities of the SignalTap embedded logic analyzer by adding 32 channels of external logic analysis. The SignalTap Plus system analyzer simultaneously captures signals from internal PLD nodes and external, board-level nodes , showing them in a single, time-correlated display.

Functional Description

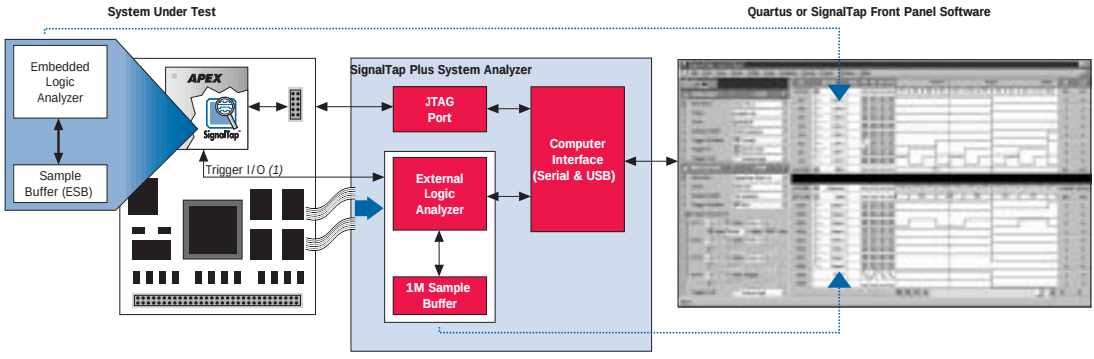
The SignalTap Plus system analyzer consists of a 32-channel, PC-hosted logic analyzer with an integrated JTAG port for PLD download and on-chip debugging via the SignalTap embedded logic analyzer. The 32 external logic analyzer channels have a 1M sample per channel acquisition buffer and can sample synchronously to a user-supplied clock, or from an internal time base, to a maximum frequency of 166 MHz.

The external analyzer provides a four-level trigger sequencer for specifying the trigger event. Each level in the sequence includes a trigger pattern with an event count and a duration filter that qualifies the trigger event. A selectable time out setting allows you to reset the trigger sequence or trigger the analyzer when a pattern does not occur within a specified period of time. A trigger output is provided to synchronize other test equipment, including the SignalTap embedded logic analyzer.

The SignalTap embedded logic analyzer provides access to signals from up to 128 internal nodes while the device is running in system at speed. Up to 2,048 samples per node are saved to internal embedded system blocks (ESBs) when the logic analyzer is triggered and streamed off-chip via the JTAG port. Optional Trigger Input and Trigger Output signals can be routed to spare I/O pins to synchronize the embedded logic analyzer with external equipment, and vice versa.

Support for the SignalTap Plus system analyzer is provided with the Quartus development environment version 2000.05 and higher. The system analyzer is also supported by the new stand-alone SignalTap Front Panel software and runs using the Windows 95, 98 and NT operating environments. Figure 1 shows the SignalTap Plus system analyzer architecture.

Figure 1. SignalTap Plus On-Chip & Off-Chip Debug Architecture



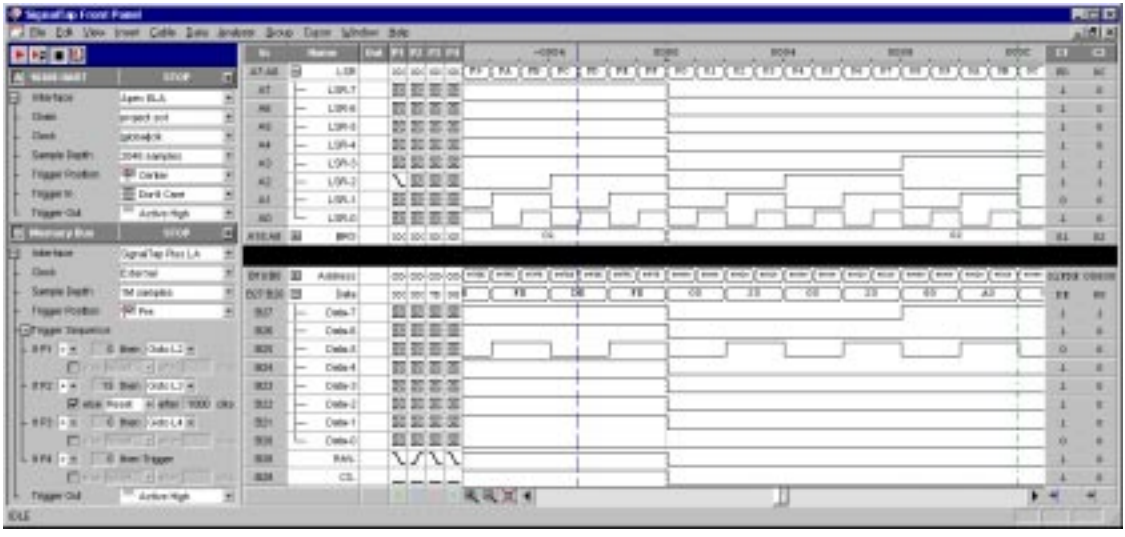
Note:
(1) Cross-trigger between internal and external analyzers.

SignalTap Front Panel Software

The SignalTap Front Panel software supports both the embedded and external logic analyzers. This new software is integrated into the Quartus development software version 2000.05 and higher to provide a complete development and debugging environment. The Front Panel software also runs as a stand-alone program under the Windows 95, 98 and NT operating environments for applications in which device design facilities are not required.

The Front Panel software provides analyzer control and data display for both internal and external logic analyzers. Trigger conditions, sample depth, and sample rates settings can be made for each analyzer. Acquired data can be time-correlated to a common clock or a common trigger point. Patterns can be used to trigger the logic analyzers and locate and/or highlight specific digital patterns in the acquired data. Figure 2 shows a typical SignalTap Front Panel software display.

Figure 2. SignalTap Front Panel Software

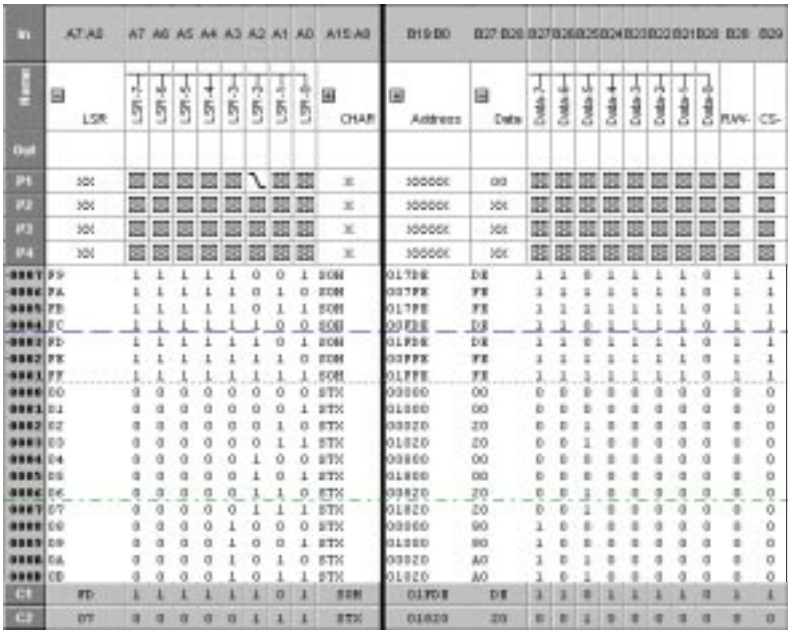


Once acquired, data can be viewed as waveforms or in a tabular list display. The tabular display list is ideal for processor trace or communications packet analysis. Signals can be grouped together as a bus and later expanded to show data for individual signals. One of several radixes may be used, including:

- Binary
- Decimal (signed and unsigned)
- Hexadecimal
- ASCII
- Analog (signed and unsigned)

Figure 3 shows a tabular display for the Front Panel software.

Figure 3. Tabular Display



SignalTap Embedded Logic Analyzer Megafunction

The SignalTap embedded logic analyzer megafunction, included in the Quartus development software, provides access to signals from nodes inside the APEX device. The logic analyzer is optimized to be small and fast, and have little or no impact on the device design. The Quartus software automatically creates the logic analyzer when internal nodes are selected for acquisition. The software does not require design file modifications.

The embedded logic analyzer captures internal signals and saves the acquired data to internal RAM. When the acquisition buffer is full, the contents are streamed off-chip via the JTAG port and uploaded through the SignalTap Plus system analyzer JTAG cable. The embedded logic analyzer is created and configured within the Quartus software. Design download capabilities, logic analyzer trigger settings, run control, and captured data display are provided within the Quartus software and the SignalTap Front Panel software.

For more information on the SignalTap embedded logic analyzer, see the *SignalTap Embedded Logic Analyzer Megafunction Data Sheet*.

SignalTap Plus External Logic Analyzer

The external logic analyzer provides acquisition for up to 32 signals at speeds of up to 166 MHz and sample depth of up to 1M samples per channel. The external logic analyzer supports multi-level triggering, allowing you to trigger the analyzer based on a sequence of up to four patterns, with event count, pattern duration, and trigger time out qualifiers for each pattern.

Acquisition Buffer

The SignalTap Plus system analyzer provides a 1M sample per channel acquisition buffer for storing data captured by the 32 external logic analysis channels. The designer can specify the amount of acquisition buffer to use based on specific needs. The sample depth choices are 4k, 8k, 16k, 32k, 64k, 128k, 256k, 512k, and 1 M samples.

Acquisition Clock

The external logic analyzer synchronously samples with the rising edge of a user-provided clock signal at a frequency of up to 166 MHz, using the External Clock input. An internal clock reference is also provided for asynchronous signal acquisition with selectable sample rates in 1–2– 5 intervals between 1 kHz to 166 MHz. The asynchronous sample rate choices are 1 kHz, 2 kHz, 5 kHz, 10 kHz, 20 kHz, 50 kHz, 100 kHz, 200 kHz, 500 kHz, 1 MHz, 2 MHz, 5 MHz, 10 MHz, 20 MHz, 50 MHz, 100 MHz, and 166 MHz.

Triggering

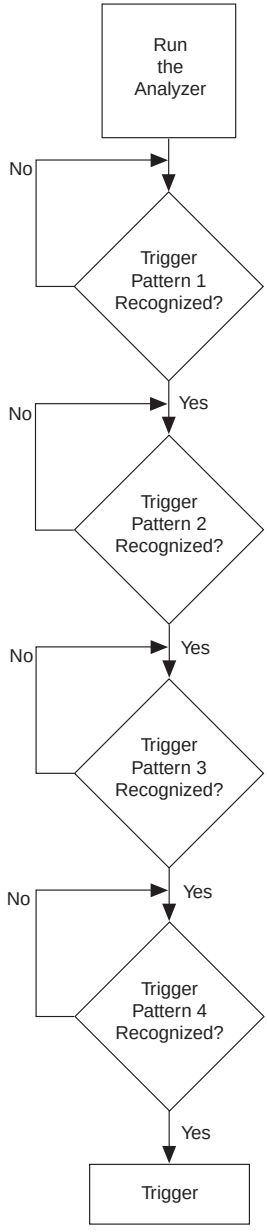
The external analyzer provides complex triggering by using a multiple pattern trigger sequencer with built-in qualifiers for pattern occurrence and duration.

Trigger Sequence

One to four trigger patterns can be combined in a trigger sequence, allowing you to specify a series of patterns to be recognized before the analyzer triggers. Each trigger pattern consists of logic conditions (i.e., high, low, rising edge, falling edge, either edge, and don't care) across all 32 input channels. Transitioning from one level in a trigger sequence to the next is instantaneous, allowing the new trigger pattern to be evaluated on the very next clock.

Figure 4 shows the trigger sequence flow when the analyzer is set to trigger on a sequence of four patterns.

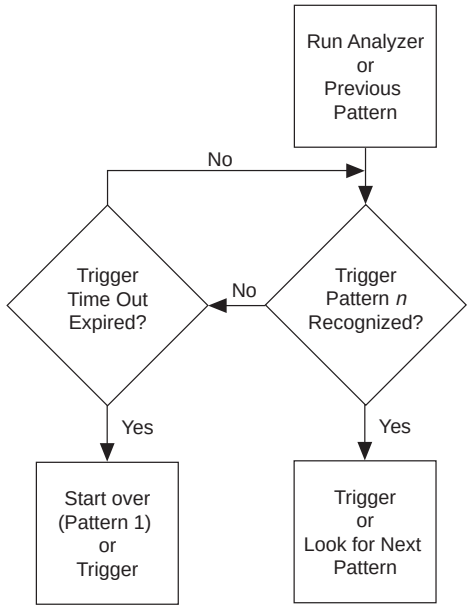
Figure 4. Trigger Sequence Flow



Trigger Time Out

The trigger time out gives you the ability to trigger the external analyzer or restart the trigger sequence from the beginning, when a trigger pattern fails to occur within a specific period of time. The time out can be set to any number between 1 and 16 M clock cycles. See Figure 5.

Figure 5. Trigger Time Out Flow



In Figure 6, the second pattern (P2) is defined as a rising edge on R/W- while CS is low. If the pattern fails to occur before 1,000 clocks, the sequence is reset to the beginning.

Trigger Output

A dedicated trigger output signal can output a positive or negative pulse when the logic analyzer triggers. This signal allows you to synchronize external test equipment to the SignalTap Plus logic analyzer.

Trigger Sequence Example

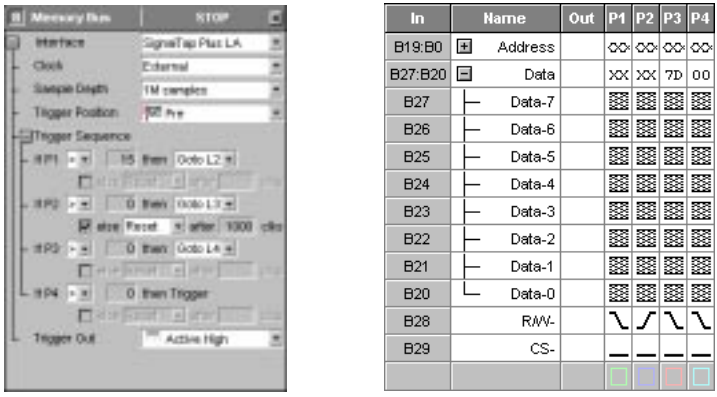
The first trigger level is satisfied when Pattern 1 (P1 falling edge on R/W- while CS is low) occurs 16 times. The sequence then advances to the next level and waits for Pattern 2. If Pattern 2 does not occur before 1000 clock cycles, the sequence is reset and starts over at the first level (P1).

Once Pattern 2 is detected, the trigger logic looks for Pattern 3 (a falling edge on R/W- while CS is low and DATA equals 7D).

Once Pattern 3 is detected, the trigger logic looks for Pattern 4 (a falling edge on R/W- while CS is low, and DATA equals 00). When this occurs, the analyzer triggers, and a positive pulse is generated on the Trigger Out wire.

Figure 6 shows a trigger sequence example.

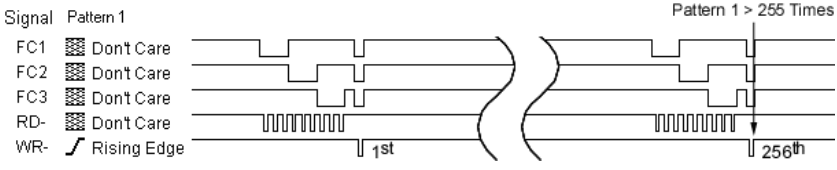
Figure 6. Trigger Sequence Example



Event Count

Patterns that contain an edge condition (i.e., rising, falling, or either edge) are counted, and the analyzer can be triggered when the count exceeds a specified value. By default, the event count is zero. A maximum of 1,023 pattern occurrences may be counted for each level in the trigger sequence. In Figure 7, Pattern 1 must occur 256 times before the trigger condition is met. Pattern 1 consists of a rising edge on WR-; the other signals are ignored.

Figure 7. Event Count

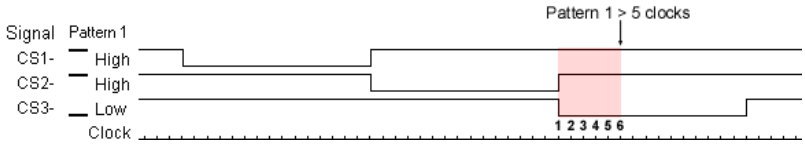


Pattern Duration

Patterns that do not contain edge conditions can be evaluated based on duration. Pattern duration values are evaluated based on *greater than* or *less than* conditions with a maximum duration of 1,023 clock cycles. By default, the pattern duration is *greater than 0*.

In Figure 8, Pattern 1 must last for greater than five clock cycles before a trigger condition is met.

Figure 8. Pattern Duration



SignalTap Plus Hardware Connections

The SignalTap Plus system analyzer connects to board-level signals using two probe cable assemblies that mate with Pod 0 and Pod 1 connectors. A JTAG port provides access to the PLD for device configuration and interface to the SignalTap embedded logic analyzer. A host PC connects to the SignalTap Plus system analyzer by using a serial or USB interface. An external adapter is included to provide power.

The SignalTap Plus system analyzer includes two interchangeable probe cable assemblies, Pod 0 and Pod 1, which connect the external logic analyzer to signals from the system under test. Each wire in the cable assembly is color coded and contains a termination resistor. The cables can be used with standard IC test clips, adapters or header pins.

The analyzer interprets captured data as logic 1 or 0, depending on whether or not the voltage exceeds a specified threshold. The threshold for all 32 channels can be manually set to 5.0 V, 3.3 V, 2.5 V, 1.8 V or to track the voltage applied to the VIO input (pin 1) of either probe cable assembly. See Figure 9.

Figure 9. SignalTap Plus System Analyzer Connections

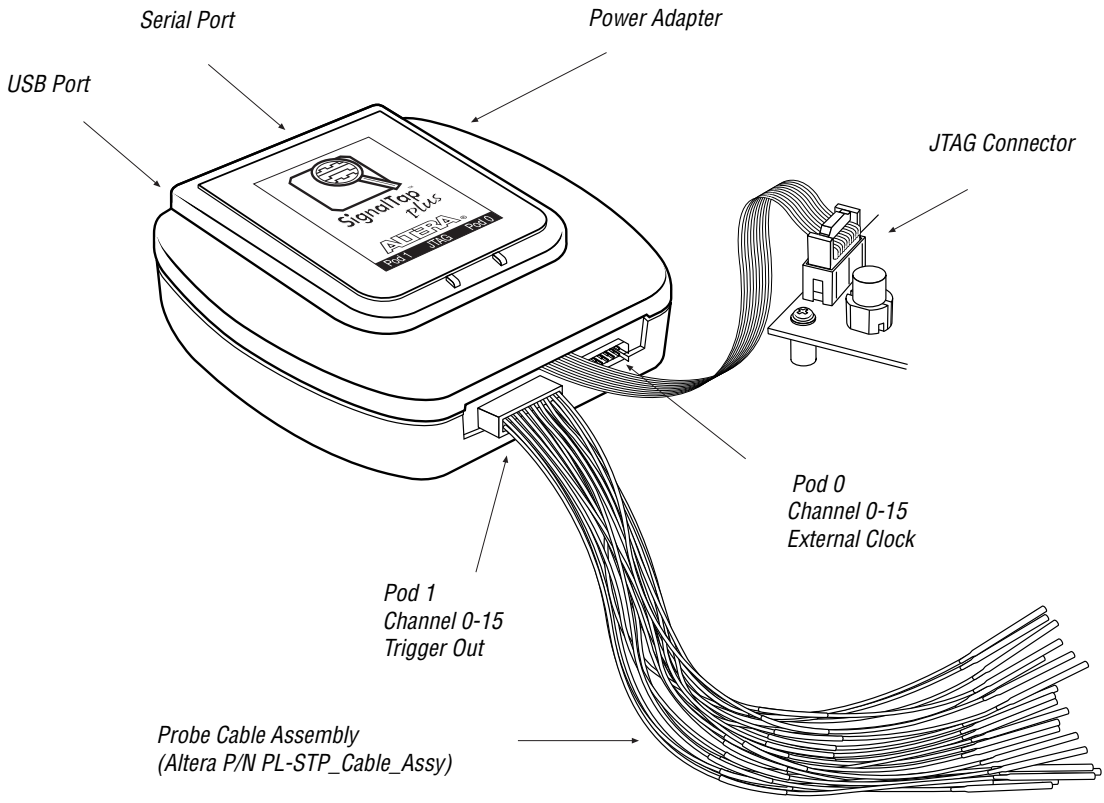


Table 1 shows the pin connections for the SignalTap Plus probe cable assembly.

Table 1. SignalTap Plus Probe Cable Assembly (Part 1 of 2)

Pin	Wire Label	Wire Color	Description
1	VIO	Red	Reference voltage for analyzer input threshold
2	GND	Black	Signal ground
3	CH0	Black	Channel 0
4	CH1	Brown	Channel 1
5	CH2	Red	Channel 2
6	CH3	Orange	Channel 3
7	CH4	Yellow	Channel 4
8	CH5	Green	Channel 5

Table 1. SignalTap Plus Probe Cable Assembly (Part 2 of 2)

Pin	Wire Label	Wire Color	Description
9	CH6	Blue	Channel 6
10	CH7	Violet	Channel 7
11	CH8	Grey	Channel 8
12	CH9	White	Channel 9
13	CH10	Black	Channel 10
14	CH11	Brown	Channel 11
15	CH12	Red	Channel 12
16	CH13	Orange	Channel 13
17	CH14	Yellow	Channel 14
18	CH15	Green	Channel 15
19	GND	Black	Signal ground
20	CLK/TRIG OUT	White	Clock signal (Pod 0) Trigger output signal (Pod 1)

Download Modes

The SignalTap Plus system analyzer provides two modes for device download; passive serial (PS) and JTAG modes. Passive serial (PS) mode is used for configuring APEX 20K and FLEX™ devices. JTAG mode uses the industry-standard IEEE Std. 1149.1 JTAG interface for programming serial configuration devices (i.e., EPC2) in-system or for configuring APEX 20K and FLEX devices.

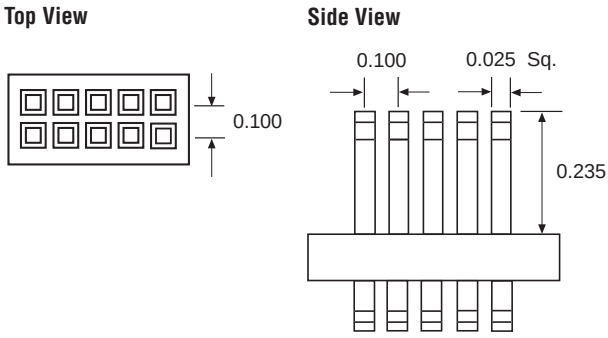
Table 2 shows the 10-pin female plug's pin names for the corresponding download mode.

Table 2. SignalTap Plus Female Plug's Pin Names & Download Modes

Pin	PS Mode		JTAG Mode	
	Signal Name	Description	Signal Name	Description
1	DCLK	Clock signal	TCK	Clock signal
2	GND	Signal ground	GND	Signal ground
3	CONF_DONE	Configuration control	TDO	Data from device
4	VCC	Power supply	VCC	Power supply
5	nCONFIG	Configuration control	TMS	JTAG state machine control
6	VIO	Reference voltage for SignalTap output driver	VIO	Reference voltage for SignalTap output driver
7	nSTATUS	Configuration status	–	No connect
8	–	No connect	–	No connect
9	DATA0	Data to device	TDI	Data to device
10	GND	Signal ground	GND	Signal ground

The SignalTap Plus system analyzer 10-pin female plug connects to a 10-pin male header on the circuit board. The 10-pin male header has two rows of five pins, which are connected to the device's programming or configuration pins. Figure 10 shows the dimensions of a typical 10-pin male header.

Figure 10. 10-Pin Male Header Dimensions



The SignalTap Plus system analyzer connects to a host computer through a serial or USB port. A 9-pin female D-type connector connects to a standard serial cable included with SignalTap Plus system analyzer. Table 3 shows the 9-pin serial header.

Table 3. SignalTap Plus 9-Pin Serial D-Type Connector Pin-Outs

Pin	Signal Name	Description
2	rx	Receive data
3	tx	Transmit data
4	dtr	Data terminal ready
5	GND	Signal ground
6	dsr	Data set ready
7	rts	Request to send
8	cts	Clear to send

The USB connector can be used with any standard USB cable.

For more information on 9-pin versus 25-pin serial connectors, search for "9-pin or 25-pin serial connectors" in the Altera technical support (Atlas®) database at **http://www.altera.com**.

Powering the SignalTap Plus System Analyzer

The SignalTap Plus system analyzer requires 9 volts DC at 660 mA for proper operation. An AC adapter is included and operates with line voltage from 100 VAC to 240 VAC and line frequencies from 50 to 60 Hz. The SignalTap Plus system analyzer can not be powered from the target system or the USB cable.

Specifications

Tables 4 through 10 list the SignalTap Plus system analyzer specifications.

Table 4. Asynchronous Sampling

Specification	Value
Maximum sample rate	166 MHz
Sample period accuracy	± 0.01%
Channel-to-channel skew	1.0 ns max

Table 5. Synchronous Sampling

Specification	Value
Maximum sample rate	166 MHz
Setup & hold	0.6 / 0.0 ns
Minimum state clock pulse width	3.0 ns

Table 6. Triggering

Specification	Value
Sequencer speed	166 MHz
Sequence levels	4
Trigger output delay	33 clocks

Table 7. Probes

Specification	Value
Input impedance	200 k, 15 pF
Minimum input voltage swing	1.44 V peak-to-peak
Threshold range	1.8 V, 2.5 V, 3.3 V, 5.0 V, variable (VIO input)
Threshold accuracy	± 60 mV
Maximum input voltage	– 0.5 V to +7.0 V

Table 8. JTAG Port

Specification	Value
Input impedance	200 k, 15 pF
Minimum input voltage swing	1.44 V peak-to-peak
Threshold range	1.8 V, 2.5 V, 3.3 V, 5.0 V, variable (VIO input)
Threshold accuracy	± 60 mV
Maximum input voltage	– 0.5 V to +7.0 V

Table 9. PC Interface

Specification	Value
RS-232	19.2 k baud to 115.2 k baud, Female 9-pin D connector
USB	Up to 12 Mbits per second

Table 10. Operating Environment

Specification	Value
Power Adapter	100 to 120 VAC, 50 to 60 Hz
Temperature	0˚C to 40˚C
Humidity	Up to 80% relative humidity (non-condensing)

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