Quartus
Programmable Logic Development System & Software

May 1999, ver. 1.01 Data Sheet

Introduction

As device densities increase, design methodologies for programmable logic devices (PLDs) must continue to evolve. The Quartus™ software, Altera's fourth-generation development system for programmable logic, allows designers to process million-gate designs with advancements never before seen in PLD development tools. With the Quartus software, Altera continues its commitment to provide development software with unmatched flexibility and performance.

The Quartus software offers state-of-the-art features—such as multi-processor support and incremental recompilation—to shorten design cycles. To streamline the development flow and increase productivity, the Quartus software supports system-level solutions with block-level editing, workgroup computing, and expanded support for megafunctions. A new embedded logic analysis feature allows engineers to verify chip functionality and timing by observing internal and I/O signal values at system clock speeds.

The Quartus software also interfaces seamlessly with other EDA software tools, allowing designers to use the tools they are already familiar with to design for Altera devices. As the industry's first "Internet-aware" development tool, the Quartus software provides up-to-the-minute information and file exchanges, including software updates, license files, and support services across the Internet. Altera effectively becomes a member of the design team by providing an unmatched level of technical support. Together, these features make the Quartus software the ideal platform for million-gate designs.

The Quartus development system includes the following features:

- *Advanced Tool Integration*—Altera works closely with EDA partners to develop a truly seamless interface between the Quartus software and major EDA tools. The resulting NativeLink™ integration enables users to launch and control the Quartus software from other EDA tools, minimizing the need to learn a new design tool. More importantly, parameters can be passed efficiently between EDA tools and the Quartus software, enabling designers to effectively debug their designs in the EDA tool. The Quartus software also provides traditional interfaces through EDIF 2 0 0 and 3 0 0, library of parameterized modules (LPM) 2.2.0, standard delay format (SDF) 1.0 and 2.0, VITAL 95, Verilog HDL, and VHDL 1987 and 1993.

- *Workgroup Computing*—Multiple designers can work on a single project using global file management and design revision control.
- *Integrated Logic Analysis Functionality*—The built-in SignalTap™ logic analyzer solution offers system-level verification of devices running at speed, which significantly reduces verification times.
- *Incremental Recompilation*—The nSTEP™ Compiler only compiles the portions of the design that have changed, offering huge savings in compilation time.
- *Advanced Synthesis*—The CoreSyn™ feature provides advanced synthesis by determining optimal mapping of a design to a device architecture.
- *Multiple Platforms*—The Quartus software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.
- *Full Integration*—The Quartus software's design entry, processing, and verification features offer the most integrated suite of programmable logic development tools available, allowing faster debugging and shorter development cycles.
- *Modular Tools*—Designers can customize their development environment by choosing from a variety of design entry, compilation, verification, and device programming options, all of which are described in this data sheet.
- *Hardware Description Languages (HDLs)*—The Quartus software supports a variety of HDL design entry options, including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL).
- *Internet-Enabled Support*—The Quartus software's direct connection to the Altera web site provides immediate access to the latest solutions and software updates. Designers can also submit service requests directly to Altera Applications and monitor the progress on-line.
- *MegaCore™ Functions*—MegaCore functions are pre-verified HDL netlist files for complex system-level functions and are optimized for Altera device architectures. Altera-created MegaCore functions simplify the design task by eliminating the need to design logic cores. With MegaCore functions, only the glue logic surrounding the core needs to be designed, thus freeing the designer to focus more time and energy on improving and differentiating the design and final product.

- *OpenCore™ Feature*—The Quartus software supports the OpenCore feature, which allows designers to evaluate megafunctions prior to licensing.

Quartus Design Process

The Quartus design process consists of four phases: design entry, design compilation, design verification, and device programming.

Design Entry

The Quartus software can integrate multiple design files—generated with the Quartus software or other industry-standard EDA design entry tools—into a single design hierarchy. The extensive integration between Quartus applications allows information to flow freely. For example, errors identified during compilation, simulation, and timing analysis can be located automatically and highlighted in the original design file or in the Floorplan Editor. If a design consists of two or more hierarchy levels, the user can navigate from one design entity to any other entity, regardless of whether it is schematic-based or text-based.

Megafunctions

Altera MegaCore functions support applications such as peripheral component interconnect (PCI), bus interface, digital signal processing (DSP), and communications applications. These functions can be instantiated into designs and simulated with the Quartus development system or any Altera-supported EDA tool. For Quartus design flows, designers simply instantiate the function in the design file. For design flows that use other EDA tools, designers can instantiate MegaCore functions by specifying the function and port names in the HDL design file. During design processing, the EDA tool includes the function in an EDIF netlist file. The Quartus software compiles the resulting EDIF netlist file for the desired Altera device architecture.

Altera Megafunction Partners Program (AMPP℠) partners also provide a wide variety of megafunctions. Like Altera, AMPP partners develop megafunctions that are optimized for Altera devices and can facilitate high-density design. The AMPP program currently offers over 75 megafunctions that serve a broad range of processor, DSP, communications, bus interface, and other applications.

The Quartus software will expand its support for megafunctions by enabling instance-specific assignments and greater control over synthesis. With this control, customers can maintain assignments for each instance of a MegaCore or AMPP function.

For more information on Altera MegaCore and AMPP megafunctions, see the ***AMPP Catalog*** or go to the Altera web site at **http://www.altera.com**.

OpenCore Feature

MegaCore and AMPP megafunctions can be previewed before licensing via the Quartus OpenCore feature. This pre-purchase evaluation feature allows designers to instantiate, compile, and simulate designs to verify a function's size and performance before making a licensing decision. However, programming files and output files for third-party EDA tool simulation can only be generated with a license file provided upon purchase.

MegaCore functions can be downloaded for OpenCore evaluation from the Altera web site.

Industry-Standard LPM Functions

Users can create designs using functions from the industry-standard LPM version 2.2.0. The LPM offers scalable logic functions—such as RAM, counters, adders, and multiplexers—and preserves high-level design information for optimal implementation. The Quartus Compiler automatically generates optimized, architecture-specific implementations of LPM functions. LPM functions can be implemented with industry-standard design entry tools, or in schematic and text designs created with the Quartus software.

For more information on LPM functions, refer to the ***LPM Quick Reference Guide***, Quartus Help, the Altera web site, or the EDIF web site at **http://www.edif.org**.

Industry-Standard EDA Design Entry

The Quartus Compiler interfaces with industry-standard EDA tools that generate EDIF 2 0 0 and 3 0 0 netlist files, including files that contain LPM functions. The Quartus Compiler uses Library Mapping Files (**.lmf**) to map symbol and pin names from other EDA tools to Quartus logic functions. Altera supports the use of LMFs with tools from companies such as Cadence, Exemplar Logic, Mentor Graphics, Synopsys, Synplicity, and Viewlogic. VHDL 1987 and 1993 and Verilog HDL design support is also available from Cadence, Exemplar Logic, Mentor Graphics, Synopsys, Synplicity, Viewlogic, and others. True WYSIWYG design support is offered with the new ATOM Netlist, which maps directly to the target device architecture.

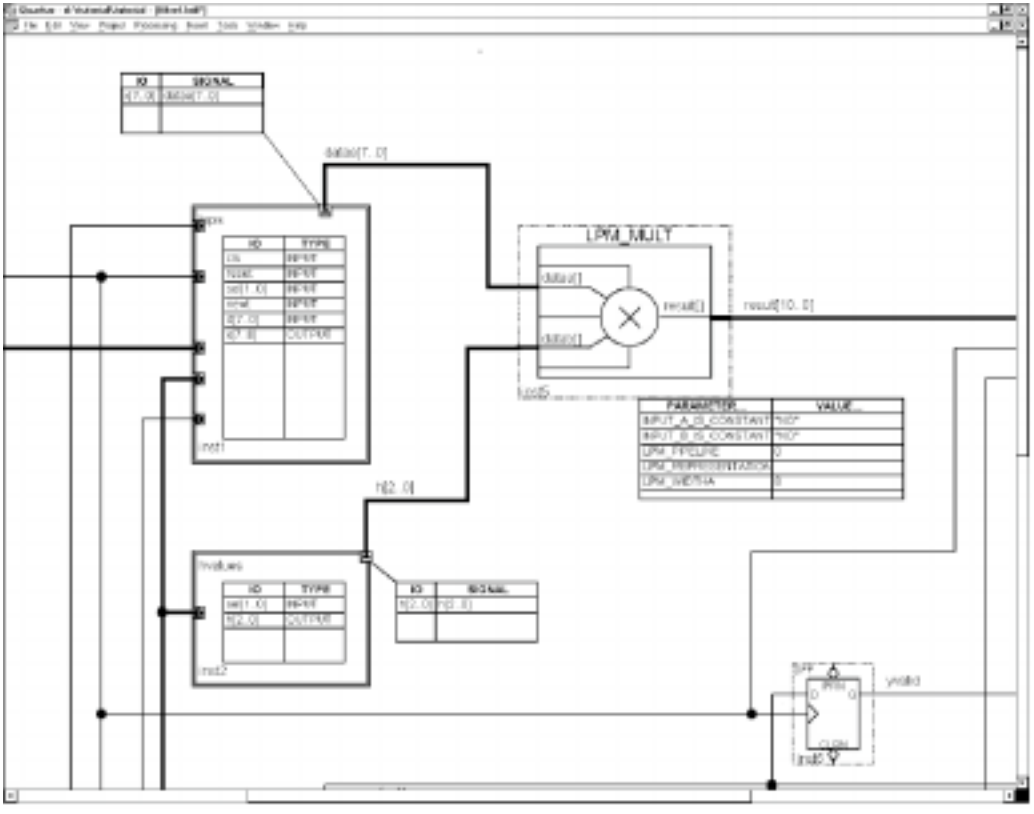
For more information on other EDA tool vendors, see *EDA Software Support*.

Graphic Design Entry

The Quartus Block Editor (shown in Figure 1) makes graphic design entry fast and easy. The Block Editor allows designers to create and edit a Block Design File (**.bdf**) that includes a combination of block diagrams, megafunctions, macrofunctions, and primitive symbols. The Quartus software provides over 300 logic functions, including LPM and custom functions.

The Quartus software allows designers to create a symbol or block diagram for any design file automatically. With the Block Editor, the designer can modify a symbol to customize its appearance, or create an entirely new symbol. The Block Editor also aids in top-down design entry by creating functional blocks of a design at an early stage of development. Designers can use these functional blocks to represent lower-level portions of a design. These blocks can be connected rapidly with conduits that connect common signals between blocks.

Figure 1. Quartus Block Editor



Hardware Description Language Entry

The Quartus Text Editor is ideal for entering and editing HDL design files written in VHDL 1987 and 1993, Verilog HDL, or AHDL. The Quartus Compiler can synthesize logic from any of these languages and map the logic to the Altera APEX™ architecture.

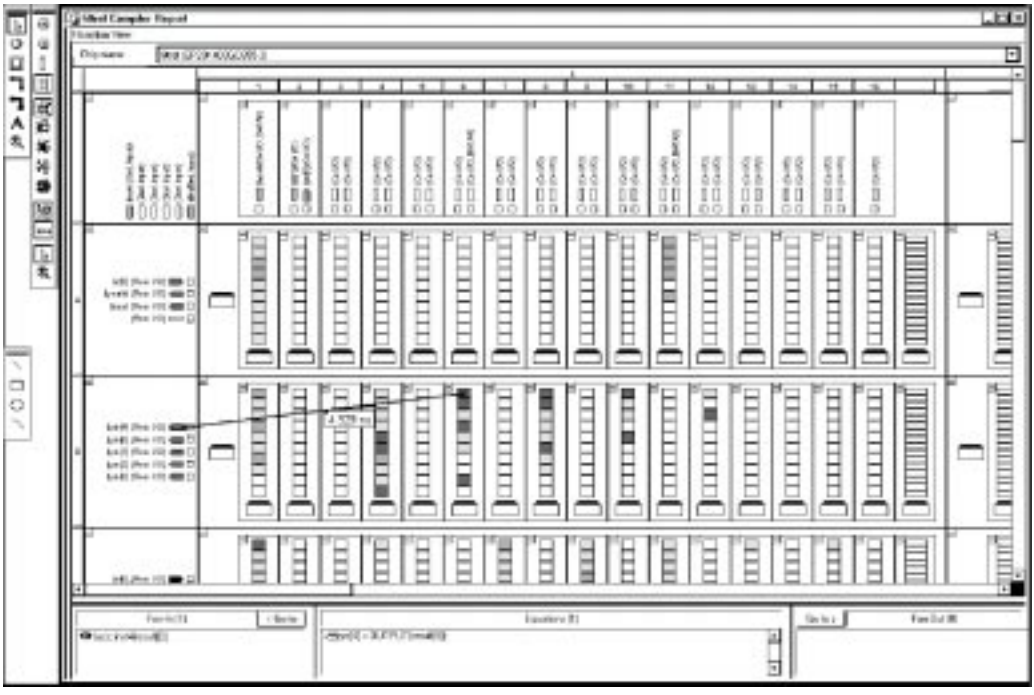
HDLs can implement state machines, truth tables, conditional logic, Boolean equations, and arithmetic operations—including addition, subtraction, equality, and magnitude comparison. The Quartus software also supports LPM functions entered in HDLs. Together, these features make it easy to implement complex projects in a concise, high-level description.

Floorplan Editing

The Quartus Floorplan Editor (shown in Figure 2) simplifies the process of assigning logic to device pins and logic cells. A graphical image of each device used in a compilation allows easy logic placement. Both high-level and detailed device views are available. The designer can assign pins and logic cells before compiling a design and also view and modify the results after compilation.

Floorplan Editor features allow the designer to view all assigned and unassigned logic in a device. The Floorplan Editor provides a color-coded view of all logic resources in the device, as well as user assignments, fan-in and fan-out information, and architecture-specific features. Any node or pin can be dragged to a new location. Logic can be assigned to specific pins and logic cells, or to more general regions within a device.

Figure 2. Quartus Floorplan Editor

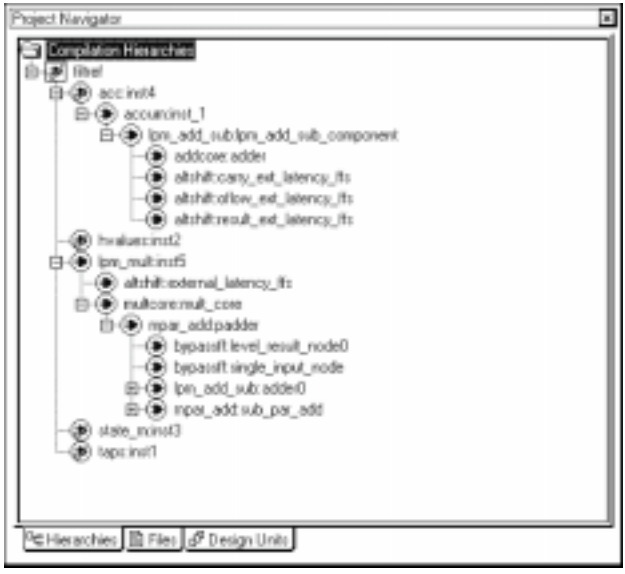


Project Navigator

The Quartus Project Navigator offers a centralized, object-oriented design database and global file management system that allows several computers to access the same project across a network without interrupting the design cycle. The revision control feature prevents more than one designer from working on any particular section of a project concurrently. The Quartus software integrates with standard external source control software to manage each design revision.

The Quartus Project Navigator also allows designers to view the hierarchy of compilation and simulation settings. Designers can traverse the hierarchy easily, automatically opening the appropriate editor for each design entity. The Quartus software's ability to support multiple levels of hierarchy in a single design allows customers to use the design entry method best suited for each portion of the design. See Figure 3.

Figure 3. Quartus Project Navigator



Design Compilation

The Quartus Compiler processes designs and outputs files for programming, simulation, and timing analysis. The Quartus nSTEP Compiler allows designers to make changes and obtain results without running a full compilation; the software only compiles the portions of a design that have changed. This powerful feature significantly shortens compile times and maintains placement and timing in portions of the design that are unchanged.

Message Window

The Quartus Message Window communicates with all Quartus applications, reporting errors, displaying information, and showing warning messages for design problems such as connection and syntax errors, as well as simulation, timing analysis, and programming information. Designers can use the Message Window to open the design file that contains the error and highlight its location automatically. The Message Window can locate errors for the current project in the Quartus software's Floorplan Editor, Text Editor, and Block Editor, or in a third-party EDA tool.

Logic Synthesis & Fitting

The Logic Synthesizer module in the Quartus Compiler supports numerous synthesis options. It selects appropriate logic reduction algorithms to minimize and remove redundant and unused logic, ensuring that the device logic resources are used as efficiently as possible for the target device architecture.

The nSTEP Compiler includes a new CoreSyn synthesis capability. The Compiler analyzes the design and then partitions functions into look-up tables, product-terms, or embedded memory logic blocks within the APEX architecture. Using the CoreSyn capability, the nSTEP Compiler invokes the appropriate synthesis technology to optimize the logic for that architecture.

The Compiler's Fitter module applies heuristic rules to select the best possible implementation for the synthesized project in one or more devices. This automatic fitting relieves the designer of tedious place-and-route tasks. The Fitter generates a report showing project implementation as well as any unused resources in the device(s). Fitting results can also be displayed in the Report Window's Floorplan Viewer.

Timing-Driven Compilation

The Compiler can implement user-specified timing requirements for propagation delays (t_{PD}), clock-to-output delays (t_{CO}), setup times (t_{SU}), internal clock frequency (f_{MAX}), and system clock frequency. Designers can specify timing requirements on selected logic functions and for a project as a whole. The Report Window and Compiler messages provide detailed information on how the timing requirements have been implemented in the project.

Industry-Standard Simulation Formats

The Quartus Compiler can create netlist files for use in a variety of simulation environments. These netlist files contain post-synthesis functional and timing information that can be used with standard design verification tools for device-level or board-level simulation.

The following interfaces are available:

- *Verilog HDL*—Creates Verilog HDL netlist files that can be used with Verilog HDL simulators.
- *VHDL*—Creates VHDL 1987 and 1993 netlist files that can be used with VHDL simulators.

For each interface, the Compiler generates a version 1.0 or 2.1 Standard Delay Output Format File (**.sdo**) that includes timing information for simulators that require timing and functional information in separate files.

Programming File Generation

Both the Quartus Compiler and Programmer can generate programming and configuration files. The following file formats are available in the Quartus software:

- Programmer Object File (**.pof**)
- SRAM Object File (**.sof**)
- Hexadecimal (Intel-format) File (**.hex**)
- Raw Binary File (**.rbf**)

For more information on programming and configuring devices with these file formats, go to Quartus Help.

Design Verification

The Quartus software offers design verification capabilities—including design simulation and timing analysis—that test the logical operation and internal timing of a design. Design verification tools for Altera devices are also available from a variety of EDA vendors.

Simulation

The Quartus Simulator provides flexibility and control for modeling single- or multi-device projects. The Simulator extracts information from the design database during compilation to perform functional, timing, or multi-device simulation for a project.

The designer either defines input stimuli with a straightforward vector input language or draws waveforms directly with the Quartus Waveform Editor. Simulation results can be viewed in the Waveform Editor or Text Editor and printed as waveform or text files.

The designer specifies commands either interactively or in a text-based Tcl/Tk file to perform a variety of tasks, such as monitoring the project for glitches and register setup and hold time violations; halting the simulation when user-defined conditions are met; forcing flipflops high or low; performing functional testing; and defining the initial memory content of RAM or ROM blocks. If a setup time, hold time, or minimum pulse width is violated, the Message Window reports the problem. The designer can then use the Message Window to locate the time at which the problem occurred as well as locate the error in the original design file.

For easy comparison, the designer can superimpose the results of two simulations in the Waveform Editor.

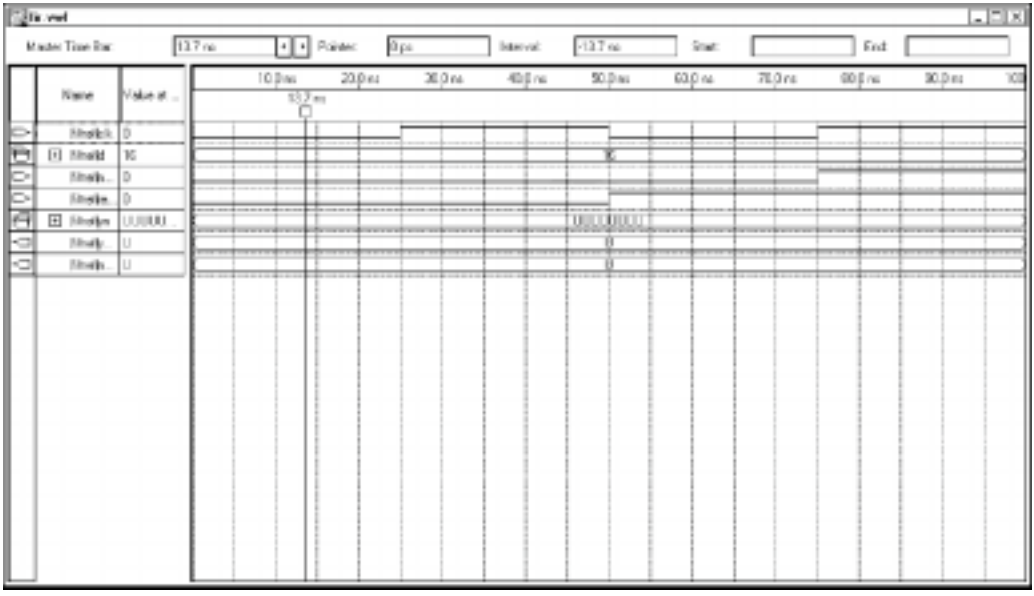
Functional Simulation

The Quartus Simulator supports functional simulation to test the logical operation of a project after it is synthesized and before it is placed and routed, thereby allowing the designer to quickly identify and correct logical errors. The Quartus Waveform Editor displays the results of functional simulation and provides easy access to all nodes in the project, including combinatorial functions.

Timing Simulation

In a timing simulation, the Quartus Simulator tests the project after it has been fully synthesized and optimized. Figure 4 shows the Waveform Editor.

Figure 4. Quartus Waveform Editor



Multi-Device Testbenches

The Quartus software can combine the timing and/or functional information from multiple Altera devices, allowing the designer to simulate several devices operating together. Designers can also perform multi-device simulation using testbenches.

Timing Analysis

The Quartus Timing Analyzer can calculate a matrix of point-to-point device delays, determine system clock frequency time requirements at device pins, and calculate maximum clock frequency. In addition, the Timing Analyzer can perform multiple clock analysis and multi-cycle timing analysis.

Quartus design entry tools are integrated with the Timing Analyzer, allowing designers to simply mark start and end points in the design or the Floorplan Editor to determine the shortest and longest propagation delays. The Message Window can also locate and display critical paths identified by the Timing Analyzer in the source design files or in the Floorplan Editor.

Embedded Logic Analyzer

The Altera SignalTap logic analyzer solution allows engineers to verify chip functionality and timing by observing internal and I/O signal values at system clock speeds. This solution—which includes the SignalTap embedded megafunction, the Quartus software, and the MasterBlaster™ communications cable—further enhances the verification and debugging process by taking advantage of the reprogrammability benefits offered by PLDs. Design edits can be quickly implemented in silicon to enable efficient debugging and verification of system enhancements, without the risks typically associated with silicon changes.

With the SignalTap logic analysis solution, the Quartus software automatically inserts a logic analyzer megafunction—which is provided with every configuration of the Quartus software—into the APEX 20K device. The SignalTap megafunction allows designers to easily capture and analyze both internal signals and signals at the device pins. The signal information is stored in the APEX embedded system blocks (ESBs) and then uploaded via the MasterBlaster communications cable to the Quartus Waveform Viewer for easy debugging, verification, and analysis. The ESBs together with the SignalTap megafunction enable device verification at full system clock speeds.

For more information on Altera's SignalTap megafunction, see the *SignalTap Embedded Logic Analyzer Megafunction Data Sheet*.

Device Programming

The Quartus Programmer is used to program or configure Altera devices. The Programmer allows the designer to program, configure, verify, examine, blank-check, and functionally test devices.

Altera provides the MasterBlaster cable and ByteBlasterMV™ parallel port download cable for device programming and configuration. The MasterBlaster cable connects to an RS-232 serial port or universal serial bus (USB) port, and the ByteBlasterMV download cable connects to a PC parallel port to provide configuration/programming data. With these cables, designers can also configure or program multiple devices using the multi-device JTAG chain mode in the Quartus Programmer.

Altera provides all hardware and software necessary for programming and verifying devices, including a Logic Programmer Card, Master Programming Unit (MPU), and programming adapters. The add-on Logic Programmer card (for PCs or compatible computers) drives the MPU. The MPU performs continuity checking to ensure adequate electrical contact between the programming adapter and the device. With the appropriate programming adapter, the MPU also supports functional testing. Vectors created for simulation can be applied to a programmed device to verify its functionality.

For more information on the MasterBlaster and ByteBlasterMV cables, programming hardware, and software, refer to the following sources:

- *MasterBlaster Serial/USB Communications Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Altera Programming Hardware Data Sheet*
- *Programming Hardware Manufacturers*

On-Line Help

On-line help provides access to all information about the Quartus software, including complete, up-to-date documentation on all Quartus applications. This on-line help extends to Altera-provided megafunctions and macrofunctions; causes and suggested actions for messages; references to related Altera documentation; text file formats (e.g., AHDL); and information on Altera devices and programming hardware.

On-line help is only a keystroke or mouse click away. The F1 key provides instant access to information on a dialog box, highlighted menu command, or pop-up message. Typing Shift+F1 or choosing the context-sensitive help button on the toolbar allows designers to click on any item on the screen—including logic function symbols or names and text file keywords—for context-sensitive help on that item.

Internet Access

The Quartus software is "web-aware," with the Microsoft Internet Explorer browser technology built in. From within the software, designers have direct access over the Internet to the Altera Technical Support (Atlas℠) Solutions database to find immediate solutions to issues encountered during the design cycle.

While in the Quartus software, customers can also submit service requests directly to Altera Applications and monitor their progress via the Internet. The design files and configuration details can be prepared automatically for transfer to Altera. This feature ensures that the Altera Applications engineer working on the issue can accurately duplicate the design environment.

Automatic notifications of software patches, new device support, and on-line help updates are communicated on a regular basis by the Quartus software. Users are prompted to download the latest software upgrades. Designers can choose to have the Quartus software update their design site to ensure access to the latest information.

Subscription Program

The Altera subscription program gives designers access to the most cost-effective, fastest, and highest density PLDs in the industry. As new device families, packages, and speed grades become available, customers will automatically receive support for these Altera devices. The Altera Subscription Program provides a number of benefits, including:

- *New Device Support*—Altera offers devices with the highest density and performance in the industry. Altera continues to offer additional devices and package options, which allow designers to create advanced systems.
- *New Software Features*—An active subscription provides the Quartus and MAX+PLUS® II software as well as all Altera development system updates and releases over the duration of the 12-month subscription period.
- *Programming Methods*—The Quartus and MAX+PLUS II development systems support the latest programming methods, e.g., in-system programmability (ISP), in-circuit reconfigurability (ICR), and the Jam™ programming and test language. Altera continues to enhance its programming hardware and software to make these programming methods easily accessible.
- *Third-Party EDA Interfaces*—The Quartus software provides interfaces to all major EDA design tools as a standard feature. These interfaces allow designers to work in the most familiar design environment and implement designs in any Altera device family. Altera will continually enhance the Quartus design environment to stay current with other EDA tool improvements and upgrades.

Recommended System Configurations

To run the Quartus software with optimum results, Altera recommends the following preliminary system configurations.

For the most up-to-date information regarding system requirements, refer to the Quartus **read.me** file.

PC System Configuration

- 400 MHz or better Windows-based PC
- 256 Mbytes to 1 Gbyte of system memory (The largest devices require up to 1 Gbyte of memory. See the Quartus **read.me** file for memory recommendations.)
- 4 Gbytes of hard disk space
- Microsoft Windows NT version 4.0 or higher
- Internet Explorer version 4.0 or higher
- Microsoft Windows-compatible graphics card and 17-inch color monitor
- CD-ROM drive
- Microsoft Windows-compatible 2-button mouse
- 8-bit ISA slot for the programmer card
- Parallel port (i.e., LPT port) for the ByteBlasterMV parallel port download cable
- RS-232 serial/USB port for the MasterBlaster communications cable

Sun Ultra 2 SPARCstation System Configuration

- 256 Mbytes to 1 Gbyte of system memory (The largest devices require up to 1 Gbyte of memory. See the Quartus **read.me** file for memory recommendations.)
- Sun Ultra 2 SPARCstation with color monitor
- Sun OpenWindows 3.0 or higher or CDE
- Solaris 2.6 or higher
- ISO 9660-compatible CD-ROM drive
- RS-232 serial port for the MasterBlaster communications cable

HP 9000 Series 700/800 Workstation System Configuration

- 256 Mbytes to 1 Gbyte of system memory (The largest devices require up to 1 Gbyte of memory. See the Quartus **read.me** file for memory recommendations.)
- HP 9000 Series 700/800 workstation with color monitor
- HP-UX version 10.20 or higher
- HP-VUE or CDE
- ISO 9660-compatible CD-ROM drive
- RS-232 serial port for the MasterBlaster communications cable

Revision History

The information in the Quartus Programmable Logic Development System & Software Data Sheet version 1.01 supersedes information contained in previous versions. In this document, the recommended system configuration for the Sun Ultra 2 SPARC station was updated.

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