SignalTap Embedded Logic Analyzer Megafunction

Features

- Provided with the Quartus™ software
- Views internal nodes while the design is running at system speeds
- Requires no design modification to use the logic analyzer megafunction
- Optimized for APEX™ 20K devices
- Provides non-intrusive probing of ball-grid array (BGA) pins
- Logic analyzer controls that are available within the Quartus development environment include:
  - Signal selection
  - Trigger setup
  - Memory configuration
  - Waveform display

General Description

The new SignalTap™ analyzer megafunction supports system-on-a-programmable-chip integration. Signal selection, logic analyzer control, and signal display are all accessible within the Quartus development system. The MasterBlaster™ communications cable supports data transfer between the APEX 20K device and the Quartus software. With this data, designers can analyze and verify designs.

Functional Description

The SignalTap megafunction is a parameterized embedded logic analyzer that provides access to signals inside an APEX 20K device. The embedded logic analyzer captures signals from the internal nodes while the device is running in-system and at-speed. The SignalTap megafunction can use APEX 20K internal embedded system block (ESB) RAM to store acquisition data.

The Quartus software can automatically instantiate the SignalTap logic analyzer without making changes to the design file. Data captured by the logic analyzer is transferred to a host computer by using the MasterBlaster communications cable via a serial or universal serial bus (USB) port. See Figure 1.

Figure 1. SignalTap Logic Analyzer
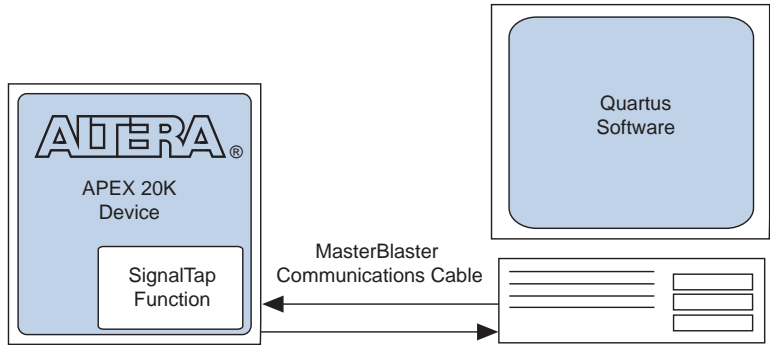
Triggering Conditions

Any input signal channel can be set to a variety of trigger conditions. Table 1 lists these conditions.

Table 1. Channel Trigger Conditions	
Trigger Condition	**Description**
Don't Care	Default trigger condition. The channel is not used to determine the trigger event.
Low	The analyzer triggers when the channel is low.
High	The analyzer triggers when the channel is high.
Falling	The analyzer triggers when the channel is falling.
Rising	The analyzer triggers when the channel is rising.
Rising or Falling Edge	The analyzer triggers when the channel is rising or falling.

Trigger I/O

An unused I/O pin can be used as an external output to indicate that a trigger event has occurred. The polarity of the output pulse may be specified as high or low. An unused I/O pin can also be used to trigger the embedded logic analyzer by setting the Trigger to recognize a high, low, rising edge, falling edge, either edge, or don't care condition.

Device Resource Usage

The number of logic elements (LEs) used by the logic analyzer is a function of the number of channels used. Table 2 shows an estimate of the number of LEs consumed by the logic analyzer.

Table 2. Logic Analyzer LE Consumption	
Channels Used	**LEs**
1	136
2	144
4	160
8	192
16	256
32	384
64	640
128	1,152

The embedded logic analyzer can use internal memory (i.e., ESBs) for acquisition data storage. The size and number of these blocks are device-dependent and must be considered when configuring the logic analyzer. The number of RAM bits consumed depends on the number of channels used and the number of samples taken. Table 3 shows the number of ESBs used to store the values for different configurations.

| Table 3. APEX 20K ESB Memory Depth					
Channels	**Buffer Samples**				
	128	**256**	**512**	**1,024**	**2,048**
1	1	1	1	1	1
2	1	1	1	1	2
4	1	1	1	2	4
8	1	1	2	4	8
16	1	2	4	8	16
32	2	4	8	16	32
64	4	8	16	32	64
128	8	16	32	64	128

Logic Analyzer Configurations

The SignalTap embedded logic analyzer provides several data configurations that can be used in any combination. The configurations are:

- Embedded logic analyzer
- Debug port
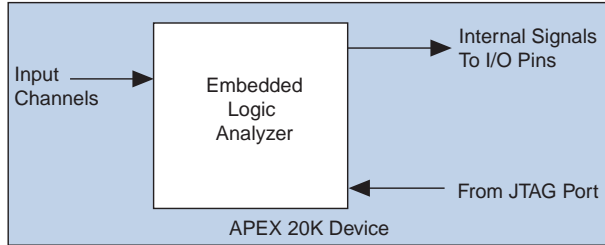- Trigger output

Embedded Logic Analyzer

In the embedded logic analyzer configuration, I/O pins and internal nodes can be connected to input channels for data capture. The analyzer clock signal comes from an internal global clock. The acquisition data is placed in RAM and then streamed off-chip via the IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface. See Figure 2. The optional trigger in and trigger out signals can be routed to spare I/O pins to synchronize the embedded logic analyzer to external test equipment or to circuitry and vice-versa.

Figure 2. Embedded Logic Analyzer Architecture
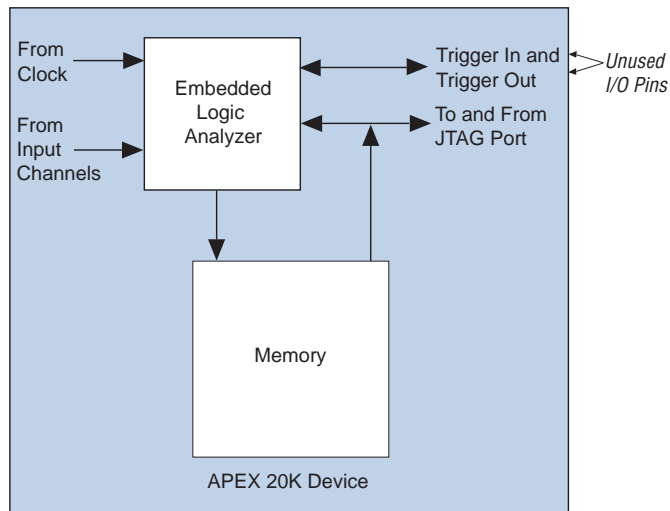
Debug Port

When device RAM is limited, you can route internal signals to unused I/O pins for capture by an external analyzer or oscilloscope. The debug port facility conserves ESBs at the expense of I/O pins, and is useful for data-intensive applications in which the amount of saved data exceeds the available sample buffer. See Figure 3.

Figure 3. Device Debugging Port

Trigger Output

The trigger out signal can be used to generate a pulse on a spare I/O pin when the embedded logic analyzer trigger pattern is recognized. The trigger out pulse can be set to active high or active low, and remains active until the input signals no longer match the trigger pattern. Trigger out requires no ESBs and only one I/O pin. See Figure 4.

Figure 4. Using the Logic Analyzer as an Event Analyzer
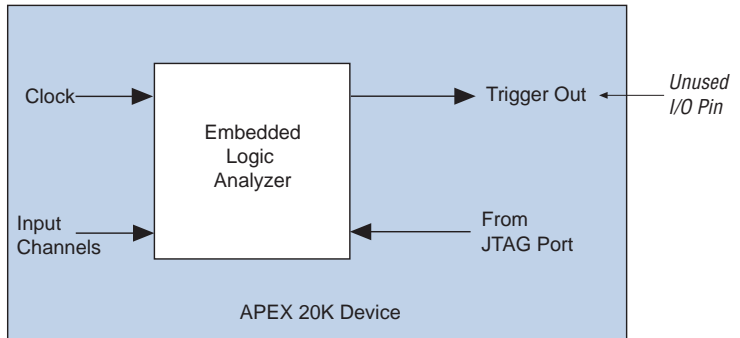
Quartus & MasterBlaster Support

All setup, control, and display functions for the SignalTap analyzer are integrated into the Quartus development software. The MasterBlaster communications cable uploads required data from internal nodes to the Quartus software, where they are displayed in the Waveform Editor window.

The MasterBlaster communications cable downloads information at high speeds to APEX 20K devices. The USB host interface supports download bit stream rates up to 12 megabits per second to the target device. An RS-232 port is also provided and runs at speeds up to 115k baud. A JTAG interface connects to the target device for design download and acquisition buffer retrieval. The MasterBlaster cable supports I/O voltages for the entire range of Altera devices.

See the *MasterBlaster Serial/USB Communications Cable Data Sheet* for more information.

Conclusion

With the SignalTap embedded analyzer megafunction, internal device signals can be monitored in a variety of ways without affecting device performance. Triggering, system resource management, and configuration can be controlled using the Quartus software in conjunction with the MasterBlaster communications cable. Data may be routed externally to unused I/O pins or to a JTAG port. Analyzed data is useful for debugging designs and optimizing system performance.

Revision History

Information contained in the *SignalTap Embedded Logic Analyzer Megafunction Data Sheet* version 1.01 supersedes information published in previous versions. Version 1.01 contains the following changes:

- The "Functional Description", "Trigger I/O", "Logic Analyzer Configurations", "Embedded Logic Analyzer", "Debug Port", "Trigger Output", and "Quartus & MasterBlaster Support" sections were updated.
- Table 3 on page 3 was updated.
- Figures 2 and 3 were updated.
- The "Time & Count", "Sequence", "SignalTap Support", "Delay", "Acquisition RAM", and "Routing Internal Signals to I/O Pins" sections were deleted.
- Figure 5 was deleted.

nsai

I.S. EN ISO 9001

Printed on Recycled Paper.