

Features

- Uses the Altera® `fft` MegaCore™ function
- Optimized for the Altera FLEX® 10K device architecture
- Uses FLEX 10K embedded array blocks (EABs) to store both data and twiddle factors
- Supported by the Altera MAX+PLUS® II software
- Parameterized number of points and data width

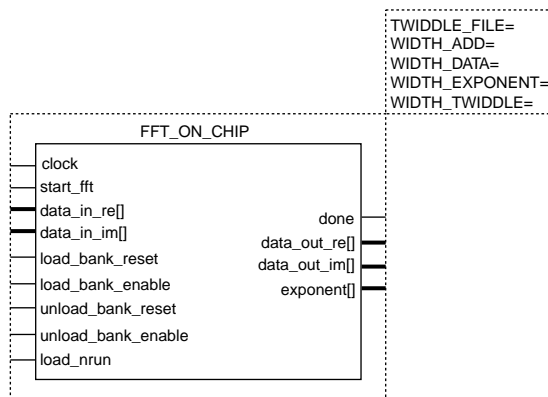
General Description

The `fft_on_chip` reference design implements a fast Fourier transform (FFT) function using the Altera `fft` MegaCore function. The `fft` function provides maximum flexibility by allowing the designer to choose the memory and I/O interface.

The `fft_on_chip` design has a memory architecture that consists of left, right, and twiddle memory banks. Each memory bank has both real and imaginary elements that are read in parallel. The `fft_on_chip` uses FLEX 10K EABs for all the memory banks, allowing an EPF10K100 device to implement an `fft` function with up to 256 data points and a 16-bit data width.

Figure 1 shows the symbol for the `fft_on_chip` reference design.

Figure 1. `fft_on_chip` Symbol



Function Prototype

The Altera Hardware Description Language (AHDL™) Function Prototype for the `fft_on_chip` reference design is shown below:

```
FUNCTION fft_on_chip (clock, start_fft,
    data_in_re[WIDTH_DATA-1..0],
    data_in_im[WIDTH_DATA-1..0], load_bank_reset,
    load_bank_enable, unload_bank_reset,
    unload_bank_enable, load_nrun)
WITH (WIDTH_DATA, TWIDDLE_FILE, WIDTH_TWIDDLE,
    WIDTH_EXPONENT, WIDTH_ADD)
RETURNS (done, data_out_re[WIDTH_DATA-1..0],
    data_out_im[WIDTH_DATA-1..0],
    exponent[WIDTH_EXPONENT-1..0]);
```

VHDL Component Declaration

The VHDL Component Declaration for the `fft_on_chip` reference design is shown below:

```
COMPONENT fft_on_chip
GENERIC(
    TWIDDLE_FILE      : STRING;
    WIDTH_ADD         : POSITIVE;
    WIDTH_DATA        : POSITIVE;
    WIDTH_EXPONENT    : POSITIVE;
    WIDTH_TWIDDLE     : POSITIVE;
);
PORT(
    clock : IN STD_LOGIC := '0';
    start_fft, load_bank_reset, load_bank_enable,
    unload_bank_reset, unload_bank_enable,
    load_nrun : IN STD_LOGIC;
    data_in_re,
    data_left_in_im :
    IN STD_LOGIC_VECTOR(WIDTH_DATA-1 DOWNT0 0);
    done : OUT STD_LOGIC;
    data_out_re, data_out_im :OUT
    STD_LOGIC_VECTOR(WIDTH_ADD - 1 DOWNT0 0);
    exponent : OUT
    STD_LOGIC_VECTOR(WIDTH_EXPONENT-1 DOWNT0 0));
END COMPONENT;
```

Ports

Table 1 shows the ports for the `fft_on_chip` reference design.

Name	Type	Required	Description
<code>clock</code>	Input	Yes	Clock signal.
<code>start_fft</code>	Input	Yes	Starts the <code>fft</code> processor after data is loaded.
<code>data_in_re[]</code>	Input	Yes	Real data input.
<code>data_in_im[]</code>	Input	Yes	Imaginary data input.
<code>load_bank_reset</code>	Input	Yes	Resets the load counter.
<code>load_bank_enable</code>	Input	Yes	Enables the load counter.
<code>unload_bank_reset</code>	Input	Yes	Resets the unload counter.
<code>unload_bank_enable</code>	Input	Yes	Enables the unload counter.
<code>load_nrun</code>	Input	Yes	Places <code>fft_on_chip</code> in either load or run mode. When <code>load_nrun</code> is high, the left and right memory banks are controlled by the load and unload counters and other input signals. When <code>load_nrun</code> is low, the memory banks are controlled by the <code>fft</code> MegaCore function.
<code>done</code>	Output	Yes	Goes high when the <code>fft</code> function has completed the calculation and data is available for unloading.
<code>data_out_re[]</code>	Output	Yes	Real data output.
<code>data_out_im[]</code>	Output	Yes	Imaginary data output.
<code>exponent[]</code>	Output	Yes	Exponent of the resultant data.

Parameters

Table 2 shows the parameters for the `fft_on_chip` reference design.

Name	Value	Description
<code>TWIDDLE_FILE</code>	String	Contains the ROM for the twiddle memory bank.
<code>WIDTH_ADD</code>	Integer	Data address bus width within <code>fft_on_chip</code> . The number of points is $2^{\text{WIDTH_ADD}}$.
<code>WIDTH_DATA</code>	Integer	Data width.
<code>WIDTH_EXPONENT</code>	Integer	Number of bits in the exponent, which is calculated by $\text{ceil}(\log_2(2 \times \text{WIDTH_ADD})) + 1$.
<code>WIDTH_TWIDDLE</code>	Integer	Twiddle width. There are $2^{\text{WIDTH_ADD} - 1}$ twiddles.

Functional Description

The `fft_on_chip` reference design is made up of several essential parts, which are described below:

- *fft MegaCore function*—Controls all aspects of the actual FFT computation. The `fft` MegaCore function is active when the `load_nrun` input is driven low.
- *Left and right memory banks*—A dual memory architecture in which data is simultaneously read from one memory bank and written to the other. The memory banks are made up of RAM blocks that are $2 \times \text{WIDTH_DATA}$ bits wide and $2^{\text{WIDTH_ADD}}$ words deep, and the memory banks hold both real and imaginary data elements. The width of the address bus port is `WIDTH_ADD`.
- *Twiddle memory bank*—A ROM block that is $2 \times \text{WIDTH_TWIDDLE}$ bits wide and $2^{\text{WIDTH_ADD} - 1}$ words deep. It holds the real and imaginary elements of the twiddle factors. The twiddle memory does not require a write enable signal or an I/O interface; it connects directly to the `fft` MegaCore function.
- *Load and unload counters*—Both counters are `WIDTH_ADD` bits wide. The load counter counts through the addresses when loading the right memory bank in normal bit order. The unload counter counts through the addresses for the left memory bank in bit-reversed order.

To use the `fft_on_chip` reference design, follow these steps:

1. Reset the load and unload counters by asserting the `load_bank_enable` and `unload_bank_reset` inputs for one or more clock cycles.
2. Drive the `load_nrun` input high to place the `fft` MegaCore into load mode.
3. Drive the `load_bank_enable` input high for $2^{\text{WIDTH_ADD} - 1}$ clock cycles while applying data to the `data_in_re[]` and `data_in_im[]` inputs. The `load_bank_enable` input can be driven high and low to accommodate the incoming data.

If the `fft` function has already completed a calculation, the `unload_bank_enable` input may be asserted to retrieve the data from the `data_out_re[]` and `data_out_im[]` outputs. The loading and unloading of data are independent and carried out in any desirable order. After the `unload_bank_enable` input is driven high, there are four (`WIDTH_ADD` is odd) or five (`WIDTH_ADD` is even) pipeline stages, and valid data is received on the `data_out_re[]` and `data_out_im[]` outputs.

4. Drive the `load_nrun` input low to place the entire design into run mode.
5. Drive the `start_fft` input high for one clock cycle to instruct the `fft` MegaCore function to begin processing the loaded data.



Remember to unload all data currently in the memory, because the `fft` MegaCore function will overwrite any old data.

6. Repeat steps 2 to 6 after done output goes high.



For instructions on how to instantiate and simulate the `fft_on_chip` reference design, see *Application Note 84 (Implementing `fft` with On-Chip RAM in FLEX 10K Devices)*.

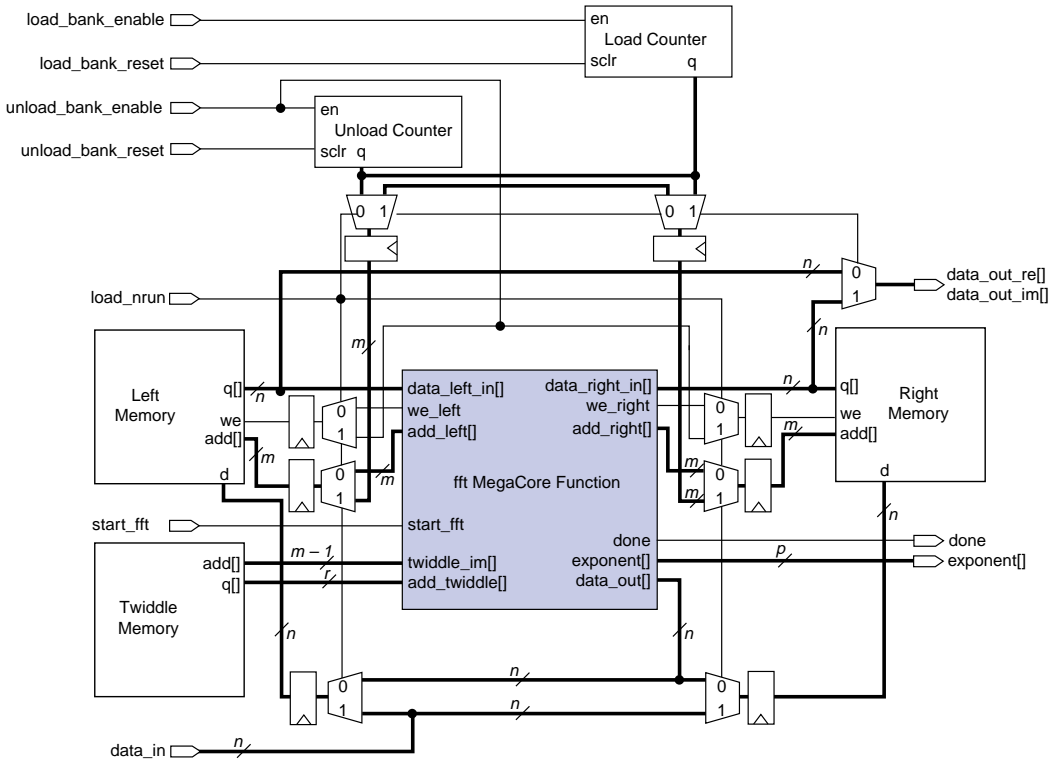
Example Implementations

Figures 2 and 3 show two possible implementations of the `fft_on_chip` reference design. Both implementations are embedded in the MAX+PLUSII `fft_on_chip` Text Design File (`fft_on_chip.tdf`). The parity of `WIDTH_ADD` (i.e., odd or even) determines which configuration will be used.

Figure 2 shows an implementation of the `fft_on_chip` reference design when `WIDTH_ADD` is odd.

Figure 3 shows an implementation of the `fft_on_chip` reference design when `WIDTH_ADD` is even.

Figure 3. `fft_on_chip` Block Diagram Reference Design When `WIDTH_ADD` Is Even



where: $m = \text{WIDTH_ADD}$
 $n = 2 \times \text{WIDTH_DATA}$
 $p = \text{WIDTH_EXPONENT}$
 $r = \text{WIDTH_TWIDDLE}$

Figure 4 shows a load and unload cycle for the `fft_on_chip` function when `WIDTH_ADD` is 3. The data is loaded, and `start_fft` is asserted. When `done` goes high, the process is repeated. If desired, data can be individually loaded and unloaded by asserting the `load_bank_enable` and `unload_bank_enable` inputs at different times (i.e., once the `done` output goes high).

Figure 4. `fft_on_chip` Whole Load & Unload Cycle

X indicates "don't care." DV indicates "data valid."

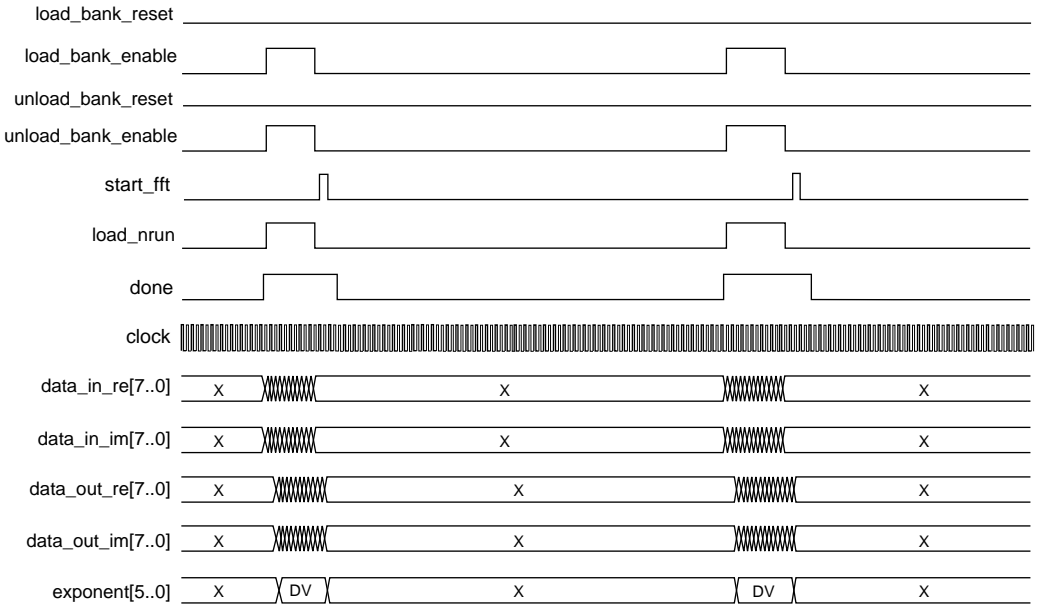
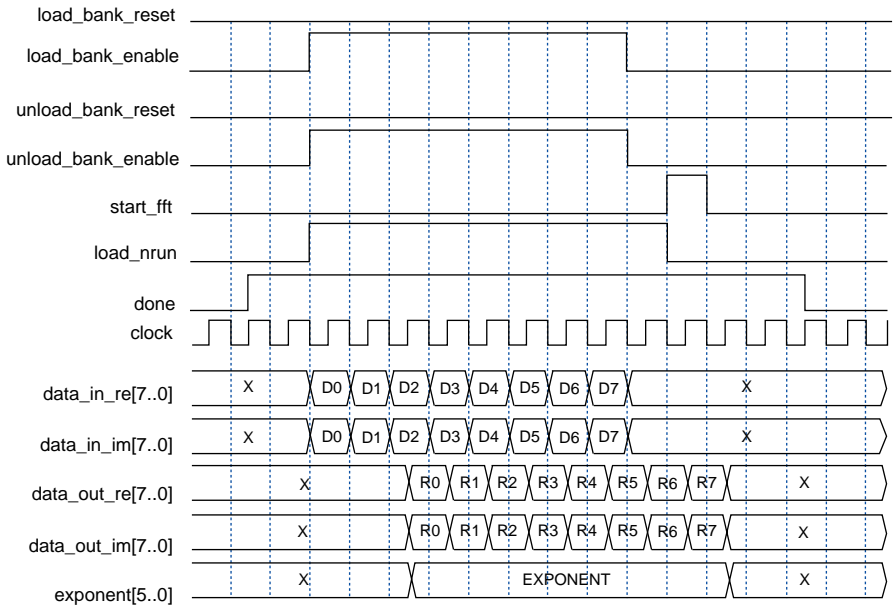


Figure 5 shows the simultaneous loading and unloading of data when WIDTH_ADD is 3. A pipeline delay of three clock cycles exists between the time when the unload_bank_enable input is asserted and valid data is received on the data_out_re[] and data_out_im[] outputs, whenever WIDTH_ADD is odd.

Figure 5. fft_on_chip Simultaneous Load & Unload Cycle When WIDTH_ADD is 3

X indicates "don't care."

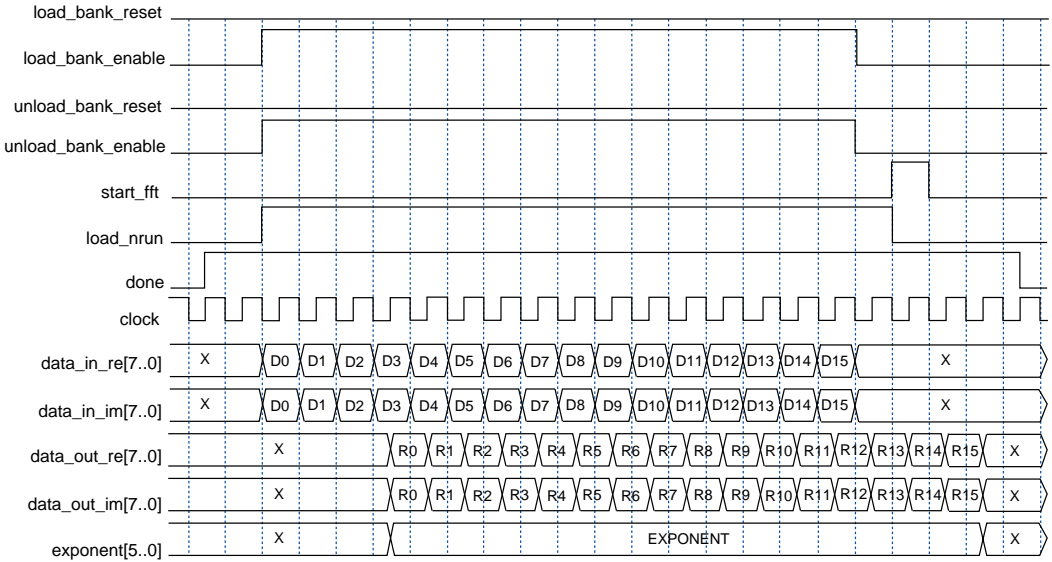


FS 7: fft_on_chip Fast Fourier Transform

Figure 6 shows the simultaneous loading and unloading of data when WIDTH_ADD is 4. A pipeline delay of three clock cycles exists between the time unload_bank_enable input is asserted and valid data is received on the data_out_im[] and data_out_re[] outputs.

Figure 6. fft_on_chip Simultaneous Load & Unload Cycle When WIDTH_ADD is 4

X indicates "don't care."





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