

May 1999

The *1999 Data Book* uses the following abbreviations and acronyms:

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| ACAP | Altera Consultants Alliance Program |
| ACCESS | Altera Commitment to Cooperative Engineering Solutions |
| AHDL | Altera Hardware Description Language |
| AMPP | Altera Megafunction Partners Program |
| APEX | Advanced Programable Embedded Matrix |
| APD | Active parallel down |
| APU | Active parallel up |
| AN | Application note |
| AS | Active serial |
| ASCII | American Standard Code for Information Interchange |
| ASIC | Application-specific integrated circuit |
| ASSP | Application-specific standard product |
| ATM | Asynchronous transfer mode |
| BGA | Ball-grid array |
| BNF | Backus-Naur form |
| BPR | Bypass register |
| BSC | Boundary-scan cell |
| BSDL | Boundary-scan description language |
| BST | Boundary-scan test |
| CAE | Computer-aided engineering |
| CAM | Content addressable memory |
| CerDIP | Ceramic dual in-line package |
| CMD | Command File |
| CMOS | Complementary metal-oxide semiconductor |
| CPLD | Complex programmable logic device |
| CPU | Central processing unit |
| CQFP | Ceramic quad flat pack |
| CRC | Cyclic redundancy code |
| DIP | Dual in-line package |
| DRAM | Dynamic random access memory |
| DS | Data sheet |
| DSP | Digital signal processing |
| DUT | Device under test |
| EAB | Embedded array block |
| EAU | Electronic application utility |
| EDA | Electronic design automation |
| EDF | EDIF Input File |

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|--------|---|
| EDIF | Electronic Design Interchange Format |
| EEPROM | Electrically erasable programmable read-only memory |
| EPLD | Erasable programmable logic device |
| EPROM | Erasable programmable read-only memory |
| ESB | Embedded system block |
| ESD | Electrostatic discharge |
| FFT | Fast Fourier transform |
| FIFO | First-in first-out |
| FIN | Fitter Input File (.fin) |
| FIR | Finite impulse response |
| FIT | Fit File (.fit) |
| FLEX | Flexible Logic Element MatriX |
| FPGA | Field-programmable gate array |
| FTP | File transfer protocol |
| GAL | Generic array logic |
| GDF | Graphic Design File (.gdf) |
| GTL | Gunning transceiver logic |
| HDL | Hardware description language |
| HEX | Hexadecimal File |
| IC | Integrated circuit |
| ICR | In-circuit reconfigurability |
| ICT | In-circuit test |
| IEEE | Institute of Electrical and Electronic Engineers |
| IIR | Infinite impulse response |
| INC | Include File (.inc) |
| INI | Initialization File (.ini) |
| I/O | Input/output |
| IOC | Input/output cell |
| IOE | Input/output element |
| IR | Instruction register |
| ISA | Industry-standard architecture |
| ISP | In-system programmability |
| JCF | JTAG Chain File (.jcf) |
| JED | JEDEC File (.jed) |
| JLCC | Ceramic J-lead chip carrier |
| JTAG | Joint Test Action Group |
| LAB | Logic array block |
| LCA | Logic cell array |
| LE | Logic element |
| LED | Light-emitting diode |
| LMF | Library Mapping File (.lmf) |
| LOG | Log File (.log) |
| LPM | Library of parameterized modules |
| LSB | Least significant bit |
| LSI | Large-scale integration |

| | |
|---------|---|
| LUT | Look-up table |
| LVC MOS | Low-voltage complementary metal-oxide semiconductor |
| LVDS | Low-voltage differential signaling |
| LVTTL | Low-voltage transistor-transistor logic |
| MAC | Multiplier-accumulator |
| MAX | Multiple Array Matrix |
| MD-SAS | Multi-device sequential active serial |
| MMF | MAX+PLUS II Message File (.mmf) |
| MPU | Master programming unit |
| MRI | Magnetic resonance imaging |
| MSB | Most significant bit |
| MSI | Medium-scale integration |
| MSPS | Million samples per second |
| MTBF | Mean time between failures |
| MTF | Message Text File (.mtf) |
| NRE | Non-recurring engineering |
| OCR | Optical character recognition |
| OEM | Original equipment manufacturer |
| OTP | One-time-programmable |
| PAL | Programmable array logic |
| PC | Personal computer |
| PCB | Printed circuit board |
| PCI | Peripheral component interconnect |
| PDIP | Plastic dual in-line package |
| PGA | Pin-grid array |
| PIA | Programmable interconnect array |
| PIB | Product information bulletin |
| PLCC | Plastic J-lead chip carrier |
| PLD | Programmable logic device |
| PLL | Phase-locked loop |
| POF | Programmer Object File (.pof) |
| POR | Power-On Reset |
| PPA | Passive parallel asynchronous |
| PPS | Passive parallel synchronous |
| PQFP | Plastic quad flat pack |
| PROM | Programmable read-only memory |
| PS | Passive serial |
| QFP | Quad flat pack |
| RAM | Random access memory |
| ROM | Read-only memory |
| RPT | Report File (.rpt) |
| RQFP | Power quad flat pack |
| RTL | Register transfer level |
| SAM | Stand-Alone Microsequencer |
| SOF | SRAM Object File (.sof) |
| SOIC | Small-outline integrated circuit |

Abbreviations

| | |
|---------|--|
| SR | Staging register |
| SRAM | Static random access memory |
| SSG | Synchronous signal generator |
| SSI | Small-scale integration |
| SSTL | Stub series terminated logic |
| SYM | Symbol File (.sym) |
| TDF | Text Design File (.tdf) |
| TQFP | Thin quad flat pack |
| TTF | Tabular Text File (.tff) |
| TTL | Transistor-to-transistor logic |
| UES | User electronic signature |
| UV | Ultraviolet |
| VEC | Vector File (.vec) |
| VHD | VHDL Design File (.vhd) |
| VHDL | VHSIC Hardware Description Language |
| VHSIC | Very high speed integrated circuit |
| VITAL | VHDL Initiative Toward ASIC Libraries |
| VLSI | Very large-scale integration |
| WDF | Waveform Design File (.wdf) |
| WWW | World-wide web |
| WYSIWYG | What-you-see-is-what-you-get |
| XNF | Xilinx Netlist Format File (.xnf) |
| ZIF | Zero-insertion-force |