EDA Software Support

November 1998, ver. 7.01

Introduction

Seamless design flow and high-quality integration of third party EDA tools are essential to the continued success of programmable logic devices (PLDs). Thus, Altera has established the Altera Commitment to Cooperative Engineering Solutions (ACCESS℠) program. Through the ACCESS program, Altera and key EDA vendors jointly develop and market next-generation high-level design tools and methodologies. Altera provides EDA partners with critical technical information and assistance, and ACCESS partners dedicate resources to ensure the best quality design results for Altera architectures.

The ACCESS program provides a total solution that allows designers to generate and verify multiple design revisions in a single day, greatly reducing the product development cycle.

Altera has been a leader in support of industry standards, such as EDIF, VHDL, Verilog HDL, VITAL, and the library of parameterized modules (LPM). Altera has also made a commitment to support current ACCESS partner design flows.

For more information on software support provided by Altera, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

This document identifies the type of product(s) available from each ACCESS partner, i.e., design entry, compilation/synthesis, timing analysis, functional simulation, and timing simulation. These products either support Altera devices directly or provide an interface to the MAX+PLUS® II development software. In addition, the MAX+PLUS II software contains the necessary interfaces and libraries to support many EDA tools. Altera recommends contacting EDA software manufacturers directly for details on product features, specific device support, and product availability. Table 1 lists third-party tool support for Altera devices.

Go to the Altera world-wide web site (**http://www.altera.com**) for up-to-date information on:

- ACCESS partner support for Altera devices.
- MAX+PLUS II ACCESS Key Interface Guidelines for Cadence, Mentor Graphics, Synopsys, Viewlogic, and other EDA vendors.

Table 1. Third-Party Tool Support for Altera Devices (Part 1 of 3)

Company	Design Entry	Compilation/ Synthesis	Timing Analysis	Functional Simulation	Timing Simulation
ACCEL Technologies, Inc. **http://www.acceltech.com** TEL: (619) 554-1000 FAX: (619) 554-1019	✓				
Accolade Design Automation, Inc. **http://www.acc-eda.com** TEL: (425) 844-6479 1-800-470-2686 FAX: (425) 788-3768	✓	✓		✓	✓
ACEO Technology **http://www.aceo.com** TEL: (510) 668-1700 FAX: (510) 668-0700		✓	✓		
ACUGEN Software, Inc. **http://www.acugen.com** TEL: (603) 881-8821 FAX: (603) 881-8906			✓	✓	✓
ALDEC, Inc. **http://www.aldec.com** TEL: (805) 499-6867 FAX: (805) 498-7945	✓	✓		✓	✓
Cadence Design Systems, Inc. **http://www.cadence.com** TEL: (408) 943-1234 FAX: (408) 943-0513	✓			✓	✓
COMPASS Design TEL: (800) 433-4880 FAX: (408) 434-7977	✓	✓			
Exemplar Logic, Inc. **http://www.exemplar.com** TEL: (510) 337-3700 FAX: (510) 337-3799		✓	✓		
Flynn Systems Corporation **http://www.flynn.com** TEL: (603) 598-4444 FAX: (603) 337-3799				✓	

Table 1. Third-Party Tool Support for Altera Devices (Part 2 of 3)

Company	Design Entry	Compilation/ Synthesis	Timing Analysis	Functional Simulation	Timing Simulation
IK Technology Corporation, Ltd. (Japan) **http://www.cgc.co.jp** TEL: (81) 3-3464-5551 FAX: (81) 3-3464-5689	✓	✓			
IKOS Systems, Inc. **http://www.ikos.com** TEL: (408) 255-4567 FAX: (408) 366-8699				✓	✓
i-Logix, Inc. **http://www.ilogix.com** TEL: (508) 682-2100 FAX: (508) 682-5995	✓			✓	
ISDATA GmbH (Germany) **http://www.intsys-europe.fr** TEL: (49) 721/75 10 87 FAX: (49) 721/75 26 34	✓	✓		✓	✓
Mentor Graphics Corporation **http://www.mentor.com** TEL: (503) 685-7000 FAX: (503) 685-7704	✓	✓	✓	✓	✓
MINC/Synario **http://www.minc.com** TEL: (719) 590-1155 FAX: (719) 590-7330	✓	✓		✓	✓
Model Technology, Inc. **http://www.model.com** TEL: (503) 641-1340 FAX: (503) 526-5410				✓	✓
OrCAD, Inc. **http://www.orcad.com** TEL: (503) 671-9500 1-800-671-9505 FAX: (503) 671-9501	✓	✓		✓	✓
Sophia Systems and Technology **http://www.sophia.com** TEL: (408) 943-9300 FAX: (408) 943-9303	✓				

Table 1. Third-Party Tool Support for Altera Devices (Part 3 of 3)

Company	Design Entry	Compilation/ Synthesis	Timing Analysis	Functional Simulation	Timing Simulation
Summit Design, Inc. **http://www.summit-design.com** TEL: (503) 643-9281 FAX: (503) 646-4954	✓			✓	
Synopsys, Inc. **http://www.synopsys.com** TEL: (650) 962-5000 FAX: (650) 965-8637		✓		✓	✓
Synplicity, Inc. **http://www.synplicity.com** TEL: (408) 617-6000 FAX: (408) 617-6001		✓	✓		
Veda, Inc. **http://www.veda.co.uk** TEL: (800) 600-VEDA FAX: (408) 970-0174	✓	✓			
VeriBest Incorporated **http://www.veribest.com** TEL: (650) 691-9680 1-800-837-4237 FAX: (650) 691-9016	✓	✓		✓	✓
Viewlogic Systems, Inc. **http://www.viewlogic.com** TEL: (508) 480-0881 FAX: (508) 480-0882	✓	✓	✓	✓	✓

Interfaces

The MAX+PLUS II development software fully supports the following design environments and provides interfaces to these tools:

- Cadence Logic Workbench and Design Framework II
- Mentor Graphics Falcon Framework
- Synopsys
- Synplicity
- Viewlogic Powerview and Workview Office

The features supported in the Cadence, Mentor Graphics, Viewlogic, and Synopsys interfaces with the MAX+PLUS II software are summarized in the following sections.

Altera/Cadence Interface

By combining Cadence design entry, synthesis, and verification tools (i.e., Logic Workbench and Design Framework II) with the MAX+PLUS II software, designs can be implemented in any Altera PLD.

The Altera/Cadence interface supports a top-down or mixed-level design methodology. Designs can be entered as a mixture of schematics, VHDL, and Verilog HDL. The Altera/Cadence interface supports the following features:

- Fully integrated design environment
- Easy-to-use, top-down design environment
- Schematic, Verilog HDL, or VHDL design entry
- EDIF netlist files that contain timing information for simulation
- LPM, version 2.1.0
- Full timing simulation
- VITAL-compliant library
- RAM/ROM support
- Design description with architecture-independent design entry libraries
- Altera-provided **gencklk** utility, which generates simulation models
- Short design cycles with the MAX+PLUS II software's automatic device selection, fitting, and multi-device partitioning

Altera/Mentor Graphics Interface

By combining Mentor Graphics design entry, synthesis, and verification tools (i.e., Falcon Framework) with the MAX+PLUS II software, designs can be implemented in any Altera PLD.

The Altera/Mentor Graphics design flow supports a top-down or mixed-level design methodology. Designs can be entered as a mixture of schematics and VHDL. The Altera/Mentor Graphics interface supports the following features:

- Fully integrated design environment
- Easy-to-use, top-down design environment
- Schematic design entry
- Industry-standard behavioral design entry with VHDL (supporting both IEEE Std. 1076-1987 and 1076-1993) and the Altera Hardware Description Language (AHDL), including syntax coloring and HDL templates in the MAX+PLUS II Text Editor
- Full timing simulation
- VITAL-compliant library
- LPM, version 2.1.0
- RAM/ROM support

- Altera-provided **genclklk** utility, which generates simulation models for ClockLock™ and ClockBoost™ features
- Design description with architecture-independent design entry libraries
- Short design cycles with the MAX+PLUS II software's automatic device selection, fitting, and multi-device partitioning

Altera/Synopsys Interface

The Altera/Synopsys interface brings high-level design methodology to high-density programmable logic. This interface contains Altera synthesis and simulation libraries, which describe logic functions that can be used to implement designs in Altera PLDs using FPGA or Design Compiler. The Altera/Synopsys interface supports the following features:

- Fully integrated design environment
- Full timing simulation
- VITAL-compliant library
- Industry-standard behavioral design entry with VHDL, Verilog HDL, and AHDL
- Synopsys timing constraints supported in the MAX+PLUS II Assignment & Configuration File (**.acf**) format
- RAM/ROM for the FLEX 10K family with the Altera-provided **genmem** utility, which generates timing and simulation models
- Altera-provided **genclklk** utility, which generates simulation models for ClockLock™ and ClockBoost™ features
- Different device speed grades for FLEX 10K, FLEX 8000, and FLEX 6000 devices
- Short design cycles with the MAX+PLUS II software's automatic device selection, fitting, and multi-device partitioning
- Synopsys-provided Altera interfaces for FPGA Express

Altera/Viewlogic Interface

By combining Viewlogic design entry, synthesis, and verification tools (i.e., Powerview and Workview Office) with the MAX+PLUS II software, designs can be implemented in any Altera PLD.

The Altera/Viewlogic design flow supports a top-down or mixed-level design methodology. Designs can be entered as a mixture of schematics, VHDL, and AHDL. The Altera/Viewlogic interface supports the following features:

- Fully integrated design environment
- Industry-standard behavioral design entry with VHDL and AHDL
- Easy-to-use, top-down design environment
- Schematic design entry

- Full timing simulation
- LPM, version 2.1.0
- RAM/ROM support
- Altera-provided **genclk** utility, which generates simulation models
- Design description with architecture-independent design entry libraries
- Short design cycles with the MAX+PLUS II software's automatic device selection, fitting, and multi-device partitioning

Revision History

The information contained in *EDA Software Support* version 7.01 supersedes information published in previous versions.

EDA Software Support version 7.01 contains the following changes:

- Added each vendor's world-wide web address to Table 1.
- Modified Table 1 to reflect the merger between Synario Design Automation and MINC, Incorporated.
- Added COMPASS Design to Table 1.
- Split the simulation/verification column in Table 1 into the timing analysis, functional simulation, and timing simulation columns.
- Made minor textual and style changes throughout the document.